The Path to Fault- and Intrusion-Resilient Manycore Systems on a Chip

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Abstract— The hardware computing landscape is changing. What used to be distributed systems can now be found on a chip with highly configurable, diverse, specialized and general purpose units. Such Systems-on-a-Chip (SoC) are used to control today's cyber-physical systems, being the building blocks of critical infrastructures. They are deployed in harsh environments and are connected to the cyberspace, which makes them exposed to both accidental faults and targeted cyberattacks. This is in addition to the changing fault landscape that continued technology scaling, emerging devices and novel application scenarios will bring. In this paper, we discuss how the very features-distributed, parallelized, reconfigurable, heterogeneous-that cause many of the imminent and emerging security and resilience challenges, also open avenues for their cure though SoC replication, diversity, rejuvenation, adaptation, and hybridization. We show how to leverage these techniques at different levels across the entire SoC hardware/software stack, calling for more research on the topic.

Index Terms—fault and intrusion tolerance, resilience, hardware, system on a chip, FPGA

I. OPPORTUNITIES FOR HARDWARE RESILIENCE

Hardware chips continue to be the core building blocks of computing devices due to their inherent immutability and speed, required in modern digital and mission-critical systems like Cyber-Physical Systems, Healthcare, Fintech, Automotive, and Space. This hardware can implement an entire monolithic system or even be used as proof-of-trust anchors. Contrary to the common belief, hardware is prone to unintentional (benign) and intentional/malicious (intrusion or Byzantine [1]) faults. The former can be caused by the fabrication (e.g., Silicon) material prone to dust, aging, and overheating, or by design/implementation glitches [2], [3]. Malicious faults manifest in many forms, prior- or post-fabrication, where stealthy logic, backdoors, trojans, kill switches, and postfab fabric editing are possible [4]-[7]. In line with this, the trends of building complex hardware out of smaller commercial-off-the-shelf (COTS) components and introducing programmable/reconfigurable hardware, e.g., FPGA [8], [9], are closing the gap with software systems: hardware systems are no longer rigid, immutable, and fixed creatures. This raises both new challenges and opportunities, which call to revisit the way resilient and secure hardware systems are built.

The notable demand on hardware due to the automation and digitalization of services in many sectors raised new challenges in the hardware fabrication industry, where vendors need to maintain delivery on time and reduce production costs. This resulted in a *divide-and-conquer* [10] production style: a system is split into smaller and cheaper building blocks, i.e., components. Components are developed in parallel to reduce the production cycle time. Each block is likely developed by a dedicated specialized vendor, i.e., generating COTS [11]. This means that the synthesising entity of these COTS can focus on the technology it masters, rather than distributing its efforts on multiple fronts. Despite this, these cheap components are becoming more prone to failures and attacks [12], which can lead to drastic impacts on critical sectors like Cyber-Physical Systems, health smart systems, mission-critical space systems, etc. Our experience in software systems shows that building resilient systems composed of small and cheap components can be more resilient than a single complex monolithic system, that is usually very expensive.

There are ample opportunities for hardware resilience leveraging the above advancements. To demonstrate this, we showcase in Fig. 1 different levels of the chip development process, from low-level fine-grained gate logic blocks up to multicore systems-on-chip (SoC). Literary works reveal some selected resiliency techniques on most of these layers for constructing resilient clock networks, replicated power domains, and lockstep coupling of cores [13]–[18], which is a good starting point. We, however, advocate for more systematic and comprehensive resiliency, probably leveraging hardware *hybrids* to simplify the designs. This holistic view helps optimising SoC designs by suggesting the right level of resiliency at each stage to reduce the redundant complexity and cost.

In a nutshell, the lowest level, in Fig. 1, is building a single layer microchip that constitutes a simple logical circuit of gates. Different gates are known to have different resiliency levels [13], [17]. Recently, SiNW transistors are used to bridge *Source* to *Drain* with multiple *nanowires* to compensate manufacturing defects and aging [19]. While a typical design process mainly considers the *space*, *energy*, and *time* metrics in the design, making these circuits more resilient would mean trading these metrics for resiliency, e.g., using backup gates, replicated parallel gates, or diverse gates [17], [18]. On the other hand, single-layered circuits can today be synthesized in a *3D fabric* [20]. Layers typically have different

complementary functionalities. However, they can also have layers of identical functionality from different vendors, which is useful to improve diversity in fault masking scenarios (discussed later). It is also helpful to synthesize a monolithic chip from multi-vendor layers to avoid vendor lock-in or potential aging issues, backdoors, and *kill switches* [2]–[4] so called *Distribution attack* on the supply chain.

At a higher level, always depicted in Fig. 1, these 3D microchips can be assembled to build a system-on-chip fabric [21]. Again, components of identical functionalities can be used to build fault and intrusion masking SoC fabric. This can be enriched with heterogeneous diverse microchips at a higher level, thus building resilient Multicore Systems on Chip (MPSoC) [9], [22]. At the higher layers, where a software stack complements the functionality of the system to form a more programmable flexible hardware (discussed next), one can take advantage of a remarkable body of research and practice to build resilient soft-custom logic [23]-[25]. This can be done by exploiting virtualization techniques to provide software-level containment and replication. More complex systems can be built through networked systems of systems on chip. First instances of networked SoC systems are already emerging in the automotive, aeronautics, and CPS domain.

Across this spectrum, we foresee a need and opportunities to revisit how resilient hardware is built:

- building complex systems of systems and MPSoCs out of smaller COTS;
- taking advantage of the programability and elasticity of modern hardware, e.g., FPGA, GPGPU, to replicate, diversity and adapt; and
- simplifying the design of secure robust systems using smaller hardware *hybrids*—easy to design and verify, as resilient anchors.

II. PROGRAMABILITY, ELASTICITY, PLASTICITY

The genuine immutability properties of hardware components and elements, make them ideal for security hardening and containment, i.e., by making the hard-implemented logic tamper-resistant against both benign and intrusion faults. Despite these facts, there is a continuous wave of relaxing these "rigid" hardware designs through introducing programmable (including reconfigurable and adaptable) fabric [8], [26]. The main reason is to improve hardware flexibility and compatibility, i.e., making them application-agnostic, and to facilitate the daunting design verification process prior to fabrication, hence cutting off fabrication costs thereof. For this, programmable hardware is considered a tradeoff between software logicfully flexible, slow, and mutable-and hard logic-fully rigid, fast, and immutable. We believe that there are promising opportunities to boost the resilience of the programmable platforms against faults and intrusions, although immutability is slightly reduced. To explain these benefits, we consider two classes of programmable hardware:

Soft Custom Logic Fabric (SCLF) : these are commonly known as software-defined devices like PLC, ECU, and SDN



Fig. 1. Resilience forms at the different (networked) hardware layers of Multicore Systems on Chip.

devices [24], [27]–[29]. This hardware is mostly domainspecialized, where computing is done using general-purpose micro-controller or microprocessors, often managed by a full software stack: hypervisors, RTOS/OS, drivers, libraries, and applications. Consequently, these devices exhibit high programability features, analogous to IT computing, although they have specialized roles and use domain specific peripherals, e.g., sensors, actuators, and interfaces.

Hard Custom Logic Fabric (HCLF) : these are hardware chip fabrics, e.g., FPGA [8] and GPGPU [26], composed of arrays of logical components, e.g., gates and multiplexers, that are not "hard etched", i.e., can be reprogrammed as needed. The programming logic in this case is almost entirely implemented in hardware, without the need for a software stack at runtime. Fabric is reprogrammed through soft *IP Cores* [30], [31] (HDL code [32]) or through components (*softcores* or *blocks*) synthesized on the chip as needed. This programability feature is a very interesting tradeoff that retains the speed and security of *Application-Specific Integrated Circuit* (ASIC) chips, while giving the flexibility to support diverse applications and update implementations without the need for costly and slow fabrication.

Although programability, in both classes, opens the door for tampering with the system, and thus injecting surveillance circuits, intrusions and backdoors [3], [4] after fabrication (though slightly compared with software systems), there is a huge opportunity to leverage this programability to improve the resilience of these systems through four main ingredients: replication, diversity, rejuvenation, and adaptation.

A. Replication

Replication is often useful to build resilience against Benign or Byzantine faults. Passive replication [33], [34] allows a failing system to failover into a backup replica. This is a cheap solution that typically requires one passive backup replica. However, recovery is slow, requires reliable detection and is not seemless to the user, even if implemented entirely at transistor level. For example, Razor [35] integrates detection capabilities, originally for timing faults in sequential logic, but also for power instability [36] and side channels [37], and reinjects stored state into the pipeline for re-execution. Albeit functionally transparent, users may observe timing differences and anomalies caused by them. Active replication masks faults through building a *deterministic replicated state machine* [38], composed of replicas of identical functionality, which execute an agreement protocol, e.g. Paxos [39] or PBFT [1]. The number of required replicas is typically $2f + \frac{1}{3}f + 1$ in order to tolerate f faults. Interestingly, several works make use of hardware hybrids as root-of-trust to simplify these protocols to build resilient broadcast and agreement abstractions for embedded real-time systems [40]–[42] (requiring only 2f + 1replicas to tolerate f Byzantine ones).

Replication in SCLF is analogous to software replication at the software layer. While some literary works have studied this in some settings [23]–[25], [43], there are research opportunities in other real-time applications like softwaredefined vehicles, UXVs, Smart Grid, etc. On the other hand, replication in HCLF is today easier than ever. Using an FPGA, it is possible to spawn replicas as soft cores or logical blocks, using off-the-shelf soft IPs. This is a nice hardware feature that gives the flexibility to create hard-replicas quickly and on-demand, using only one fabric, in a similar way to creating virtual machines or containers at software level.

B. Diversity

Resiliency through active replication is, however, only guaranteed as long as the replicas fail independently [1], [38]. The second ingredient, diversity, helps building replicas of the same functionality but with different implementations. The aim is to avoid common-mode benign failures and intrusions.

Since programability in both classes, SCLF and HCLF, open new avenues for multi-vendor implementations and COTS, the likelihood of diversity is higher than the case of monolithic hardware that require deep technology capabilities. An interesting trend that would benefit this model greatly is more standardization for architectures and APIs. For instance, the introduction of the *AutoSAR* [44] standard has greatly enriched the automotive market with multi-vendor implementations of the entire software and hardware stack, which act as a blockboxes of identical functionalities. *CUDA* [26] and *OpenGL* [45] provide standard APIs to implement accelerated parallel computing logic on a GPGPU using COTS implementations. Open source hardware platforms like RISC-V [46] also

standardize the architectures provided by different vendors, and enrich the market with diverse architectures.

Interestingly, FPGAs allow for hardware diversity through modifying the hard-logic through using different implementations or specifications for the softcore/block IP, possibly from different vendors, which is then used to spawn computing cores. It would be interesting to study the case where IP compilers can generate diverse versions of identical softcores to be used on the fly. First approaches towards such a generation of morphable softcores has been investigated in the context of organic computing [47].

C. Rejuvenation

Rejuvenation is the third complementary ingredient to replication and diversity. These latter techniques can only maintain resilience as long as the assumed number of failing replicas fis fixed. This assumption is unfortunately hard due to benign faults and malicious behaviours. The first is related to aging, which manifest in software [48] as memory leakage, failure to release resources and locks, failure to garbage collect, data corruption, etc. Surprisingly, aging occurs also in hardware, due to the deterioration of hardware material under overuse and overheating, etc. The second reason is recently getting more attention with the increasing attempts of Advanced Persistent Attacks (APT)-where a big deal of time and effort is usually put to identify vulnerabilities and exploit them. While this might be clear at the software level, there are continuous concerns about hardware backdoors and timed Trojans. Indeed, this is behind the recent agendas of acquiring chip sovereignty or split manufacturing in many countries [49], [50].

SCLF reprogramability can greatly benefit from the huge body of research on software rejuvenation, that is proven to mitigate failures. This would even be more effective when rejuvenation is simultaneous with diversity, which allows the rejuvenation to a different implementation with identical functionally, in consequence, reducing the success rate of APTs. Using FPGAs, rejuvenation can also happen at hardware level in HCLF [51]. An FPGA allows restarting or spawning new soft cores and logical blocks at runtime—avoiding slow device restarts. In fact, one can partially rejuvenate some soft cores while others continue to run. FPGAs allow for even smarter techniques, e.g., to rejuvenate to diverse softcore variants that are loaded in different FPGA spatial locations, which can avoid potential backdoors in the FPGA grid fabric.

D. Adaptation

Yet, another way to withstand a varying number of faults f is to adapt the resilient system accordingly. Among the adaptation forms are scaling out/in the system when f may change, e.g., upon experiencing more threats, or switching to a backup protocol that is more adequate to the current conditions [23], [52]–[54] (considering safety, liveness, performance, etc.). This would require research on the aforementioned adaptation mechanisms and, importantly, on severity detectors that can trigger adaptation actions once needed. As we discussed above, both SCLF (e.g., virtualization) and HCLF (e.g., FPGAs)

provide tempo-spatial elasticity, which allows changing the number of replicas and their locations on the fabric as needed. It will be interesting to study these research questions from scratch or validating the feasibility of existing ones (developed in the software realm).

E. Resilient Reconfiguration

It should be evident that reconfiguration must be resilient to faults and attacks, irrespective of the kind of adjustment performed (i.e., diverse rejuvenation, relocation, or adaptation). This holds for both reconfiguration of an FPGA grid fabric as well as multi-chip FPGAs-where the individual FPGA chiplets are the unit of reconfiguration. We shall focus here exclusively on internal, partial and dynamic reconfiguration, since the reliance on external complex and non-configurable modules (e.g., CPUs) would induce a weak spot in the system, which could contaminate its resilience or introduce downtimes. Nevertheless, dependencies on external hybrids that are simple, and thus easy to verify, are allowed if they simplify the design. Internal, partial and dynamic mean respectively that reconfiguration (i) is driven from within the FPGA, e.g., by an HCLF or softcore defining the configuration bitstream to be loaded into a reconfigurable region (or frame) through interfaces like internal configuration access ports, (ii) it is bound to the reconfigured area and elements therein, and (iii) it happens while other parts of the FPGA continue to execute.

Optimizing the mapping of blocks to the FPGA grid fabric and integrating the configured block with the remaining blocks remain sufficiently complex tasks to be executed by a software-level operating-system kernel. Disabling and enabling configured circuits and frames constitute the critical operations, which leaves writing the configuration memory and validating that a correct bitstream is written as tasks that can be executed by the responsible kernel or possibly even kernel replicas. Provided sufficient access controls are in place at the internal configuration access ports, the actual configuration of a frame can even be delegated to its current user. However, as shown in Gouveia et al. [55], privilege change must remain a trusted operation executed *consensually* and enforced by a trusted-trustworthy component. This leads to the more general question of architectural hybridization, which we address next.

III. ARCHITECTURAL HYBRIDIZATION

Differentiating how the individual hard- and software components of an MPSoC architecture can fail, architectural *hybridization* aims at benefiting from small easy-to-verify and therefore more trustworthy components, called *hybrids*. The goal is to enable, simplify or improve the performance of the overall system, by serving as trust anchors for these properties. These could be components (registers, memory, trusted execution environments or networks) such as USIG, A2M, TrInc, SGX and others, used in hybrid BFT-SMR protocols [41], [56]–[65].

Realizing hybridization poses a challenge dual to the question whether SCLF or HCLF leads to more reliable systemson-a-chip. For software-only hybrids, we used to equate simplicity (measured for example in lines-of-code required to realize a certain functionality) with a low likelihood of failure and ease of verification. However, at hardware level, this equation is not as obvious, even if we consider lines-of-VHDL or another hardware description language.

We illustrate this using the USIG from the MinBFT protocol by Veronese et al. [41] as example. USIG is essentially a sequential circuit, which is driven by the counter register and a few additional registers, which provide as constants the secret key for the HMAC and the ID of the replica. The lowest complexity version of such a circuit will use normal registers. But then any bitflip in the counter will have catastrophic effects on the consensus problem at hand since it is reflected unchanged in the computed HMAC and USIG output. ECC-registers on the other hand add extra bits and the logic required for correction, which both increase the complexity of the circuit at the benefit of tolerating a certain number of bitflips. We also see the converse effect when the required complexity of producing a special purpose circuit for a given functionality exceeds the complexity of a simple core that is able to fetch, decode and execute software. Once the inherent complexity of such a functionality exceeds this bound, software implementations become preferable and hybridization amounts to providing such an isolated core.

The objective of hardware-level hybridization is therefore to remain in this middle-ground. Hardware hybrids, protected by ECC and other accidental- and malicious-fault countermeasures, provide the desired functionality. This can then be extended into the realm of software hybrids that are possibly executed in a replicated manner and that vote to perform critical operations [55].

IV. CONCLUSIONS AND CALL TO ACTION

We emphasized that hardware architectures, and in particular multi- and manycore systems-on-a-chip are not the robust, dependable and reliable computing units we would like to have. We have subsequently started to replicate entire systems, which has ultimately lead to the huge body of knowledge on implementing resilient distributed systems. However, as we have seen, the continuing miniaturization and integration of processing elements into a single MPSoC, makes full system resilience increasingly costly, in particular when a single system already provides all the processing power that future critical applications need. We have shown how reconfiguration, rejuvenation and adaptation already allow the hardware to repair itself, to recover from faults and retain the resources classical resilience mechanisms need, when applied entirely on chip. Hybridization rooted in exactly the right-complexity circuits and applied to construct incrementally more complex dependable systems will produce the next generation flexible, morphable and highly trustable systems mission-critical systems will need. We therefore appeal for more research to study the resilience of hardware-based systems, systems of systems, and MPSoCs at different layers and cutting vertically across layers, probably through validating the techniques developed in the software Systems and Dependability areas.

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