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OFDM MODULATOR IMPLEMENTATION IN FPGA FOR INDUSTRY 4.0 NETWORKS

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ABSTRACT

Industry 4.0 demands new paradigms in modern production factories worldwide, where the supporting communication infrastructure is critical. Higher transmission capacities with low-latency constraints are such key use cases for smart factories. Previous research outlines the feasibility of using orthogonal frequency division multiplexing (OFDM) modulation as a candidate in the next-generation industrial networks. The modeling and subsequent implementation of these mechanisms in FPGA facilitate the path toward future practical developments of functional communications systems. This paper investigates the hardware design in FPGA for transmissions and the modeling of the wired channel as a twisted copper pair cable using the System Generator simulator. The OFDM modulator is implemented, and the channel model follows the KHM parameters. The resulting simulation results evidence the feasibility of high-speed digital data transmission.

INDEX TERMS: Industry 4.0, OFDM, KHM model, twisted-copper-pair cable, System Generator.

IMPLEMENTACIÓN DE MODULADOR OFDM EN FPGA PARA REDES DE INDUSTRIA 4.0

RESUMEN

La Industria 4.0 exige nuevos paradigmas en las fábricas de producción modernas de todo el mundo, donde la infraestructura de comunicación de soporte desempeña un papel fundamental. Las capacidades de transmisión más altas con restricciones de baja latencia son casos de uso clave para las fábricas inteligentes. Investigaciones anteriores describen la viabilidad del uso de la modulación de multiplexación por división de frecuencia ortogonal (OFDM) como candidato en las redes industriales de próxima generación. El modelado y posterior implementación de estos mecanismos en FPGA facilitan el camino hacia futuros desarrollos prácticos de sistemas de comunicaciones funcionales. Este artículo investiga el diseño de hardware en FPGA para transmisiones y el modelado del canal cableado como un cable de par trenzado utilizando el simulador System Generator. El modulador OFDM es implementado y el modelo de canal sigue los parámetros KHM. La evidencia de simulación resultante da como resultado la viabilidad de la transmisión de datos digitales de alta velocidad.

PALABRAS CLAVES: Industria 4.0, OFDM, FPGA, par de cobre trenzado, System Generator.

1. INTRODUCTION

Modern factories are today under development as pledging to the paradigm of Industry 4.0 [1]. In this regard, Cuban policymakers are today assessing a program where the confluence of various technological and industrial sectors are interplaying: Biotechnology, electronics, and software [2]. Its implementation is highly dependent on the conception of Cyber-Physical Production Systems (CPS), where automated smart machines support factory workers to achieve improved production capacities [3, 4]. Following this trend, this article aims to elaborate on the conception of

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transceivers for improved communication rates in fieldbuses. Designing more transmission capacity in fieldbuses directs critical as the data volume dramatically increases with the number of interconnected sensors and actuators in factories.

One of the main challenges in this field is the massive integration of IoT devices that exchange multimedia information [5]. The resulting high amount of data happens prohibitive to handle in typical industry networks, where deployed fieldbuses are limited to a maximum of 12 Mbps (PROFIBUS) [6]. Such protocols implement communication systems that only use short messages among nodes with low computational capacity, aiming to guarantee timing constraints. Furthermore, ethernet-based solutions offer an alternative to data forwarding capabilities, supporting complex streaming services [7]. However, this solution is costly for industries with large physical spaces and the need to interconnect large numbers of distant working places. Specifically, the costs of the equipment associated with the Ethernet infrastructure, such as switches, routers, and PCs, increase with the distance and the total of nodes to interconnect.

Therefore, the currently available techniques have a high computational and commercial cost, in addition to not guaranteeing the transmission rates demanded by Industry 4.0 applications. In this regard, this work features in the System Generator simulator a transmission scheme for Orthogonal Frequency Division Multiplexing (OFDM) modulation over twisted-copper-pair; as the physical medium of standard fieldbuses. We conceive the OFDM modulator in Simulink/Matlab, to be later implemented in FPGA as described in Section 2. The resulting implementation allows conducting measurement campaigns with real hardware to illustrate the promising capabilities of this framework. The modulator is designed with HDL blocks optimized for FPGAs from Xilinx [8]. A detailed description is given in Section 3. The main results illustrate the feasibility of this testbed design in Section 4

2. OFDM MODULATOR AND CHANNELS MODELS

We implement the OFDM modulator and the communication channel model in System Generator according to the scheme in Fig. 1. Using this general block diagram, we can determine the signal attenuation and noise level at the receiver node. We placed scopes at the channel output to display the received waveform.

Figure 1: Block diagram of the OFDM modulator and the channel developed in System Generator.

OFDM as a multicarrier modulation multiplexes serial input data into several parallel streams and transmits them over independent subcarriers [9]. These subcarriers can be individually modulated and manipulated, allowing for their optimization with respect to the channel. The ability of multicarrier modulation to tailor its transmission parameters across the different subcarriers is especially useful when dealing with frequency-selective fading channel environments.

OFDM Modulator

The OFDM modulator mainly consists of two blocks; the QAM modulator and the Inverse-Fast-Fourier Transform (IFFT). The M-QAM block packs on each different symbol a total of $b = \log_2 M$ bits from the source. Next, the IFFT block allocates the input QAM symbols into each different orthogonal subcarrier from a total of N, as depicted in Fig. 2 [9]. Finally, the OFDM signal is derived after superposing all the subcarriers as indicated in

$$x(t) = \sum_{n=0}^{N-1} D_n e^{j2\pi \frac{kn}{N}}, \quad (1)$$

where D_n is the complex QAM symbol.

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The resulting OFDM symbol is transmitted through the channel and will carry a total of $N \log_2 M$ bits. The OFDM symbol rate depends on the binary stream received from the QAM modulator as

$$R_{s\,OFDM} = \frac{R_{s\,QAM}}{N}, \quad (2)$$

where $R_{s\,QAM}$ is the QAM symbol rate and N is the total of subcarriers. Besides, considering the orthogonality of the OFDM subcarriers, the following equation also holds

$$R_{s\,OFDM} = \Delta f, \quad (3)$$

where Δf is the subcarrier spacing. Similarly, the symbol rate from the QAM block will be related to the source bit rate R_b through

$$R_{s\,QAM} = R_b / \log_2 M. \quad (4)$$

Using the above relations, the achievable bit rate is

$$R_b = \Delta f \cdot N \cdot \log_2 M. \quad (5)$$

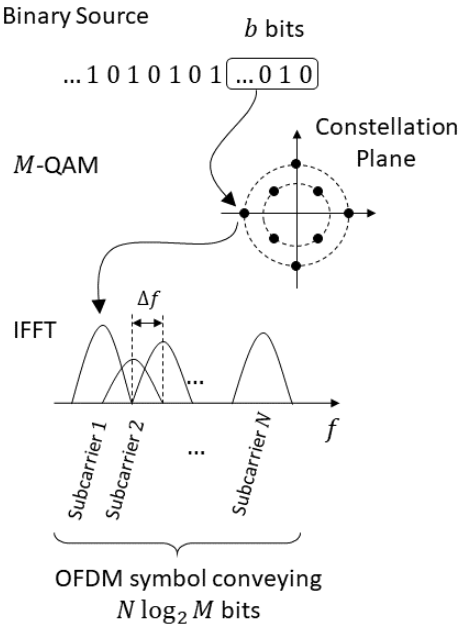

Figure 2: Functional description of the OFDM modulation.

To illustrate, we implement the OFDM modulator based on 3GPP 36.212 standard recommendations [10], using a 16-QAM modulation ($M = 4$) and a IFFT size $N = 2048$. Selecting the subcarrier spacing as $\Delta f = 6.104$ kHz, the achievable bit rate will be $R_b \approx 50$ Mbits/s, which results in a system capable of reaching the speeds of Ethernet connections [11].

Communication channel

Various cables are reported for data transmission in industrial networks [12]. Twisted copper pair is widespread in Industrial Ethernet applications supporting maximum speeds [12]. This variant has a characteristic impedance of 100 Ω with a variance of 5 Ω, measured at 100 MHz, and an attenuation of 24 dB per 100 meters. Other cable types described, such as MegaLine® D1-20 SF/U HV, CAT 5, heavy-duty, MegaLine® F6-70 S/F HV flex CAT 7, have similar electrical characteristics. Still, the cable's complexity, weight, and cost are higher than the simple two-wire variant. Others, such as the products offered by FOUNDATION™ Fieldbus, provide a similar impedance characteristic, e.g. (100 Ω), with an attenuation of 3 dB/km [12] and bandwidths in the order of the kilohertz.

In the industrial scenario, the wired channel might be modeled through various mathematical models for twisted-pair cables [13 - 15]. Operating at relatively high frequencies, most parametric cable models reported in the literature were designed for the very high-speed digital subscriber line (VDSL) frequencies with a maximum bandwidth of 30 MHz [13]. For instance, the TNO/EAB model incorporates an extra parameter for improving accuracy compared to the TNO model presented in [14]. Furthermore, the well-known BTO model was modified in [13] with new parameter values and targeting frequencies up to hundreds of megahertz.

Extending [15], the study in [13] reports a simple and causal model for the characteristic impedance Z_0, as referred to the KHM model. Together with the so-called KM1 model from [13], the new Z_0 model composes the KHM model, which supports multiple segments and frequencies up to hundreds of megahertz. This solution has few parameters, is causal, and introduces a closed-form expression allowing to fit channel measurements. This model provides two closed-form expressions for the characteristic impedance Z_0 and channel propagation constant γ through five parameters $(k_1, k_2, k_3, h_1, h_2)$.

The mathematical development of KHM model is detailed in [13], where the least-square (LS) method determines the h parameter, typically done after measuring the S-parameters using a vector network analyzer [13]. In our work, we follow the values obtained in [13], as shown in Table 1, over a frequency range of 100 kHz to 200 MHz.

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Table 1: Parameters of the KHM model for a CAT 5 cable from the manufacturer.

Parameter	Value
k_1	$2.07 \cdot 10^{-3}$
k_2	$2.39281 \cdot 10^{-8}$
k_3	$2.94153 \cdot 10^{-5}$
h_1	$1.012393 \cdot 10^{2}$
h_2	$3.2608 \cdot 10^{3}$

Having these parameters, the channel propagation constant and the characteristic impedance are [13]

$$\begin{aligned} \Re\{\gamma\} &= k_1\sqrt{f} + k_2 f, \\ \Im\{\gamma\} &= k_1\sqrt{f} - k_2\frac{2}{\pi} f \cdot \ln f \cdot k_3 \cdot f, \\ \Re\{Z_0\} &= h_1 + h_2\frac{1}{\sqrt{f}}, \\ \Im\{Z_0\} &= -h_2\frac{1}{\sqrt{f}}. \end{aligned} \tag{6}$$

Using the relations in Eq. (6) and the parameters in Table 1, we characterize the cable through its impedance matrix, denoted as Z. To compute the parameters of the Z matrix, we first calculate the T matrix of the cable according to [11]. Then we use the T to Z parameter conversion using the equations reported in [16]. In this work, we use this model of the twisted-pair copper cable to simulate the transmission channel for the OFDM waveforms.

3. IMPLEMENTING THE SYSTEM WITH XILINX BLOCKS

The blocks in Simulink are synthesized and implemented to produce the FPGA configuration bitstream automatically. We follow the block diagram in Fig. 1, to separately implement each component as described in the following subsections. The proposed architecture seeks to create a digital hardware with low resource consumption and latency. Table 2 summarizes the main parameters used for the modulator.

Table 2: Parameters of the OFDM modulator implemented in the System Generator.

Parameter	Value
Bit rate R_b	50 Mbit/s
RF bandwidth	30 MHz
Target clock	100 MHz
Target FPGA	XC7K325TFFG676-1
QAM order (M)	16
Number of subcarriers (N)	2048
Subcarrier spacing (Δf)	6.104 kHz
Cyclic Prefix Length	512 samples

The target clock and target FPGA are set in System Generator to synthetize the intellectual property (IP) module, to be later encapsulated in the FPGA. The number of subcarriers defines the IFFT size and directly concerns the number of implementation resources. Besides, the subcarrier spacing sets the minimum operating frequency of the digital-to-analog converter (DAC). The cyclic prefix length sets the number of samples inserted at the beginning of each OFDM symbol. The following subsections provide more details about these blocks.

Data source for the OFDM modulator

This subsystem comprises two System Generator blocks (see Fig. 3): an up-counter and a ROM memory. The purpose of the counter is to generate the memory addresses for the ROM block. The ROM memory stores the 4-bits packets to be sent to the modulator. These packets correspond to the number of bits per symbol the 16-QAM module supports. The binary sequence is randomly generated from the integer range 0 to 15 using the Matlab randi function.

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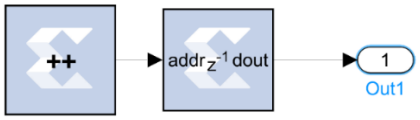

Figure 3: Integer data generator.

QAM modulator

The QAM modulator block directly produces the symbols as depicted in Fig. 2. The implemented scheme is illustrated in Fig. 4 with the I (in-phase) and Q (quadrature) channels. The Slice block is used as a selector control for the multiplexer, which outputs the proper QAM symbol. The upper part of these bits is used to select the in-phase component, while the lower part is for the quadrature one.

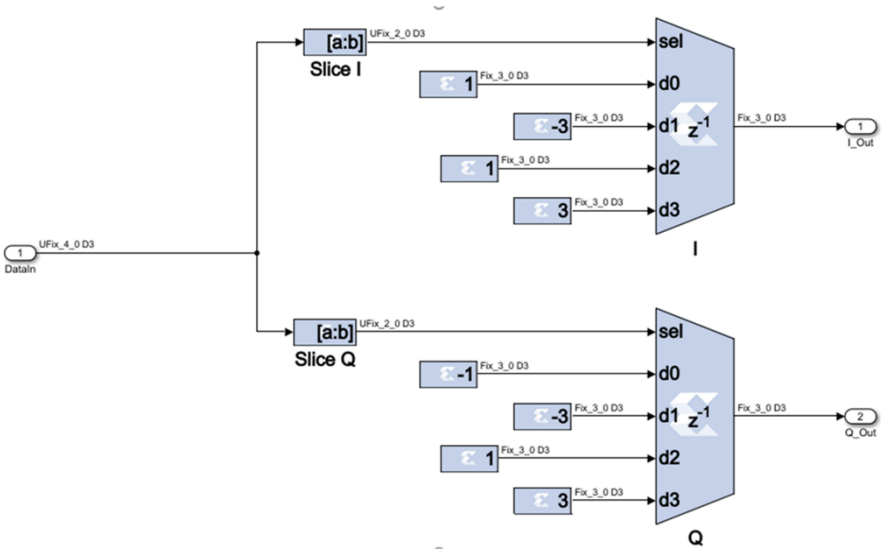

Figure 4: 16-QAM modulator.

The constants correspond to the reference constellation illustrated in Fig. 5. The summary of parameters to implement this block are the modulation order $M = 16$, a Gray coding for bit-to-symbol assignment, a minimum distance of 2 as the normalization method and a zero Phase offset.

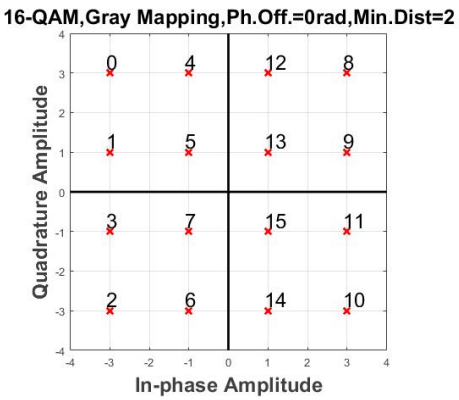

Figure 5: 16-QAM constellation.

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OFDM modulator

Part (a) of Fig. 6 shows the design for the OFDM modulator. This comprises the OFDM Symbol, IFFT Data Preprocessing, IFFT_Config, and IFFT subsystems. The OFDMSymbol subsystem in part (b) performs the assignment of the QAM symbols to the subcarriers or IFFT bins. This is conceived by multiplexing in time QAM symbols stream with null symbols.

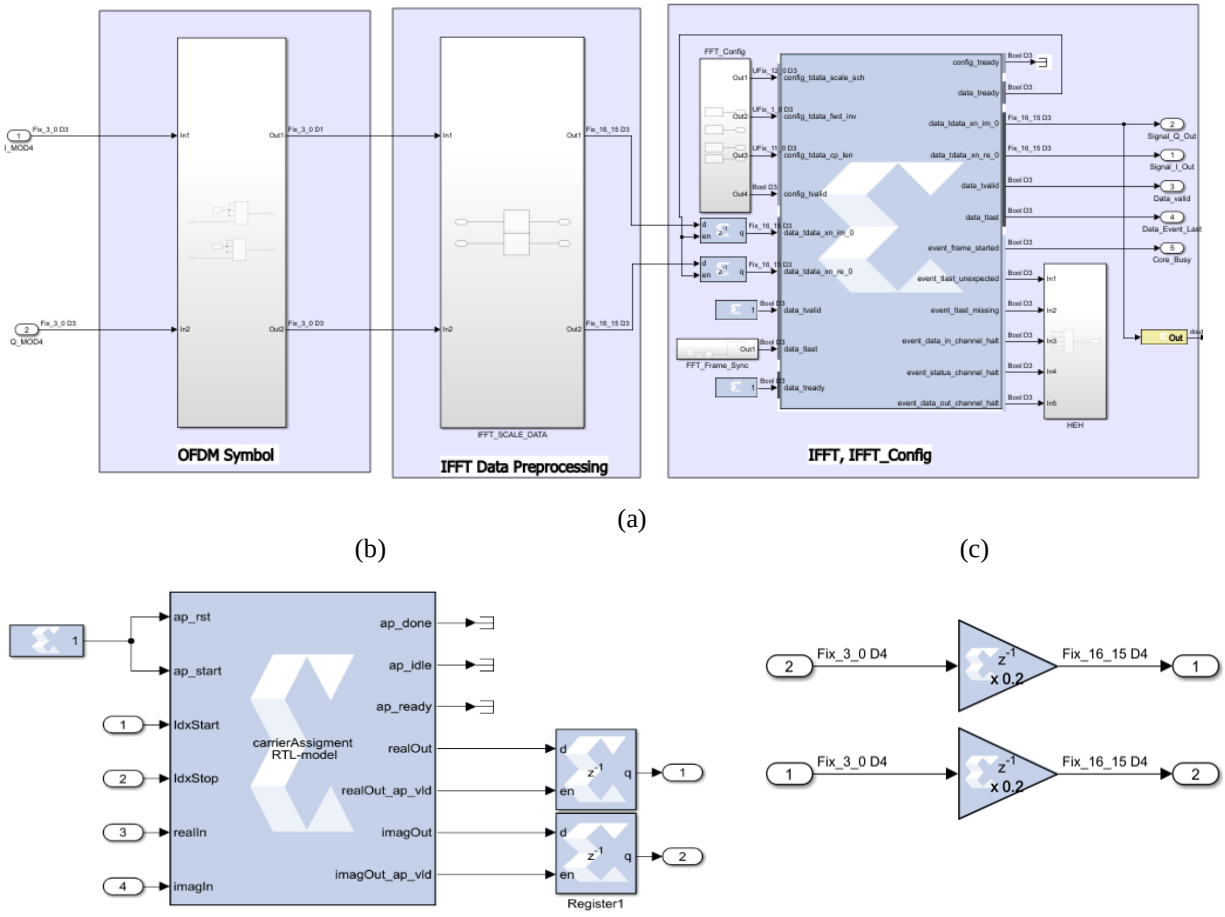

Figure 6: (a) OFDM Modulator implemented in System Generator, (b) OFDM Symbol subsystem and (c) IFFT Data Preprocessing subsystem.

The multiplexing is performed by an algorithm [17] that consecutively interleaves the QAM symbols with zeros. The first step is to store this stream of symbols in a temporary memory with size corresponding to the number of assigned subcarriers. Then, according to the variables IdxStart and IdxStop, the QAM symbols are consecutively assigned to the N subcarriers, establishing a set of null subcarriers and QAM-modulated subcarriers, thus shaping the spectrum of the transmitted signal. We implemented this function by means of a Vitis HLS block, which allows us to describe the carrier mapping algorithm in C programming language and to insert the code in System Generator.

The IFFT Data preprocessing block performs a data type conversion and symbol amplitude scaling. Part (c) of Fig. 6 shows that the IFFT requires a fix16_15 data type [18], i.e. one bit used for the sign and fifteen to describe the decimal part of the value. Finally, the IFFT subsystem converts the signal in the frequency domain to the time domain. This block also inserts the cyclic prefix, a parameter that must be indicated from the IFFT_Config block. The cyclic prefix is the process of adding the final samples of the previous OFDM symbol to the beginning of the current symbol. Following the standards such as LTE, we use a preamble length of 512 samples (called a long prefix) [10].

The RF toolbox was used for modeling the communications channel in the Simulink environment. Fig. 7 shows the connections between the channel model (Z) and the interface ports. The input data is taken as a voltage plus noise source with a 150 Ω impedance, corresponding to DACs from Analog Devices [19].

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Figure 7: Interconnection of the RF blocks.

The Z block simulates the twisted-copper pair cable, which is a passive network dependent on the parameters of the Z matrix, which elements are computed as described in Section 2. For a cable length of 300 meters and a frequency of 100 MHz, we obtained the following results

$$Z = \begin{bmatrix} 0.0157 - j0.32626 & 0.1634 - j0.1138 \\ 0.1634 - j0.1138 & 0.010157 - j0.32626 \end{bmatrix}. \quad (7)$$

4. RESULTS

Results were obtained using the parameters in Table 1 for the cable model, according to the frequency range of 100 kHz to 200 MHz. As for the modulator parameters, we used those in Table 2. We illustrate different results for the channel model, the received OFDM waveform, latency, and the resource consumption of the implemented system.

Figure 8 shows the modeling of the characteristic impedance Z_0 with frequency. The resulting values for Z_0 are located around 102 Ω for frequencies ranging from 20 MHz to 200 MHz. In order to obtain the attenuation of the twisted pair copper cable, the model was excited with an OFDM signal of equal spectral power density (80 dBm/Hz) for all the subcarriers. The attenuation was directly determined by comparing the power ratio between the output and the input.

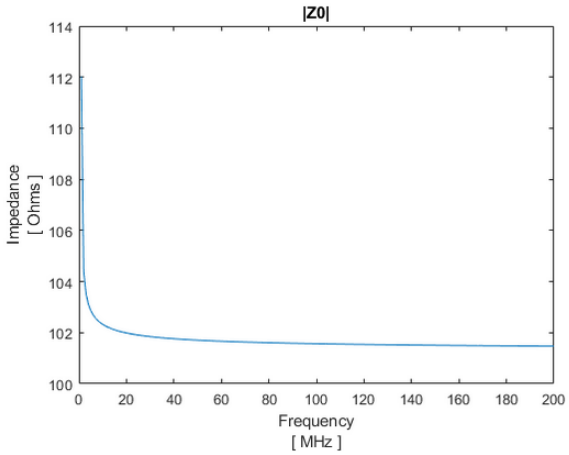

Figure 8: Characteristic impedance of the twist-pair cable according to KHM model.

The spectrum of the modulator output and the received signal are shown in Fig. 9. Both signals were obtained from the OFDM modulator implemented through the System Generator blocks. The RF band of the OFDM signals has a center frequency of 100 MHz with a 30 MHz bandwidth. The noise floor level has a power spectral density of -170 dBm/Hz for a signal-to-noise ratio (SNR) of 20 dB. Thus, the resulting power spectral density of the useful signal is equal to -150 dBm/Hz. In real scenarios, these values may change and the proper operation will depend largely on the characteristics of the receiver. Directly comparing the amplitude levels at the modulator's output and at the channel model's output, the resulting attenuation introduced by the twisted copper pair cable is -65 dB.

Another factor we considered in the design was the latency of the modulator. This parameter defines the time it takes for the OFDM modulator to transmit an RF signal once it has digital data available. Latency measured using Simulink time scope was 5.344 µs. This parameter depends on the settings for the blocks included in the design.

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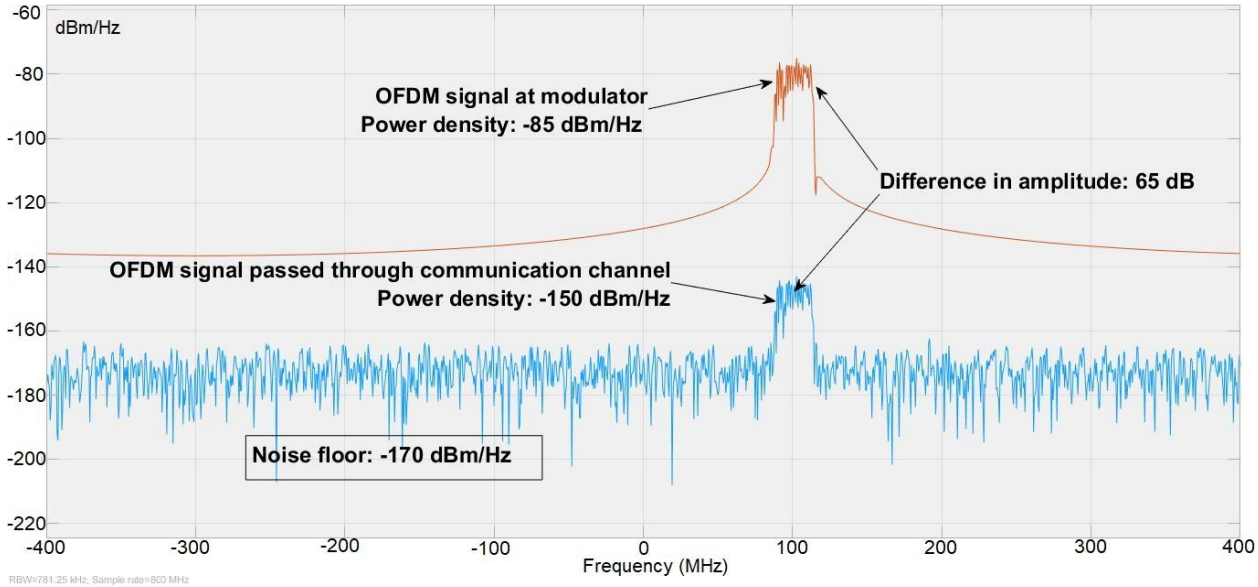

Figure 9: Spectrum of signals at the modulator and the output of the channel.

We compiled the OFDM modulator design for the Kintex7 FPGA family using the Xilinx tools. When compiled, we determined the number of resources needed, also verifying its feasibility for other FPGA platforms. After executing the synthesis and implementation of the proposed hardware, the number of resources needed for the OFDM modulator is very low, as shown in Table 3.

Table 3: Hardware resources reported by Vivado tool.

Resource	Utilization	Available	Utilization %
LUT	5026	203800	2.47
LUTRAM	1921	64000	3.00
FF	9007	407600	2.21
BRAM	18.5	445	4.16
DSP	98	840	11.67

The FPGA configuration file was generated using the default synthesis and implementation strategies to validate the results. Finally, the time waveform of the OFDM modulator was obtained through the integrated logic analyzer interface with Vivado. Figure 10 shows a time window of 202 ns duration for a segment of the OFDM signal, captured at the instant a new OFDM symbol begins.

5. CONCLUSIONS

This paper evidences a low-complex design for an OFDM transmitter aiming to improve the communication capacities in industry 4.0 networks. The model we presented features a functional implementation in hardware and includes realistic values for the channel model and noise levels. As the first step for a transceiver testbed, this model demonstrates the suitability of OFDM signals for communications in Industry 4.0 environments. As implemented in Simulink, the OFDM transmitter results in affordable digital hardware conceived as a low-cost SDR platform solution. The resulting implementation allows measurement campaigns with real hardware to illustrate the promising capabilities of this framework. In the future, we plan to design the OFDM receiver and build an on-site test bed to conduct measurement campaigns.

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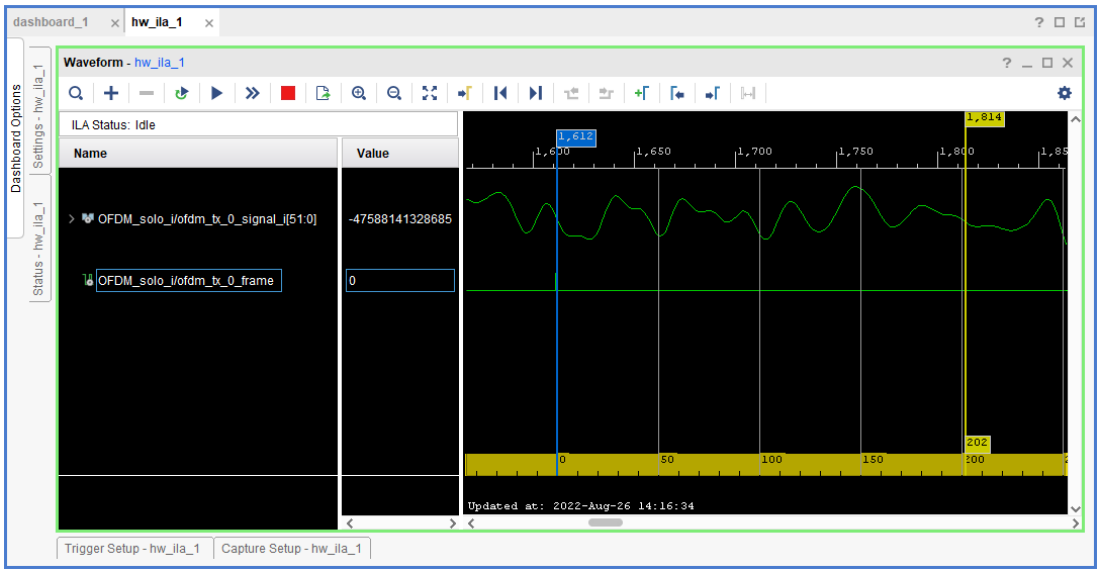

Figure 10: Time representation of a segment of the OFDM signal.

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CONFLICT OF INTEREST

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- **Fernando Hernandez Vives:** Development of the article, programming of the method in the development tools and obtaining results.
- **Camilo Guillen Soriano:** Writing, review and discussion of results.
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