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INTERFACE OPEN-CIRCUIT VOLTAGE DEFICIT IN CU(IN,GA)S$_2$ SOLAR CELL: CHARACTERIZATION, SIMULATION AND MITIGATION

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“On the other side of a storm is the strength that comes from having navigated through it. Raise your sail and begin.” - Gregory S. Williams.

Abstract

Current commercial photovoltaic technologies are close to their practical limits, and enhancing their power conversion efficiency (PCE) requires a paradigm shift to tandem approaches. Tandem solar cells can exceed the single junction practical and thermodynamic limits. The desired top cell bandgap to enhance PCE of current photovoltaic technologies is ~1.6-1.7 eV. The bandgap tunability from 1.5 eV to 2.5 eV positions $Cu(In,Ga)S_2$ as a prime top cell candidate for next-generation low-cost tandem cells. However, they are limited by a low external open-circuit voltage ($V_{OC,ex}$). In this thesis, we have studied the interface recombination and found it to cause a difference between $V_{OC,ex}$ and internal open-circuit voltage ($V_{OC,in}$) in $Cu(In,Ga)S_2$ solar cell. We have introduced a quantifiable metric that has not been used before for $Cu(In,Ga)S_2$, to evaluate V_{OC} disparity in terms of "interface V_{OC} deficit" defined as ($V_{OC,in} – V_{OC,ex}$). The temperature-dependent current-voltage measurement allows to investigate the activation energy (E_a) of the dominating recombination path in the device, uncovering the cause of interface V_{OC} deficit in Cu-poor and Cu-rich $Cu(In,Ga)S_2$ devices. We find that negative conduction band offset (CBO) at the absorber/buffer interface results in interface V_{OC} deficit in Cu-poor $Cu(In,Ga)S_2$ devices.

Although the interface V_{OC} deficit can be reduced by replacing the buffer for favorable band alignment at the absorber/buffer interface, a substantial deficiency still exists. We observe that the CBO not only at the absorber/buffer interface but also at the buffer/i-layer interface leads to an interface V_{OC} deficit in devices. This, in general, is not an issue in $Cu(In,Ga)Se_2$ devices. By optimizing buffer and i-layer, we mitigate and overcome buffer/i-layer losses to get Cu-poor $Cu(In,Ga)S_2$ devices with consistently low interface V_{OC} deficit. As a result, an in-house PCE of 15.1 % is achieved together with an externally certified PCE of 14 %. This is, by far, the best $Cu(In,Ga)S_2$ device performance except for the record PCE device.

In contrast, the interface V_{OC} deficit and the interface recombination persists in Cu-rich $Cu(In,Ga)S_2$ devices and is not resolved by alternative buffers. To identify the possible origin of the interface V_{OC} deficit, we characterize two sister systems $CuInS_2$ and $CuInSe_2$, which offer reduced complexity due to Ga exclusion. The Cu-rich devices of these systems are also known to suffer from interface recombination, and for $CuInSe_2$, it has been linked to the "200 meV" defect. However, the underlying mechanism of how this defect leads to interface recombination remains unknown. Through results obtained from photoelectron spectroscopic measurements, we exclude

the possibility of two commonly evoked causes of interface recombination: negative CBO and Fermi-level pinning.

Sulfur-based post-deposition treatments on KCN etched Cu-rich $CuInS_2$ absorbers reveal near interface defects as a possible alternative cause of interface V_{OC} deficit. The treatment increases the $V_{OC,ex}$, which originates from improved E_a and interface V_{OC} deficit in treated devices. The capacitance transient measurements further reveal that slow metastable defects are present in the untreated sample. The treated samples show that the slow transient is suppressed, suggesting the passivation of slow metastable defects. The treatment adapted to Cu-rich $CuInSe_2$ displays a reduction in the deep defect signature in admittance spectra, which explains the observed improvement in interface V_{OC} deficit. This indicates that the defects near the absorber/buffer interface, acting as non-radiative recombination centers, as the source of interface V_{OC} deficit.

Finally, to understand how the defect leads to interface recombination, a new model based on near interface defects is offered using the holistic analysis and evaluation of the defect characteristics. We can reproduce an interface V_{OC} deficit with all the signatures of an interface recombination-dominated device using numerical simulations. This model provides a solution for the consideration of interface recombination by defects distributed in a thin layer within the bulk absorber, an explanation beyond classical models. The near interface defect model finally explains why Cu-rich chalcopyrite solar cells are limited in their $V_{OC,ex}$ despite a good $V_{OC,in}$, which was not discovered before. The model thus forms a new third explanation for interface recombination signature in devices and is applicable to any device with highly recombinative defects near the interface.

Chapter 1

Introduction

1.1 Rise of a “New King”

The global pandemic caused by ‘SARS-CoV-2’ has brought major disruption in the global economy in the year 2020. Many sectors are facing a major drop in demand as a direct consequence, energy being one of them. However, during the pandemic year 2020, renewable energy was the only energy source to grow and accelerate.[1] This was one of the rare positive consequences of the pandemic. Countries globally are trying to emerge from this pandemic and boost their economies through various measures and strategies. An excellent opportunity presents itself to achieve a net-zero carbon emission target by 2050.[2, 3] New policies aiming at sustainable development scenarios [1] are needed to limit the global temperature rise to below 1.5 °C by the year 2100. For this, the massive packages being implanted to boost the economic recovery must include a significant acceleration towards more efficient systems for cleaner energy.

Renewable energy sources are set to meet 80 % of global electricity demand by 2030, with solar photovoltaic (PV) being crowned “New King.”[1] The global PV module production is soaring higher and higher in recent years, and in 2019 only it reached 133 GWp.[4] This contribution comes majorly from silicon (Si) PV that dominates market shares, followed by copper indium gallium diselenide ($Cu(In,Ga)Se_2$ or CIGSe) and cadmium telluride (CdTe) thin-film PV.[4] It doesn’t stop here; the signs for PV are looking very promising, with the International Energy Agency world energy outlook 2020 report predicting a 13 % average growth per year till 2030.[1] Predictions like these have repeatedly underestimated solar energy potential,[5] and PV might grow at an even higher rate. The cost of PV systems continues to fall, majorly through new advancements and improvement in system efficiencies resulting from scientific and technical progress. However, to compete and even dominate (in the near future) non-renewable energy sources, the Levelized Cost of Electricity (LCOE) for these systems must decrease further. Already, in 2018 the LCOE for utility-scale PV in Germany was around ~7 € cent/kWh, the lowest among all energy resources.[6]

1.2 Multi-junction solar cell: The more, the merrier

Today, 50 – 60 % of the total cost of the PV system is due to contribution from the ‘Balance of System’, which encompasses components such as inverter, inter-connection materials, construction, mounting, maintenance charges, and land cost.[7] The balance of system thus dominates the LCOE. The LCOE is calculated as the ratio of the PV system's production, assembly, and maintenance cost to the sum of energy produced over the lifetime. A direct way of lowering the LCOE is to raise the efficiency of the cells in the PV system without incurring significant additional costs. At present, the PV market is dominated by systems that have almost reached their practical efficiencies limits with Si at 26.7 %,[8] CIGSe at 23.3 %, [9] CdTe at (22.1 %).[10] Further efficiency enhancements require the employment of novel third-generation PV concepts. These concepts are based on reducing non-absorption and thermalization losses in a solar cell.[11] Multijunction or tandem solar cell is one concept that has taken the efficiencies of these single-junction solar cells beyond their current value (in a two junction configuration).[12, 13]

A multijunction solar cell consists of two or more solar cells stacked on top of each other. The partner solar cells of certain bandgap are chosen in a way to get the optimum performance from the device by minimizing the thermalization and non-absorption losses. Fig. 1 depicts the two losses and their minimization through the utilization of multi-junction solar cell. Among the available technologies, Si and CIGSe are the two preferable candidates that will benefit most in a multijunction solar cell when combined with a solar cell of high bandgap ~1.6-1.7 eV.[14] The two technologies have already been teamed up with perovskite solar cells of the suitable band gap. The resulting multijunction solar cells have surpassed their single-junction counterparts by reaching a power conversion efficiency of ~29 % for Si-perovskite tandem solar cell,[12] and above 24 % for CIGSe-perovskite tandem solar cell.[13] Although, the long-term stability of these solar cells remains a bottleneck, as the perovskite solar cell suffers from stability issues.[15] While researchers continue to work towards conquering this challenge, it is imperative to discover and investigate other worthy alternates.

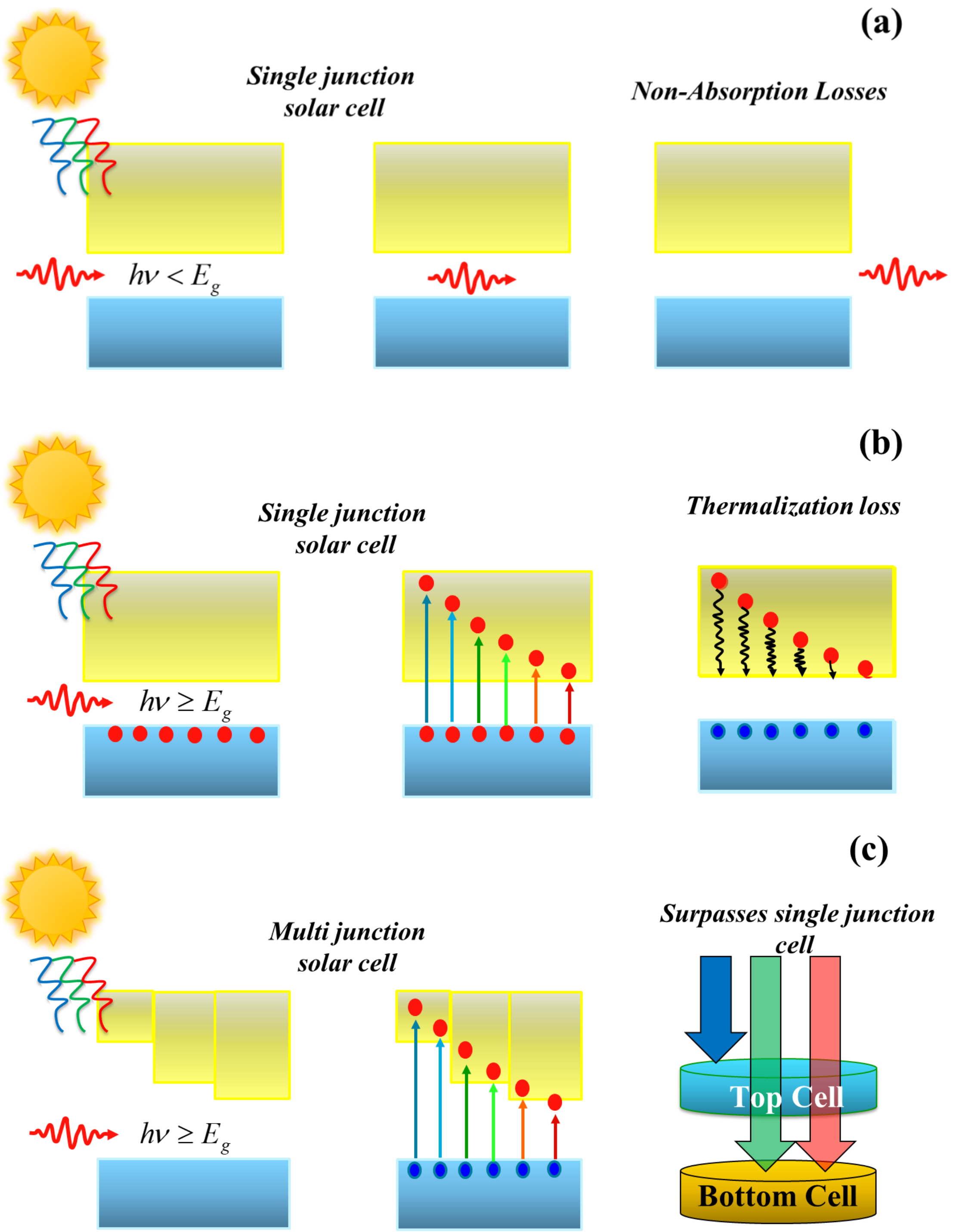


Figure 1: *Schematic illustration of (a) non-absorption loss in a single junction (b) thermalization loss in a single junction (c) reduction of both thermalization and non-absorption loss in a multi-junction solar cell.*

1.3 Re-emergence of a warrior

Copper indium gallium disulfide ($Cu(In,Ga)S_2$), a quaternary alloy system, has tremendous potential for becoming a top cell partner for Si and $Cu(In,Ga)S_2$ tandem devices. The bandgap of

$Cu(In,Ga)S_2$ can be tuned from 1.54 eV ($CuInS_2$) to 2.53eV ($CuGaS_2$) by varying the indium to gallium concentration in the deposited film.[16] Moreover, properties such as direct bandgap and large absorption coefficient make $Cu(In,Ga)S_2$ a good (solar) absorber material for thin-film PV application. This would mean low material and energy consumption for the fabrication process and, therefore, a small energy payback time.[17]

Due to its structural tolerance to compositional variation, $Cu(In,Ga)S_2$ has a phase stability region even outside the stoichiometric region, making it possible to grow stable films even under non-stoichiometry conditions within a certain limit.[18, 19] Depending upon the growth conditions, the final as-grown film composition can be [Cu]/ ([Ga] + [In]) or CGI < 1; generally labelled "Cu-poor", or it can be [Cu]/ ([Ga] + [In]) or CGI > 1 labelled as "Cu-rich", a film which is not pure phase $Cu(In,Ga)S_2$ but rather a mixture of $Cu(In,Ga)S_2$ and $Cu_{2-x}S$ phase.[18] The current record of 15.5 % efficient $Cu(In,Ga)S_2$ devices [20] are realized by growing absorber at a temperature above 550 ^oC with as grown Cu-poor composition. Barring this new record device, $CuInS_2$ devices were historically realized with absorbers grown with a Cu-rich composition.[21-23] As, historically, Cu-poor $CuInS_2$ characterized with low mobility value of carriers,[24] and were therefore deemed unsuitable for solar cell application.[25] In his dissertation, A. Lomuscio studied the optical properties of Cu-rich and Cu-poor as grown $CuInS_2$ films under various deposition conditions, particularly the internal open-circuit voltage or quasi-Fermi level splitting ($V_{OC,in}$ or qFLs). The $V_{OC,in}$, which is measured optically using calibrated photoluminescence (PL), is an important characteristic of a solar cell and gives the measure of the bulk quality of the absorber. He demonstrated that the Cu-rich $CuInS_2$ films possess a higher characteristic $V_{OC,in}$ than the Cu-poor $CuInS_2$ films.[26] Although, the $V_{OC,in}$ for Cu-rich absorbers was still significantly lower (~700 meV) than the bandgap (1.5 eV).[27, 28] Moreover, solar cells obtained from corresponding absorbers suffer a deficit between a $V_{OC,in}$ and external open-circuit voltage ($V_{OC,ex}$).[26, 28] The $V_{OC,ex}$ represents the overall quality of the device as it takes into account the interfaces and contacts in addition to the absorber. Thus, a difference between the $V_{OC,in}$ and $V_{OC,ex}$, defined in this thesis as interface V_{OC} deficit, in Cu-rich $CuInS_2$ devices leads to lower device performance.[28] This deficit could result from unfavorable band-offset at $CuInS_2$/CdS interface,[29, 30] when using CdS as a buffer layer, and the native defects present near the surface of the $Cu(In,Ga)S_2$.[28, 31-33] Both these factors affect the $V_{OC,ex}$ and performance of the $Cu(In,Ga)S_2$ solar cell through various physical processes and recombination mechanisms.[34]

To use Cu(In,Ga)S_2 as the top cell in tandem solar cell, obtaining efficiency and, more particularly $V_{OC,ex}$ values much higher than the present values are required. These aspirations require a good $V_{OC,in}$ and its translation to $V_{OC,ex}$ without a significant difference between the two. The Cu(In,Ga)S_2 solar cell structure comprises multilayers - absorber, buffer, i-layer, contact layers etc. Any of these layers can introduce a $V_{OC,in}$ gradient due to non-radiative recombinations in them[35] and thus an interface V_{OC} deficit. Therefore, it is essential to identify and minimize the non-radiative recombination channels in the complete device to have a constant $V_{OC,in}$ throughout the device structure,[36] *i.e.* to translate the optical quality of the absorber into electrical efficiency, *i.e.* $V_{OC,ex}$.[37, 38]. This can only be achieved with an enhanced understanding of recombination processes in these devices. However, there have been no dedicated studies that focused solely on detecting and identifying the source of interface V_{OC} deficit in Cu(In,Ga)S_2 solar cells by combining $V_{OC,ex}$ and $V_{OC,in}$ measurements.

1.4 Scope of this thesis

This thesis aims to explore, understand and reduce the interface V_{OC} deficit in Cu(In,Ga)S_2 solar cells having a bandgap ~1.6 eV, with the motivation to make them a viable candidate for the top cell in a tandem solar cell. In particular, the focus will be on the interface properties of these solar cells. This is accomplished by characterizing Cu(In,Ga)S_2 solar cell with special attention to the absorber buffer interface, the limiting interface in these devices.

A detailed investigation of the electrical properties of solar cells made with Cu(In,Ga)S_2, along with numerical simulations, can provide some valuable insights into the interface V_{OC} defect in these devices. To perform this analysis Cu(In,Ga)S_2 absorbers, grown with either Cu-rich stoichiometry, *i.e.* [Cu]/[In+Ga] atomic concentration > 1 or Cu-poor, *i.e.* [Cu]/[In+Ga] atomic concentration < 1 are considered. The current-voltage measurements are explored to gain information about the $V_{OC,ex}$, the maximum voltage across the contacts in the solar cells. These $V_{OC,ex}$ values are compared to the $V_{OC,in}$ values, the maximum extractable voltage from a solar cell. The $V_{OC,in}$ measurement, however, is not a part of this work. A benchmark "interface V_{OC} deficit" will be used to quantify the difference between $V_{OC,in}$ and $V_{OC,ex}$. Temperature-dependent $V_{OC,ex}$ measurements can corroborate the source of dominating recombination in the device and is therefore used here to uncover interface recombination in the devices.

Different buffer layer materials CdS, Zn(O,S), ZnMgO and ZnSnO, deposited using chemical and physical deposition techniques, are explored as possible candidates for realizing optimum device performance. However, the effect of change of thickness and individual characteristics of the buffer layer is not studied in this work. The main results of this part of the study show that for Cu-poor Cu(In,Ga)S_2, it is possible to significantly reduce the interface V_{OC} deficit by using alternative buffer and i-layers. However, this approach does not reduce the interface V_{OC} deficit for Cu-rich Cu(In,Ga)S_2 solar cells, making the source of the deficit unclear.

The main accomplishment of this thesis is discovering the source of interface V_{OC} deficit and interface recombination in Cu-rich Cu(In,Ga)S_2 and even Cu(In,Ga)Se_2 devices. For this, we will perform a detailed electrical and numerical investigation on the ternary counterparts Cu-rich $CuInS_2$ and $CuInSe_2$, a simpler system due to Ga omission. Taking motivation from A. Lomuscio's work [26], a dedicated sulfur post-deposition treatment (PDT) will be devised to gain more insights into the puzzling cause of interface V_{OC} deficit. Along with this, the impact of PDTs, namely: Na_2S, $(NH_4)_2S$, Zn, Cd, Br etching and KCN etching, on device performance and defect signatures will be investigated. For this part, we will use specific characterization techniques such as: current-voltage measurements, admittance spectroscopy, capacitance transient measurements, and deep level transient spectroscopy (however, rarely due to setup accessibility constraints). The chemistry of these PDTs will not be optimized in the course of this thesis.

Using the extracted data from the electrical analysis of PDT samples, a numerical model will be developed to explain the experimental observations. The model explores the possibility of obtaining the signature of interface recombination that can only be observed through classical origins of interface recombination.

1.5 Structure of the thesis

For the characterization of devices, I-V and capacitance measurements were used as the two essential techniques because they probe and provide insights into the absorber buffer interface or the p-n junction. The basic principles of these techniques and the working principles of a solar cell are presented in chapter 2. The chapter introduces p-n junction, followed by the basics of solar cell operation and characterization by I-V measurements. The capacitance measurements technique is introduced together with information that can be extracted using these measurements. After describing measurement techniques, a literature review is provided for $Cu(In,Ga)S_2$. The latter half of chapter 2 presents the impact of band-offsets at the absorber/buffer and buffer/interface on the device $V_{OC,ex}$ and efficiency. At last, a discussion on the influence of metastable defects and barriers in the device structure concludes the chapter.

Chapter 3 discusses deposition techniques used to deposit absorber, buffer, window, and front contact layers to complete the device. A short description of the process used to grow $Cu(In,Ga)S_2$ thin films used in this work is provided. The procedure is developed by A. Lomuscio, S. Shukla, and D. Adeleye and is not a part of this thesis. In addition, the process to deposit $CuInSe_2$ is also provided. The setup details of the characterization techniques used in this work is also encompassed here. This includes the electrical characterization, as well as the band energetic characterizations. The band energetic characterizations were done in the HZB BESSY II facility, with Jakob Bombsch, who contributed to a large portion of this section. In this thesis, drift-diffusion simulations using solar cell capacitance simulator (SCAPS-1D) is used widely. Hence a short description of SCAPS is also provided.

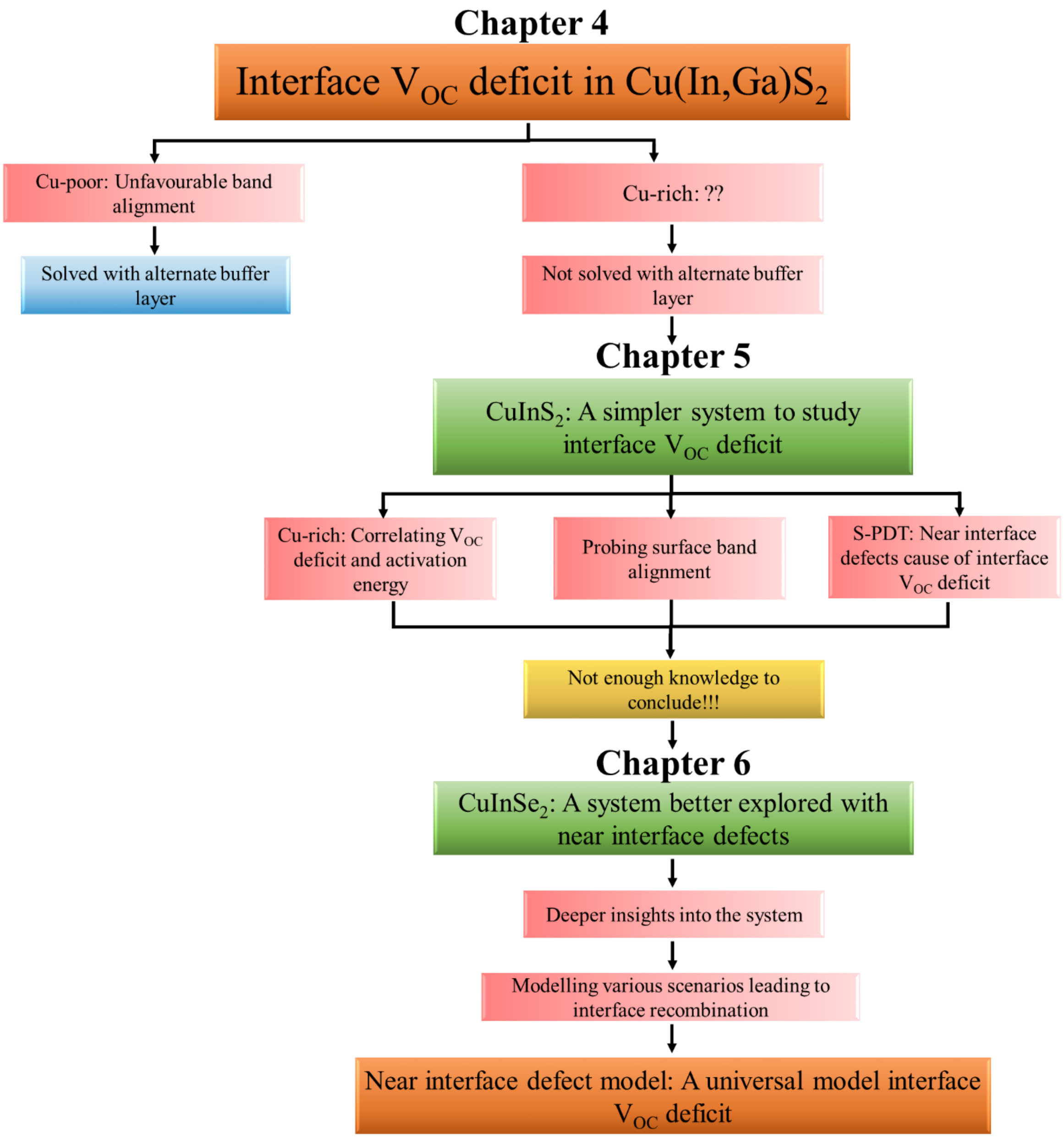


Figure. 1.2: *Flow chart of this thesis from chapter 4 onwards.*

The rest of the thesis loosely follows the flow chart shown in Fig. 1.2. In chapter 4, the $Cu(In,Ga)S_2$ solar cells are probed, emphasizing the interface V_{OC} deficit. The deficit has been linked to interface recombination in the device in other thin-film solar cells, namely $Cu(In,Ga)Se_2$, CdTe, and perovskite.[38-42] The mismatch of the energy bands at the interface between absorber and buffer/charge transport layer,[38, 43] and Fermi level pinning[44] are the two commonly evoked models[45] to explain the interface recombination in these devices. Therefore, a comparison between the device performance of Cu-rich and Cu-poor $Cu(In,Ga)S_2$ devices prepared with CdS and Zn(O,S) buffer layers is presented in section 4.1. This comparison helps comprehend the role of band alignment at the absorber/buffer interface on the interface V_{OC} deficit. For Cu-poor devices, alternate buffer layers are explored to minimize the interface V_{OC} deficit. Section 4.2 and 4.3 are devoted to developing ZnMgO and ZnSnO buffer, and ZnO, ZnMgO i-layers for Cu-poor Cu(In,Ga)S_2 devices. Using electrical analysis and numerical simulations, the impact of these buffer and i-layers on the solar cell's performance is analyzed. A pathway to reach high-efficiency Cu-poor Cu(In,Ga)S_2 devices is discussed in the end. We show that it is possible to significantly reduce the interface V_{OC} deficit for Cu-poor Cu(In,Ga)S_2, by using a buffer layer that has optimum band alignment with the Cu(In,Ga)S_2. This approach, however, does not reduce the interface V_{OC} deficit for Cu-rich Cu(In,Ga)S_2 solar cells, making the source of the deficit unclear for these devices.

In chapter 5, for a detailed investigation to comprehend the cause of the interface V_{OC} deficit in Cu-rich Cu(In,Ga)S_2 solar cell, we explore $CuInS_2$, a system with reduced complexity due to Ga exclusion. Section 5.1 compares Cu-rich and Cu-poor devices prepared with Zn(O,S) buffer layers to see if $CuInS_2$ also suffers from interface V_{OC} deficit for the same causes. We perform comprehensive photoelectron spectroscopy measurements on the absorber buffer interface in section 5.2. In section 5.3, we present the results of surface treatments devised to passivate near-surface defects together with a discussion on the metastability of these defects. Building a reliable model to understand the interface V_{OC} deficit requires better knowledge of the defect responsible, which was not accessible through admittance spectroscopy of $CuInS_2$. This evoked the need to study $CuInSe_2$ a closely related alloy system, to develop a model that explains the interface V_{OC} deficit. The $CuInSe_2$ system also suffers from interface V_{OC} deficit in Cu-rich solar cells, which is well linked to the "200 meV defect" signature in the admittance spectroscopy.[46] However, a model for interface V_{OC} deficit is missing for this system too. Therefore, the knowledge of this system can be used to model interface V_{OC} deficit in Cu-rich Cu(In,Ga)S_2 devices along with $CuInSe_2$ devices.

Chapter 6 is dedicated to gaining more insights into the defect, such as root cause, nature, possible passivation strategies, and concentration in the $CuInSe_2$ system. In section 6.1, results of I-V measurements are revisited to understand the similarities between the $CuInS_2$ and $CuInSe_2$ devices. Section 6.2 discusses the properties of the defect culprit for the interface V_{OC} deficit in the devices by probing the effect of different post-deposition treatments using admittance spectroscopy and deep-level transient spectroscopy measurements. Finally, in section 6.3, we devise a near interface defect model based on experimental observations using all the information on the defect characteristics. Using numerical simulations, we compare various scenarios leading to interface V_{OC} deficit in a device. A near-surface defective model successfully explaining the experimental observations is highlighted, which has the scope and validity beyond $Cu(In,Ga)(S,Se)_2$ solar cells.

Chapter 7 summarizes the results discussed throughout this thesis, together with an outlook.

1.6 Contributions in the thesis

For the devices presented in chapter 4, I deposited the CdS and the Zn(O,S) buffer layers together with Al:ZnMgO and Al:ZnO window layers, completed the device's fabrication and measured the electrical characteristics of the final devices. Poorani Gnanasambandan deposited the buffers ZnMgO at Luxembourg Institute of Technology, and Dr. Tobias Törndahl and Dr. Adam Hultqvist at Uppsala University deposited ZnSnO buffer at Angstrom laboratory. Dr. Sudhanshu Shukla prepared the absorbers, and Damilola Adeleye measured the optical characteristics of the absorbers. Dr. Michele Melchiorre and Damilola Adeleye characterized absorbers using scanning electron microscope and energy dispersive x-ray (EDX) spectroscopy. To measure the elemental composition of as-grown absorbers, ZnMgO and ZnSnO buffer layers energy-dispersive x-ray spectroscopy (EDX) at 20 kV was performed using a 20 mm^2 area Oxford Instruments X-Max Silicon Drift Detector (SDD) installed in a Hitachi SU-70 field-emission SEM with a Schottky electron source and with a secondary electron detector. In addition to this microscope, a 40 mm^2 area Oxford Instruments UltimMax40 Silicon Drift Detector (SDD) installed in a Zeiss EVO10 microscope with a LaB6 emission system and with a secondary electron detector was used to measure the EDX at 20 kV, 5 kV. The measurements at 20 kV were done to know the average composition of the absorbers, whereas the 5 kV measurements were done to know the composition close to the surface.

For the devices discussed in chapter 5, I deposited the buffer layer on the absorbers and measured electrical characteristics on the final devices. I also developed post-deposition treatments. Dr. Alberto Lomuscio prepared the absorbers and measured the optical characteristics of the absorbers. Dr. Michele Melchiorre prepared final devices and characterized absorbers using scanning electron microscope and energy dispersive x-ray (EDX) spectroscopy. Jakob Bombsch, Dr. Regan G. Wilks, Dr. Marcus Bär and Dr. Jérôme Guillot performed all the photoelectron measurements.

For the devices discussed in chapter 6, I developed the post-deposition treatments. The buffer layers were deposited on the absorbers by Dr. Michele Melchiorre and me. Dr. Alberto Lomuscio prepared the $CuInS_2$ absorbers and the $CuInSe_2$ absorbers were prepared by Dr. Hossam Elanzeery and Dr. Finn Babbe. The device preparation steps after buffer layer deposition were performed by Dr. Michele Melchiorre, who also characterized absorbers using the scanning electron microscope and energy dispersive x-ray (EDX) spectroscopy. The optical characteristics of the absorbers were measured by Dr. Alberto Lomuscio and Dr. Finn Babbe. The electrical characteristics of the absorbers were measured by me, except for deep level transient spectroscopy (DLTS), which was measured and interpreted by Dr. Aleksander Urbaniak of Warsaw University of Technology.

Chapter 2

Background

This chapter provides an overview of the basics of solar cells along with the important background to Cu(In,Ga)S_2 solar cells in the context of the present work. Although a working solar cell only requires selective contacts and not necessarily requires a p-n junction,[47] the chalcogenide solar cells are, however based on p-n junction.[48] The chapter is divided into two sections; the first section focuses on the p-n junction and its properties. The properties of a p-n junction under dark and illumination form the basis of chalcogenide solar cells, *i.e.* its current-voltage characteristics and capacitance spectroscopy. Most discussion presented here will be brief and is taken from [45, 49, 50], as it is meant to provide a summary for grasping the results presented in chapter 4-6. For a detailed description, the reader should refer to standard textbooks on solar cell basics.[48-51]

The second section introduces Cu(In,Ga)S_2 together with a brief literature summary on historical and recent developments in the field. Later, the band offsets at the absorber/buffer and buffer/window interface are discussed for Cu(In,Ga)S_2 device with traditional buffer and window layers. A complimentary discussion is also presented on how the band-offset at these interfaces leads to barriers for charge carriers. Lastly, an introduction to metastability in Cu(In,Ga)S(e)$_2$ solar cells and its impact on device performance is discussed.

2.1 Fundamentals and electrical characterization of solar cells

2.1.1 The p-n junction: the driver of solar cell

A solar cell is a semiconducting material with a certain bandgap or sometimes even bandgap gradient, as in the case of record chalcogenide solar cells [9, 20], which absorbs the sunlight and consequently generates electron-hole pairs. However, when generated, these charge carriers do not have a preferred direction of movement. To extract a photocurrent from the device, the generated carriers, *i.e.* electron and hole, must exit the device from opposite ends. In chalcogenide solar cells, this is achieved *via* the built-in asymmetry of a p-n junction, *i.e.* a p-type and n-type semiconductor that are connected. The formation of a p-n junction can be understood by a thought experiment as follows: At the point of contact between p and n-type semiconductor, the free electron density (the ionized donor density) N_d or the electron chemical potential on the p-region of the contact is much lower than on the n-region of the contact. Vice-versa holds true for free hole density (ionized acceptor density) N_a. Consequently, electrons from the n-region diffuse towards the p-region, and holes from the p-region diffuse towards the n-region semiconductor. The diffusion process of these carriers results in the accumulation of negative charges on the p-region and positive charges in the n-region of the junction. This process triggers the build-up of an electrostatic field. This electrostatic field would lead to electrons drifting from the p-region to the n-region (vice-versa for holes). The two processes, diffusion and drift, lead to a flow of respective current in the device and is given by:[49]

$$J_{diffusion,i} = -\frac{\sigma_i}{z_i e}\nabla(\xi_i) \tag{2.1}$$

$$J_{drift,i} = -\frac{\sigma_i}{e}\nabla(e\phi) \tag{2.2}$$

i is the carrier type, σ_i is the electrical conductivity of the carrier, z_i is the charge of the carrier, e is the elementary charge, ξ_i is the chemical potential of the carrier and φ is the electrostatic potential. At thermal equilibrium, the two driving forces, diffusion and drift add up to zero.[50] Consequently, no carrier flows from n to p or p to n region, and hence the total current in the device equals zero.

$$J_{total,i} = -\frac{\sigma_i}{e}\nabla(e\varphi) - \frac{\sigma_i}{z_i e}\nabla(\xi_i) = 0 \tag{2.3}$$

$$J_{total,i} = -\frac{\sigma_i}{z_i e}\nabla(z_i e\varphi + \xi_i) = 0 \tag{2.4}$$

$$J_{total,i} = -\frac{\sigma_i}{z_i e}\nabla(E_{f\,i}) = 0 \tag{2.5}$$

where E_{fi} is the electrochemical potential, which is constant under thermal equilibrium and is the driving force under non-equilibrium conditions.

Formation of depletion region: Two common characteristics of p-n junction that are of significant interest are depletion width or space charge region width and built-in potential. Let us look at a small derivation of these two parameters. Assuming an infinite p-n semiconductor on both sides, the electrostatic potential drops to zero at a certain distance from the junction. The region from the junction where the electrostatic potential becomes zero is known as the space charge region (SCR). Since the electron affinity and bandgap are fixed quantities for a semiconductor, in the SCR, only the vacuum energy changes on the two sides of the junction. This phenomenon is referred to as band bending, and it is quantified by the term built-in voltage (V_{bi}). A sketch of above-mentioned process is presented in Fig. 2.1.

$$qV_{bi} = E_g - \left(qE_{fp\infty} + qE_{fn\infty}\right) = q\varphi_p + q\varphi_n \tag{2.6}$$

Where $E_{fp\infty}$ is the distance of hole Fermi-level from the valence band on the p-side and $E_{fp\infty}$ is the distance of electron Fermi-level from the conduction band on the n-side far away from the junction. To calculate SCR width, let’s first assume depletion approximation holds true, *i.e.* a box-like distribution of charges on either side of the junction, and full ionization of the dopant on either side of the junction, complete charge neutrality and an abrupt junction at the point where the two semiconductors are joined x = 0. The charge neutrality then reads:

$$N_a x_p = N_d x_n \tag{2.7}$$

where N_a and N_d are the net acceptor and donor concentration on the p-region and n-region of the junction, x_p is the space charge width extending into the p-region of the junction, and x_n is the space charge width extending into the n-region of the junction. From the Poisson equation with proper boundary conditions, the potential drop on either side of the junction is given by:

$$\varphi_p = \frac{qN_a x_p^2}{2\varepsilon_{r1}\varepsilon_0} \quad \text{and} \quad \varphi_n = \frac{qN_d x_n^2}{2\varepsilon_{r2}\varepsilon_0} \tag{2.8}$$

here ε_0, ε_{r1} and ε_{r2} are the vacuum permittivity and the dielectric constant of the p-type material and n-type material constituting either region of the junction. Together with equations 2.6, 2.7, and 2.8 and assuming $\varepsilon_{r2} = \varepsilon_{r2} = \varepsilon_r$, the SCR on p and n region is given by:

$$x_p = \sqrt{\frac{2\varepsilon_r\varepsilon_0 V_{bi}}{q}\frac{N_d}{N_a(N_a+N_d)}} \quad \text{and} \quad x_n = \sqrt{\frac{2\varepsilon_r\varepsilon_0 V_{bi}}{q}\frac{N_a}{N_d(N_a+N_d)}} \tag{2.9}$$

In case the n-region of the junction is heavily doped compared to the p-region of the junction (*i.e.* p-n$^+$), which is usually the case for chalcopyrite solar cells $N_d >> N_a$ the SCR simplifies to:

$$x_p = \sqrt{\frac{2\varepsilon_r \varepsilon_0 V_{bi}}{qN_a}} = x_{SCR} \qquad \text{and} \qquad x_n \approx 0 \tag{2.10}$$

Under application of an external voltage (V) the total potential across the junction is given by V_{bi}-V, with V being positive for a forward bias and negative for a reverse bias. We will come back to these equations when we discuss capacitance measurements.

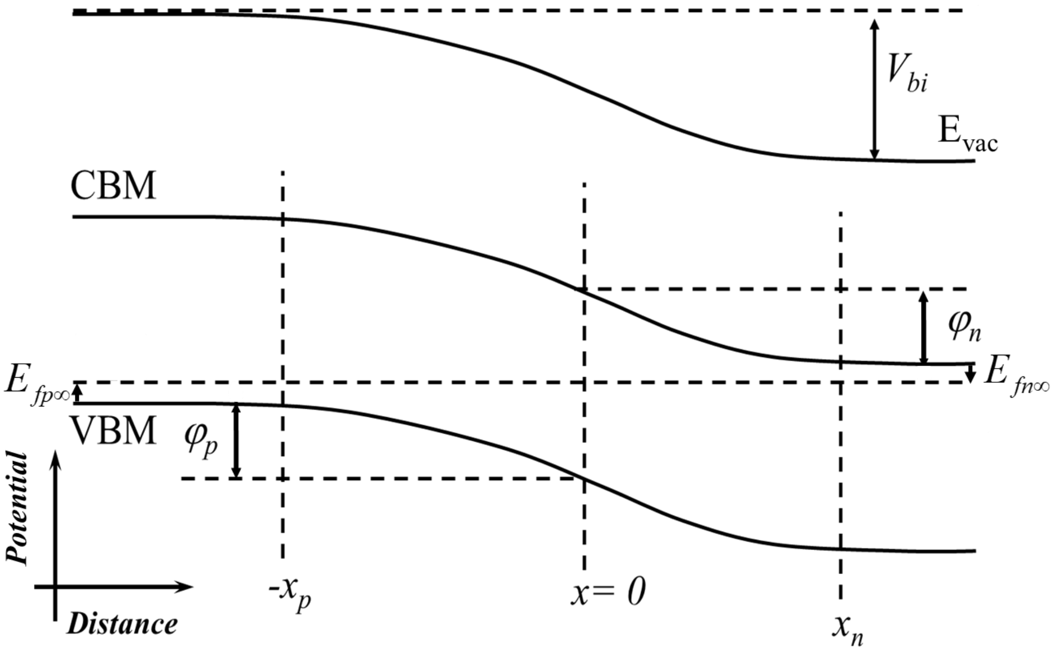


Figure 2.1: *Sketch of the band diagram of a p-n junction* **(***not to scale), depicting band bending and depletion width on the p and n region.*

2.1.2 Solar cell basics: IV measurements

IV characteristic of an ideal solar cell

So far, solar cell as a p-n junction was discussed under thermal equilibrium. We now discuss it under two non-equilibrium conditions: under an applied voltage and under illumination. Under the application of a voltage, a net current flows through the junction that is given by the diode equation.

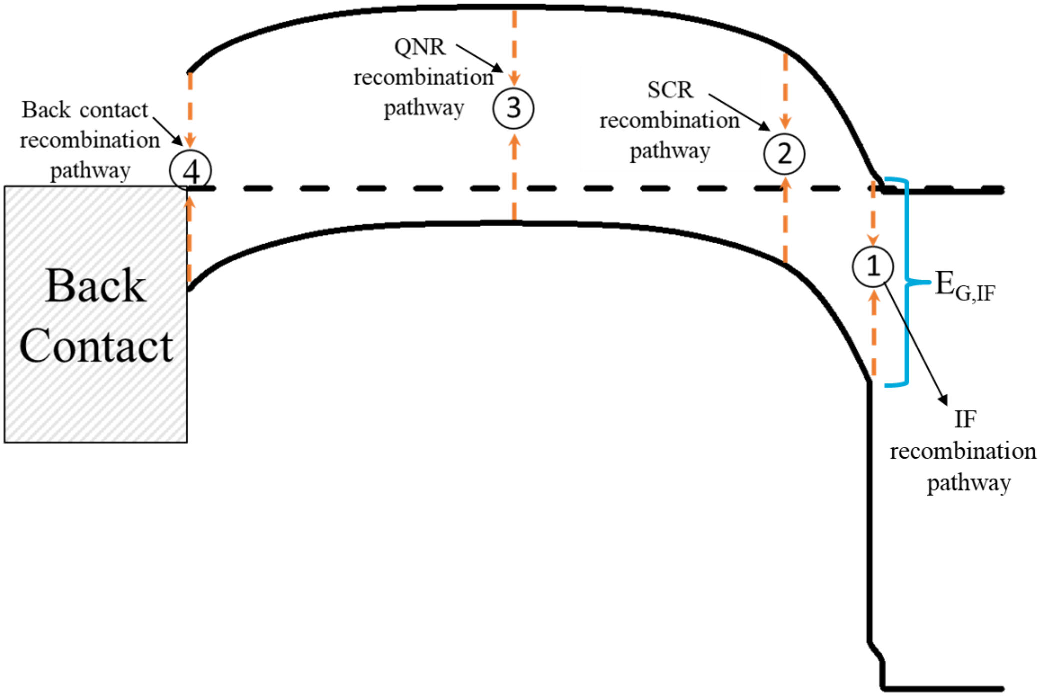


Figure 2.2: *Sketch of Cu(In,Ga)S$_2$ solar cell displaying four most prominent dominating recombination path (adapted from [45]). The figure also shows the interface bandgap, which is the difference between min(conduction band minima at the interface) and max(conduction band maxima at the interface).*

In a heterostructure device, the recombination may occur from any path depicted in Fig. 2.2. This can be at the p-n junction interface (path 1), SCR (path 2), quasi-neutral region (path 3) and back contact (path 4). Complete details of these recombination paths can be found in [45]. Depending upon the activation energy of these recombination rates, either one will dominate the diode current. Neglecting the contribution from the back surface recombination and further assuming that the diode current flows in only one dimension (x) for ease of analysis, the diode current density J_{diode} can be described as:

$$J_{diode} = J_{diode,QNR} + J_{diode,SCR} + J_{diode,IF} \tag{2.11}$$

where

$$J_{diode,QNR} = qD_n \frac{dn(x)}{dz}\Big|_{x=-w_a} \tag{2.12}$$

and

$$J_{diode,SCR} = q\int_{-x_a}^{0} (U_n(x) - G_0(x))dx \tag{2.13}$$

where $J_{diode,QNR}$, $J_{diode,SCR}$ *and* $J_{diode,IF}$ are the diode current density in quasi-neutral region, space charge region and interface, respectively. D_n is the electron diffusion coefficient; Un and G_0 are the recombination rate in thermal equilibrium and generation rate under illumination. The three terms on the right side of the equation 2.11 contain the carrier density term in them, hence, can be described by a voltage and temperature-dependent exponential equation:[45]

$$J_{dark} = J_0\left(\exp\left(\frac{eV}{Ak_BT}\right)-1\right) \tag{2.14}$$

with

$$J_0 = J_{00}\left(\exp\left(\frac{-E_a}{Ak_BT}\right)\right) \tag{2.15}$$

Under illumination

$$J_{light} = J_0\left(\exp\left(\frac{eV}{Ak_BT}\right)-1\right)-J_{ph} \tag{2.16}$$

where J_{dark} and J_{light} are the is the total current density under dark and illumination, V is the applied voltage, J_{ph} is the photocurrent density incorporating the total generation current and is known as J_{SC} short-circuit current density at 0V (neglecting any parasitic series or shunt resistance, will be discussed shortly). J_0 is the saturation current density and is activated by E_a the activation energy. A is the ideality factor and is usually between 1 or 2 depending on the recombination process. J_{00} is a weakly temperature-dependent term and is labeled as reference current density. The two terms J_0 and A incorporate complete information about the recombination process in the device.

Fig. 2.3 depicts the J-V curve of a solar cell in the dark and under illuminations and is described by equations 2.14 and 2.16. Like any power generating device, the efficiency of a solar cell is given by the ratio of maximum power out to power in. For comparability of solar cells made anywhere in the world, a global power-in known as 'air mass 1.5 global' (AM 1.5) with illumination intensity 100 mW cm^{-2} is used to illuminate and calculate the efficiency of all standard solar cells. The maximum power point in J-V curve (Fig. 2.3) is the point where the product of current density and voltage is maximum. Other than this, the solar cell has two important parameters which signify the quality of the device J_{SC} and $V_{OC,ex}$. The J_{SC} contains information about the percentage of photons that have been converted into electron-hole pairs. The $V_{OC,ex}$ is the voltage at zero current and contains the information regarding the percentage of non-radiative to radiative recombination in the device. Fill factor is another important term that contains information about the ratio of maximum power obtainable for a particular J_{SC} and $V_{OC,ex}$ in a solar cell. It is calculated from the quotient of maximum power (P_{max}) to the product of J_{SC} and $V_{OC,ex}$, *i.e.* $FF=P_{max}/(J_{SC} \times V_{OC,ex})$. Because of the inherent exponential nature of the diode equation, the FF is never unity. The power conversion efficiency (PCE) of a solar cell device can be computed by either directly as the ratio of maximum power to input power (P_{in}), *i.e.* $PCE = P_{max}/P_{in}$, with P_{in} equal to 100 mW/cm^2, *i.e.* AM1.5G power or 'one sun', or using the definition of FF, *i.e.* $PCE = (FF \times J_{SC} \times V_{OC,ex})/P_{in}$. Throughout this thesis, we will use the latter to compute the devices' PCE, except for the certified measurements where the first expression is used. Also, the I-V curve can be divided into four quadrants, as depicted in Fig. 2.3. Often in this thesis, these quadrants will be referred to. Hence one must remember these quadrant nomenclatures for better understanding the discussion in the thesis.

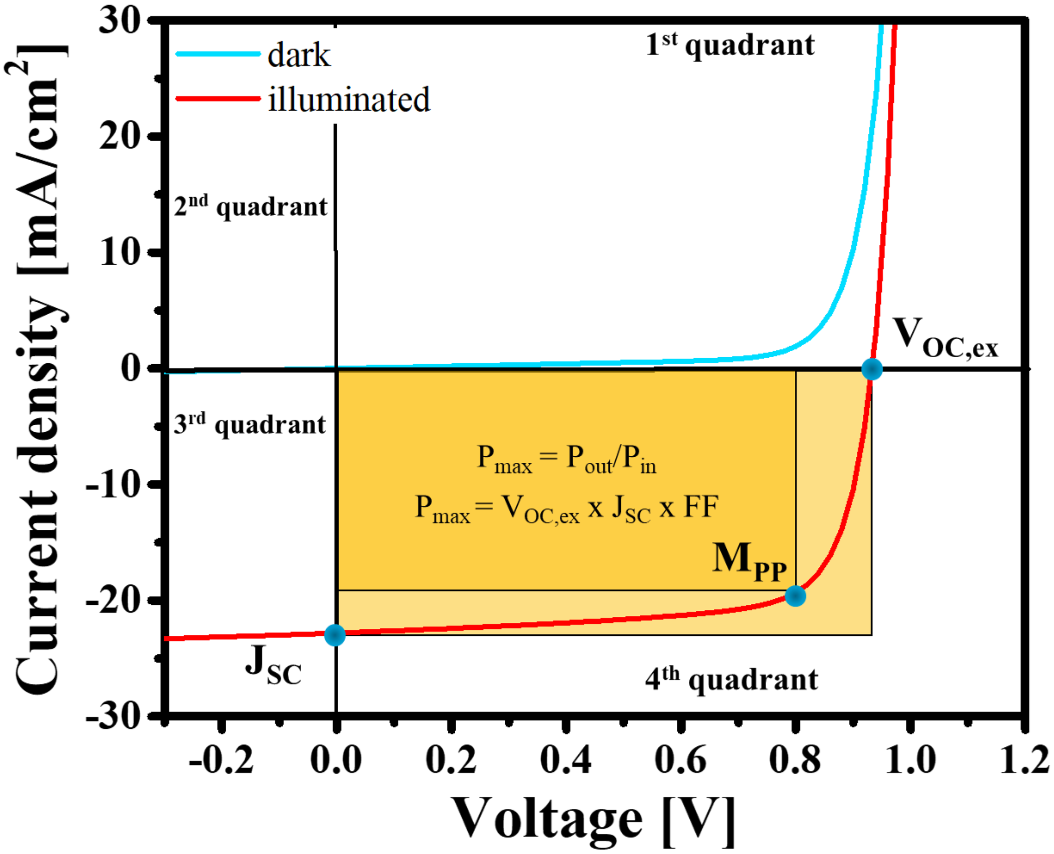


Figure 2.3: *Exemplary I-V curve of a solar cell under dark and illumination. Dark yellow rectangle indicates the maximum power that can be extracted from the device, and the light yellow rectangle shows the maximum power that could be generated, i.e.* $J_{SC} \times V_{OCex}$.

Non-ideal IV characteristic of a solar cell

So far, in deriving the diode current, we have ignored the fact that the semiconductor used to fabricate a solar cell has a finite conductivity. In non-ideal (real) solar cells, this finite conductivity results in a difference between the external voltage (V_{ext}) or applied voltage and internal voltage (V_i) or the actual voltage across the diode. Thus, a series resistance term 'R_s' has to be included in equation 2.16 to account for the voltage difference. R_s can originate from other factors such as bandgap gradient in the absorber or barriers at the front and back contact. In addition, to account for the shunting pathways across the diode, an additional term 'shunt resistance R_{sh}' has to be included. The model including one diode R_s and R_{sh} is known as the 1-diode model (Fig. 2.4).

$$J_{light} = J_0\left(\exp\left(\frac{e(V_{ext} - R_s J_{light})}{Ak_B T}\right) - 1\right) + \frac{V_{ext} - R_s J_{light}}{R_{sh}} - J_{ph} \tag{2.17}$$

Thus, both R_{sh} and R_s impact the maximum power point and consequently the FF of the device. Martin Green has worked out an expression for the impact on FF of R_{sh} and R_s in his book [52], which is as follows:

$$FF = FF_0\left\{(1-1.1r_s) + \frac{r_s^{\,2}}{5.4}\right\}\left\{1 - \frac{V_{OC,ex} + 0.7}{V_{OC,ex}} * \frac{FF_0}{r_{sh}}\left[(1-1.1r_s) + \frac{r_s^{\,2}}{5.4}\right]\right\} \tag{2.18}$$

Where FF_0 is the fill factor of the device without any shunt and series resistance, r_s is the normalized series resistance in ohms and is equal to $R_s * I_{SC}/V_{OC}$, r_{sh} is the normalized shunt resistance in ohms and is equal to $R_{sh} * I_{SC}/V_{OC}$, I_{SC} is the short circuit current, and FF is the fill factor of the device having both shunt and series resistance. From the equation, it can be seen that the FF of a device decreases as the R_s increases and as the R_{sh} decreases. Hence to get a good PCE, the R_s must be minimized and R_{sh} must be maximized. I would urge the reader to visit "https://www.pveducation.org/pvcdrom/solar-cell-operation/impact-of-both-series-and-shunt-resistance" to have a better visualization of how R_s and R_{sh} affect the I-V curve and FF of a solar cell.

In this thesis, for determination of the device parameters such as J_0, A, R_s and R_{sh} I-V fit routine [53] was used to fit IV curve to equation 2.17 using a python script developed in our lab by Dr. Thomas Weiss. A detailed description can be found in his doctoral dissertation.[54]

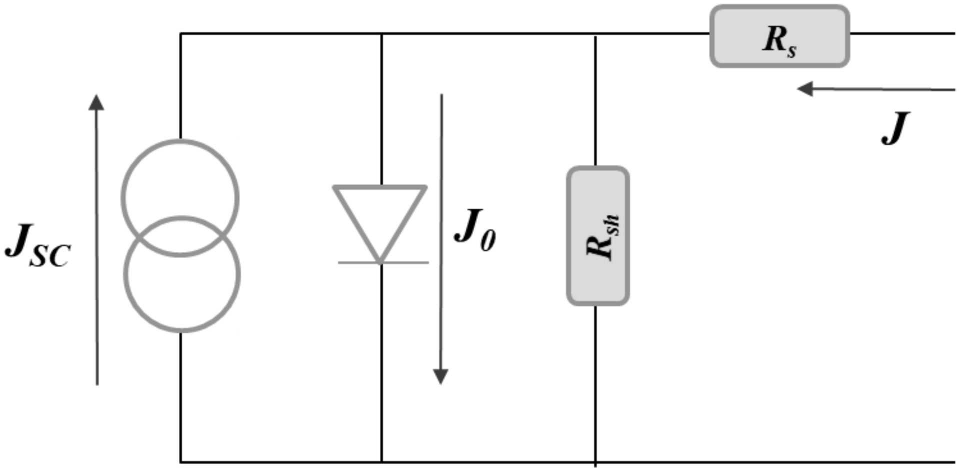


Figure 2.4: *Equivalent 1-diode circuit of a p-n junction solar cell. The circuit consists of a current source represented by* J_{SC}*, one diode, one series resistance and one shunt resistance.*

Temperature-dependent IV measurements

I-V measurements performed at different temperatures (IVT) reveal important device characteristics, such as dominant recombination current path or barrier heights in the device. At $V_{OC,ex}$, the equation 2.14 together with equation equation 2.15 transforms to give:[45]

$$V_{OC,ex} \approx \frac{E_a}{e} - \frac{AkT}{e}\left(\frac{J_{00}}{J_{ph}}\right) \tag{2.19}$$

Thus, by measuring the $V_{OC,ex}$ of the device as a function of temperature, one can extract the activation energy E_a of the saturation current density, provided the temperature dependence of A, J_{00} and J_{ph} can be neglected. Devices that are not dominated by interface recombinations the $E_a = E_G$ of the absorber, whereas for devices dominated by interface recombinations, either due to a negative conduction band offset (introduced in section 2.2.1) at the absorber/buffer interface or due to Fermi-level pinning, E_a is less than E_G as the above expression modifies to:[45, 55]

either
$$V_{OC,ex} \approx \frac{E_{G,IF}}{e} - \frac{kT}{e}\left(\frac{J_{00}}{J_{ph}}\right) \tag{2.20}$$

or
$$V_{OC,ex} \approx \frac{E_b{}^h}{e} - \frac{kT}{e}\left(\frac{J_{00}}{J_{ph}}\right) \tag{2.21}$$

Here, $E_{G,IF}$ is the interface band gap (see Fig. 2.2), which is the difference between conduction band minima of absorber or buffer (whichever is the lower of the two) and valence band maximum of absorber or buffer (whichever is higher of the two), 'e' is the elementary charge, E_b^h is the equilibrium hole barrier at the interface and is equal to the energy difference between the position of electron Fermi level (F_e) and the valence band edge (E_v) of the absorber, *i.e.* $E_b^h = F_e - E_v$.[56] Equation 2.20 and 2.21 are the modified version of equation equation 2.19 for a negative conduction band offset and Fermi-level pinning at the absorber/buffer interface, respectively. Therefore, the E_a energy for negative conduction band offset at the absorber/buffer interface is given by the interface bandgap $E_{G,IF}$, and is equal to the position of pinned Fermi-level from the absorber valence band.[55] The $Cu(In,Ga)S_2$ and Cu-rich $CuInSe_2$ solar cells have been known to suffer from strong interface recombination.[32, 33, 57] IVT measurement becomes an indispensable tool for characterizing the activation energy of the dominant recombination path in the device. In chapters 4, 5 and 6, both these parameters, *i.e.* $V_{OC,ex}$ and E_a will be studied, and device performance will be discussed in light of these parameters.

2.1.3 Solar cell basics: External quantum efficiency measurements

A solar cell usually suffers from many optical and recombination loss mechanisms. Consequently, not all the photons in the AM1.5G spectrum are converted into electron-hole pairs, and therefore, into J_{SC}. Thus, a simple I-V measurement alone is not sufficient to uncover the origin of these loss mechanisms in the device. One of the methods to discover and understand the J_{SC} loss mechanisms in a solar cell would be to measure spectrally resolved J_{SC} of the device. This exact goal is achieved by the external quantum efficiency (EQE) measurements. The EQE is defined as the number of electrons collected per photon incident on the solar cell [58]

$$EQE(\lambda) = \frac{n_e(\lambda)}{n_{ph}(\lambda)} = \frac{1}{q}\frac{dJ_{sc}(\lambda)}{d\Phi(\lambda)} \tag{2.22}$$

Where $n_e(\lambda)$ is the number of electrons collected, $n_{ph}(\lambda)$ is the number of photons incident, q is the elementary charge, and $d\Phi(\lambda)$ is the incident photon flux in the wavelength interface $d\lambda$ with unit cm^{-2} s^{-1} nm^{-1}. With the knowledge of EQE at every wavelength using the above equation, the $J_{SC,EQE}$ of solar cell can be computed by integrating the product EQE(λ) and $\Phi_{AM1.5G}(\lambda)$, *i.e.* the spectrally resolved photon flux corresponding to AM1.5G between the limits λ_1 (starting wavelength of EQE measurement) and λ_g (wavelength higher than the onset of EQE):

$$J_{SC,EQE} = q\int_{\lambda_1}^{\lambda_g} EQE(\lambda)\Phi_{AM1.5G}\, d\lambda \tag{2.23}$$

The AM1.5G spectrum used in this thesis is obtained from https://www.nrel.gov/grid/solar-resource/spectra.html. Thus using equation 2.23, the $J_{SC,EQE}$ of a solar cell can be easily calculated. An ideal solar cell has a step-like absorption edge, *i.e.* no absorption below the bandgap and complete absorption above the bandgap. Thus, the EQE of an ideal cell should be unity at all wavelengths above the bandgap of the absorber. However, in real solar cells, the EQE spectrum is never unity as they suffer from optical and recombination losses, as observed in Fig. 2.5. These are represented by different regions in the EQE and are very well explained in [59]. A short description of these regions is as follows:

(a) Region 1 represents the fundamental non-absorption loss. Photons having energy less than the E_G of the absorber layer are not absorbed in the solar cell. Consequently, these photons do not contribute to the J_{SC} of the solar cell.

(b) Region 2 represents the optical loss due to the incomplete generation of carriers. The band edges of a semiconductor are not abrupt due to the presence of band tails.[60] which originate from structural disorder.[61] Consequently, the absorptivity of the semiconductor is not unity near the band edges. This leads to incomplete absorption of photons, *i.e.* not all the photons are absorbed and converted into electron-hole pairs. Other than this, the region also represents the losses due to an incomplete collection of carriers generated in the quasi-neutral region absorber. Photogenerated carriers, particularly electrons due to low diffusion length or small SCR width, might recombine before they reach SCR.[45, 62, 63]

(c) Region 3 represents the optical reflection loss from the complete solar cell. Optical reflections are always present in the solar cell, causing non-absorption of a certain percentage of photons. A properly chosen ARC layer can minimize these losses to a certain extent.

(d) Region 4 represents the optical loss that incurs due to the absorption of photons in the window layers. The window layers used in this thesis to make $Cu(In,Ga)S_2$ solar cells have a bandgap of ~3.3 eV. Hence they start absorbing photons near 380 nm, causing a drop in EQE in the low wavelength (< 380 nm) region.

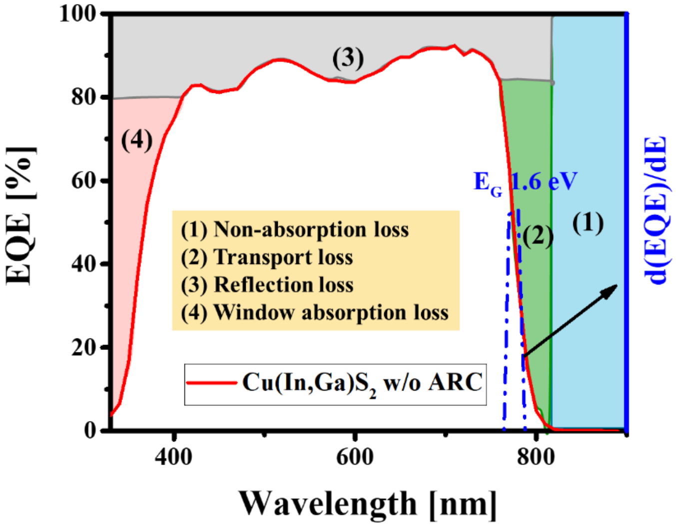


Figure 2.5: *Exemplary external quantum efficiency of Cu(In,Ga)S_2 device illustrating different optical and recombination loss mechanisms. The peak of the energy derivative of EQE yields the bandgap of the absorber.*

The EQE measurements also provide the means to calculate the bandgap energy of the absorber. While several other methods can be used to calculate the bandgap energy,[64] in this thesis, the energy derivative of EQE, *i.e.* $\frac{d(EQE)}{dE}$, is used to extract the bandgap of the absorbers. The inflection point of EQE or the peak energy of the EQE derivative is interpreted as the bandgap of the absorber.

2.1.4 Solar cell basics: Capacitance measurements

A p-n junction behaves just like a capacitor under the application of an applied bias owing to the SCR. The two ends of the SCR acts as the two parallel plates of the capacitor under depletion approximation.[49] The capacitance measurement of a device provides important information such as depth profile of doping density, built-in voltage, and, most importantly, electrical defects. This thesis contains two capacitance characterization techniques: capacitance-voltage profiling and admittance spectroscopy, referred to as "CV measurements" and AS in this work. Below is a brief introduction to these characterization techniques.

For a parallel plate capacitor, the capacitance (per unit area) is given by the ratio of relative dielectric permittivity to the distance between the two plates. In the case of a p-n$^+$ junction, the SCR width is approximately equal to the width of the depletion region on the p-region of the junction. Therefore, the capacitance of a p-n$^+$ junction is given by:[49]

$$C_{SCR} = \frac{\varepsilon_r \varepsilon_0}{x_p} \tag{2.24}$$

or

$$C_{SCR} = \sqrt{\frac{\varepsilon_r \varepsilon_0 q N_a}{2}} \left(V_{bi} - V\right)^{-1/2} \tag{2.25}$$

here equation 2.25 has been obtained by using equation 2.10 in equation 2.24, and has a voltage dependence. A plot of C^{-2} vs V, commonly known as the Mott-Schottky plot, is used to extract the carrier concentration on the p-region (N_a) and built-in voltage of the junction. The intersection of the plot with abscissa gives the V_{bi}, and the inverse of the slope gives the N_a. Under the depletion approximation, the application of voltage bias leads to capacitance response originating only from the edge of the depletion region. This fact is used to obtain a doping profile as a function of SCR width.[65] It must be kept in mind that the p-n^+ model is a strong simplification, as it ignores the capacitance contribution of the buffer, i-layer, and any capacitance in the back contact of the device.

While it seems straightforward, special care must be taken when interpreting the CV measurements to extract reliable doping density. Ideally, the Mott-Schottky plot should yield a straight line. However, it is generally not the case. A doping gradient in the chalcopyrite device from the diffusion of certain species (e.g. Cd from the buffer) or a contribution from deep defects results in a Mott-Schottky plot with varying local slope.[66] The deep defect states contribute additional charges and hence adds up to the total junction capacitance.[67] Therefore, the extracted doping density is, at best, an approximate doping density. Thus the doping density and SCR width will be referred to as apparent doping and apparent width throughout this thesis. Below, we discuss the influence of a deep state on measured capacitance. The discussion is taken from [68, 69].

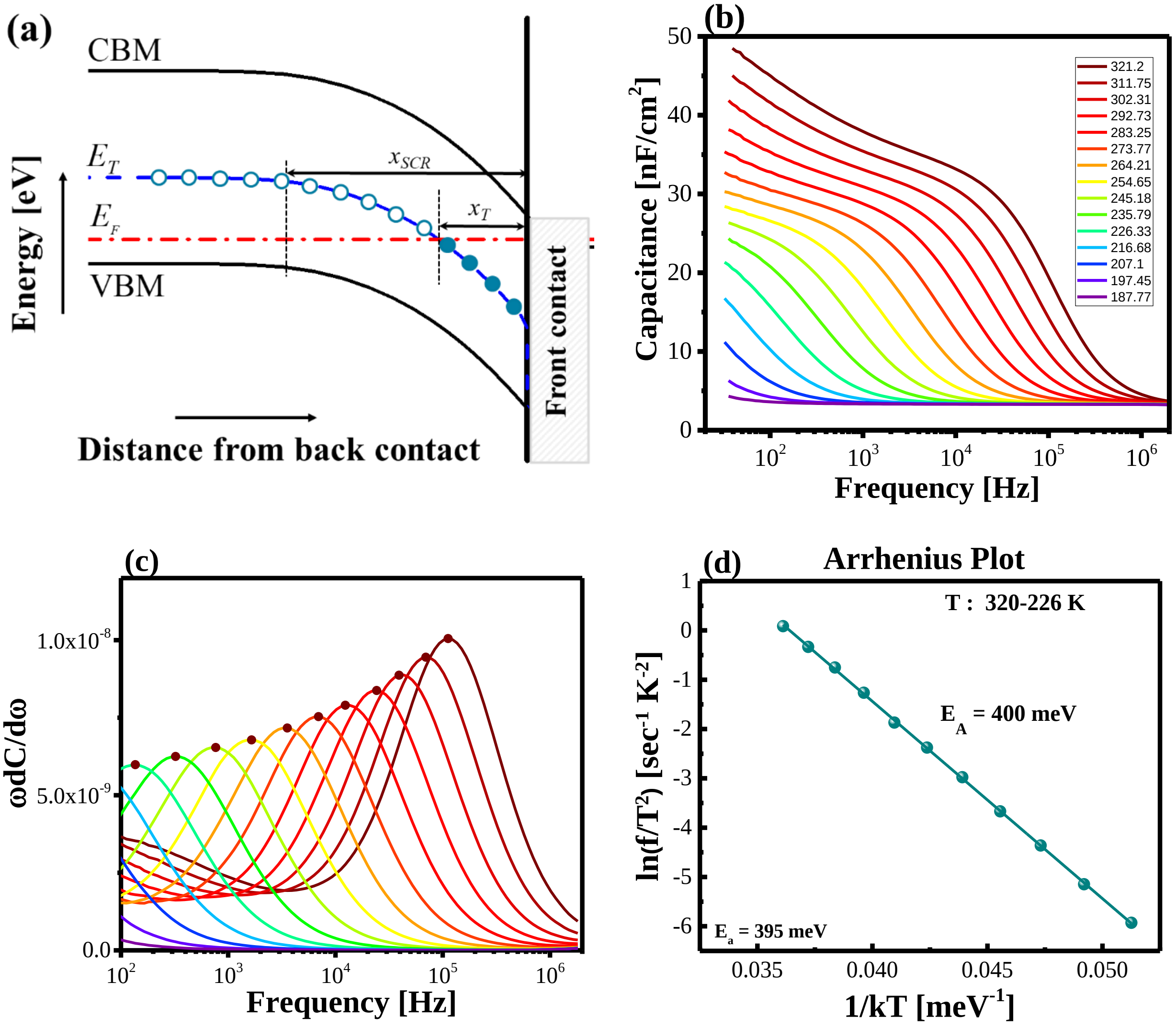


Figure 2.6: *(a) Sketch of the energy band diagram of a solar cell in the energy vs. distance scale, depicting the trap energy level E_T in blue and Fermi-level in red. At position x_T the trap level crosses the Fermi level due to band bending. (b) exemplary admittance spectra of Cu(In,Ga)S_2 device (c) derivative of the corresponding admittance spectra, the frequency corresponding to each peak (dot in the plot) gives the inflection frequency f_t (d) the Arrhenius plot corresponding to the points of the inflection frequencies which gives the activation energy of the capacitance step, which in this case is 400 meV.*

Deep defect states deep in the absorber may cross the Fermi level at a certain position (x_T) inside the SCR (see Fig. 2.6a). In thermal equilibrium, the capture rate of electron (c_n) in an empty defect state and emission rate (e_n) of the defect must be equal and is given as:[69]

$$c_n = \sigma_n \langle v_n \rangle n \quad \text{and} \qquad e_n n_T = c_n \left(N_T - n_T \right) \tag{2.26}$$

N_T is the total trap states and n_T is the occupied trap states, σ_n is the electron capture cross-section, v_n is the rms thermal velocity and *n* is the free electron density in the conduction band given by Fermi distribution. The Fermi distribution function can be used to calculate the fractional occupancy of these trap states in thermal equilibrium.

$$\frac{n_T}{N_T} = \frac{c_n}{c_n + e_n} = \left[1 + \frac{g_o}{g_1}\left(\frac{E_T - E_F}{kT}\right)\right]^{-1} \qquad (2.27)$$

and therefore

$$e_n = \gamma \sigma_{na} T^2 \exp\left(-\frac{E_A}{kT}\right) \qquad (2.28)$$

g_0 is the degeneracy of initial, g_1 degeneracy of final states, E_A is the activation energy of the trap and γ is the temperature-independent part of $N_C<v_n>$. The energetic position of the trap can be extracted once the emission rate is known, which is usually with the aid of capacitance spectroscopy. One of them is admittance spectroscopy and is described below.

Admittance spectroscopy: A solar cell circuit contains capacitive and resistive components, and therefore the application of an applied ac voltage V_{ac} is characterized by complex admittance (*Y*) of the circuit:[68]

$$Y(\omega) = G(\omega) + iS(\omega) \qquad (2.29)$$

i is the square root of -1, often referred to as 'iota' an imaginary number, *G(ω)* is conductance, while *S(ω)* is the susceptance and is related to capacitance by $S(\omega) = \omega C(\omega)$, where ω is the angular frequency of applied ac voltage pulse. Under the application of an external V_{ac} a deep trap state may contribute to the capacitance or precisely to the admittance signal, provided the frequency of the V_{ac} is low enough for the charge carriers to follow the signal.

In admittance spectroscopy, a small ac voltage ~30 mV is applied to the sample under investigation. The voltage signal results in perturbation of the Fermi level position. Assuming a trap state with energy E_T present at position x_T a few *kT* above or below the E_F, then under the application of voltage perturbation, this trap state will contribute to the total charge change of the sample under investigation. The admittance in such case is expressed as:

$$Y(\omega)=\left(1-\frac{x_T}{x_{SCR}}\right)\frac{\omega^2 g_t}{f_t^2+\omega^2}+i\omega\left[\frac{\varepsilon_r\varepsilon_0}{x_{scr}}+\left(1-\frac{x_T}{x_{SCR}}\right)\frac{f_t g_t}{f_t^2+\omega^2}\right] \tag{2.30}$$

with $$f_t = f_0\left(1-\frac{x_T N_T}{x_{SCR}N_a}\right) \quad \text{and} \quad g_t = f_0\,\frac{\varepsilon_r\varepsilon_0}{x_{scr}}\,\frac{N_T}{N_a} \tag{2.31}$$

f_o is the inverse of the time constant of the defect, f_t is the inflection frequency of the trap and g_t is the conductance due to traps. The capacitance of the device can be directly calculated from the imaginary part of equation 2.30 and is:

$$C(\omega)=\left[\frac{\varepsilon_r\varepsilon_0}{x_{scr}}+\left(1-\frac{x_T}{x_{SCR}}\right)\frac{f_t g_t}{f_t^2+\omega^2}\right] \tag{2.32}$$

with $$C_{SCR}=\frac{\varepsilon_r\varepsilon_0}{x_{scr}} \quad \text{and} \quad \Delta C=\left(1-\frac{x_T}{x_{SCR}}\right)\frac{g_t}{f_t}$$

equation 2.30 yields $$C(\omega)=C_{SCR}+\Delta C\,\frac{1}{1+\frac{\omega^2}{f_t^2}} \tag{2.33}$$

From equation 2.33, it is clear that deep defects can give rise to additional capacitance in the circuit. This capacitance step follows a step-like function with amplitude ΔC and an inflection dependent on the defect's time constant. Equation 2.31 gives the inflection frequency, for $N_a >> N_t$, f_t is equal to the inverse of the time constant of the defect and is equal to two times the emission rate, *i.e.* $f_t = 2e_n$. Hence using equation 2.28 the trap energy of a defect can be calculated.

Experimentally, the admittance is measured at different temperatures for extracting the defect energy, as shown in Fig. 2.6b. For each admittance measurement at a particular temperature, inflection frequency is extracted from the derivative of capacitance as a function of frequency, where peak maximum gives f_t (see Fig. 2.6c). These inflection frequencies are then plotted as an Arrhenius plot. The slope of the corresponding plot gives the defect activation energy (see Fig. 2.6d).

Other contributing factors: So far, we have assumed deep defects to be the only origin of the capacitance step. However, other factors such as series resistance, back contact barrier, carrier freeze-out, and interface defects may also cause a frequency dependence of the capacitance step. The influence of each of these factors on device admittance has been discussed in detail in the dissertation of T.P. Weiss [54] and references therein. Below we focus on how series and shunt resistance influence the admittance signal in an ideal device without any deep defects.

As discussed previously, a solar cell contains circuit elements such as R_s and R_{sh} in addition to the diode. The admittance of such a circuit is well described in the model given by Scofield.[70] The model assumes solar cell to be an electrical circuit comprising a capacitor 'C' in parallel to the R_{sh} together with a series resistance, as shown in Fig. 2.7. The admittance of such a circuit according to this model is given by:

$$Y_{\text{mod}} = \frac{1}{R_{sh}} \frac{1 + \frac{R_s}{R_{sh}} + \omega^2 R_{sh} R_s C^2}{\left(1 + \frac{R_s}{R_{sh}}\right)^2 + \left(\omega R_s C\right)^2} + i\omega C \frac{1}{\left(1 + \frac{R_s}{R_{sh}}\right)^2 + \left(\omega R_s C\right)^2} \tag{2.34}$$

Y_{mod} is admittance according to this model. The term 'C' is the junction capacitance and has no contribution from deep defects, as they are ignored here. As before, the complex part of equation 2.34 gives the measured capacitance, based on a simple RC model:

$$C_{\text{mod}} = \frac{\text{Im}\left(Y_{\text{mod}}\right)}{\omega} = \frac{C}{\left(1 + \frac{R_s}{R_{sh}}\right)^2 + \left(\omega R_s C\right)^2} \tag{2.35}$$

C_{mod} is the capacitance from this model, which includes the effect of series and shunt resistance. From the equation 2.35, it becomes evident that the measured capacitance values in admittance and even capacitance-voltage measurements are influenced by series and shunt resistance. For $R_s/R_{sh}<<1$, at low frequencies, C_{mod} is equal to C, and inversely proportional to R_s^2C at high frequencies. Thus, the resistive elements can clearly give rise to a capacitance step in admittance spectroscopy. Therefore, the measured capacitance must be corrected for these resistive elements to estimate junction capacitance properly. This can be achieved by the following routine: Assuming the capacitance step originates from the series resistance and not from defect state, for low frequencies, the equation 2.35 can be rearranged to the following form:

$$C = C_{\mathrm{mod}} \left[\left(1 + \frac{R_s}{R_{sh}} \right)^2 \right] \tag{2.36}$$

Therefore, by extracting series and shunt resistance from the I-V curves by I-V fit routine described in section 2.1.2, expression 2.36 can be used to correct the C_{mod} to get the true junction capacitance. Using true junction capacitance, it is then possible to determine the true doping profile of the sample with the help of equation 2.35 together with equation 2.36.

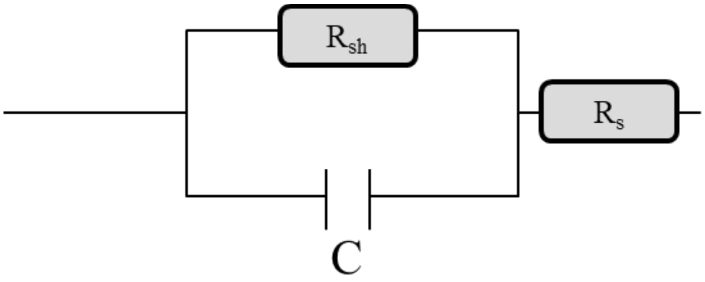


Figure 2.7: *Equivalent circuit of a solar cell containing series and shunt resistance in addition to junction capacitance.*

The usual causes of series resistance-generated capacitance steps are interface barriers at the back or the front contact in chalcopyrite solar cells. In both cases, a thermally activated series resistance leads to a step in the capacitance spectrum.[71] This capacitance step can be differentiated from the deep defect response by comparing the thermal activation energy of the capacitance step and series resistance. If both activation energies are equal, it could be possible that the capacitance step originates from series resistance and is not a deep defect.

Deep level transient spectroscopy: The deep level transient spectroscopy or DLTS,[72] is based on measurement and analysis of capacitance transients that arise during emission of charge carriers from energy levels introduced by defects. By applying a negative voltage, the space charge region expands emptying traps. A voltage pulse in the forward direction narrows the space charge region allowing charge carriers to be trapped. After removing the bias, the trapped charge carriers are emitted, which results in a capacitance transient that can be recorded and analyzed. When the carrier thermal emission rate from a trap is equal to the window rate used in the analysis, a peak in the DLTS spectrum appears. An Arrhenius plot of the used measurement time window vs. inverse temperature of the (positive or negative) maximum can then be plotted to calculate the activation energy of an energy level involved in the capture and emission of charge carriers.

Additionally, the sign of the capacitance change and thus the sign of the DLTS peak reveals whether minority (positive peak) or majority carriers (negative peak) are emitted during the analyzed process.[72]

2.2 Cu(In,Ga)S_2 and Cu(In,Ga)Se_2 solar cells

As mentioned earlier, the scope of the thesis is to explore, understand and improve Cu(In,Ga)S_2 solar cell. In this aspect, Cu(In,Ga)Se_2, which is the closest alloy system to Cu(In,Ga)S_2, plays a vital role to help understand the deficit between $V_{OC,in}$ and $V_{OC,ex}$ in Cu-rich Cu(In,Ga)S_2 solar cells as they also suffer from a similar problem. While a significant portion of this thesis deals with post-deposition treatments, buffer development and characterization of the device using electrical and photoelectron spectroscopy, the thesis could not be made possible without the absorber material, *i.e.* Cu(In,Ga)S_2 and $CuInSe_2$. All the Cu(In,Ga)S_2 absorbers used in this study were prepared by Dr. Alberto Lomuscio and Dr. Sudhanshu Shukla, whereas the $CuInSe_2$ absorbers were prepared by Dr. Hossam Elanzeery and Dr. Finn Babbe. For Cu(In,Ga)S_2 and $CuInSe_2$, two different physical vapor deposition processes were employed to prepare the absorbers. The much employed co-evaporation and molecular beam epitaxy process were used for Cu(In,Ga)S_2 an $CuInSe_2$ deposition, respectively. In the following subsection, a short description of the process is presented, and a detailed description of the process is available in work done by Lomuscio et. al.[26] and Shukla et al.[73] (for Cu(In,Ga)S_2), and Elanzeery [74] and Babbe [75] (for $CuInSe_2$).

Historical Background of Cu(In,Ga)S_2: The first solar cell based on $CuInS_2$ already dates back to 1977 with a PCE of 3.3 %.[76] The PCE grew close to 10 % within one decade, which was achieved from an n-type $CuInS_2$ absorber in an electrochemical cell. The first breakthrough above 10 % PCE was achieved by R. Scheer et al. utilizing p-type $CuInS_2$ films grown by thermal co-evaporation with as-grown film composition [Cu]/[In] > 1.[77] The introduction of Zn and Ga into the films made the efficiency of $CuInS_2$ solar cells even higher.[78, 79] A careful optimization of the deposition process and rapid thermal annealing of co-sputtered copper, indium and gallium metallic stack under H_2S environment helped S. Merdes achieve PCE close to 13 % for Cu(In,Ga)S_2,[80] which remained the highest PCE until the introduction of high-temperature growth process by Solar Frontier. Today, Solar Frontier holds the record for the highest PCE of 15.5 %. This significant leap in PCE was achieved by two important alternations: first, they used

Cu-poor as grown absorbers; second, they grew their absorbers at temperatures above 600°C significantly higher than the conventional temperature.[20, 81] Moreover, they utilized the ZnMgO buffer layer as a replacement to the traditional CdS buffer layer.[20] The prominent motive for the replacement of CdS is severe interface recombination at the absorber/buffer, (*i.e.* $Cu(In,Ga)S_2/CdS$) interface.[31, 32] Recent work by A. Lomuscio has shed light onto why barring this new record device, previous high-efficiency devices were always realized with as grown Cu-rich ([Cu]/[Ga+In]>1) composition.[21-23] His calibrated photoluminescence (PL) measurements demonstrate that the Ga free Cu-rich $CuInS_2$ absorbers have characteristic high quasi-Fermi level splitting ($V_{OC,in}$) compared to their Cu-poor counterpart.[27, 28] Moreover, a suppression in deep defect peak ~0.9 eV was observed with increasing deposition temperature.[27] However, it must be kept in mind that the solar cells obtained by these Cu-rich absorbers do not reach an external open-circuit voltage ($V_{OC,ex}$) value close to the $V_{OC,in}$ of the corresponding absorbers. This is one of the key issues that this thesis tries to address.

V_{OC} deficit in Cu-rich $CuInSe_2$ solar cells: Despite its superior morphological and high $V_{OC,in}$, the device performance of $CuInSe_2$ absorbers grown under Cu-rich conditions is known to be inferior to its Cu-poor counterpart.[39] The Cu-rich $Cu(In,Ga)Se_2$ devices are known to suffer from a low $V_{OC,ex}$ compared to Cu-poor devices,[82] causing a large deficit between V_{OCin} and $V_{OC,ex}$ in these devices.[83] Researchers have employed different post-deposition treatments to reduce this deficit. Among most successful is the treatment by Tobias Bertram, Aida Yasuhiro and others, where they utilize a thin layer (~5-10 nm) of In-Se together with an annealing step to improve the $V_{OC,ex}$ and efficiency of the Cu-rich devices to values comparable to Cu-poor devices.[84-86] Other than this, recently F. Babbe and H. Elanzeery have utilized in-situ KF treatment,[87], annealing in Se environment,[46] and chemical bath deposited (CBD) CdS or Zn(O,S) buffer layer deposited with a high sulfur concentration in the bath solution as alternate treatments that reduce the deficit between $V_{OC,in}$ and $V_{OC,ex}$.[46] In his thesis, Dr. Elanzeery linked the deficit between $V_{OC,in}$ and $V_{OC,ex}$ to the presence of 200±20 meV defect, identified as a Se-related defect in the Cu-rich device,[74] which is absent in Cu-poor devices. He identified that the defect is formed as a consequence of a strong KCN etching (10 % weight in de-ionized water).[46] Though not discussed explicitly, the defect is linked to the deep defect signature ~0.8 eV found in photoluminescence spectra of Cu-rich $CuInSe_2$ absorber.[46, 88] However, there are still some open questions regarding the defect: is the defect formed independently of the etchant used? What is the nature of the defect (is it donor or acceptor defect)? Is it just a Se-related defect or a di-vacancy (Cu-Se) complex defect? How does this defect lead to a deficit between $V_{OC,in}$ and $V_{OC,ex}$? These are some big questions which this thesis will address.

2.2.1 Band/offset at the absorber/buffer and buffer/window interface

A typical $Cu(In,Ga)(S,Se)_2$ solar cell structure presented in Fig. 2.8, consists of many interfaces due to the different layers present in the device. These layers are Molybdenum back contact, absorber layer ($Cu(In,Ga)(S,Se)_2$), buffer layer (CdS), i-layer (i-ZnO), window layer (Al:ZnO) and Ni-Al front contact. These layers play an essential role in either charge separation or charge collection. It goes without saying that buffer, i-layer and window layer materials are chosen to have a high bandgap in order to minimize the absorption losses due to these layers. Among these layers, since different buffer and i-layers are dealt with in this thesis, a brief description of their role in the device is necessary. The buffer layer, as the name suggests, protects the absorber layer against the sputtering damage and the diffusion of impurities highly conductive window layer during sputtering.[89-91] An ideal buffer layer should provide a pinhole-free coverage of the absorber layer. Other than this, if appropriately chosen, the buffer layer also provides a band alignment at the interface that reduces the interface recombination in the final device.[48] While the buffer layer is the first protective layer to prevent the absorber from sputter damage, the i-layer (highly resistive layer) is an additional protective layer that covers any pinholes that the buffer might not have covered. As a result, it reduces the shunting pathways and weak diodes that might form after window deposition.[92-94]

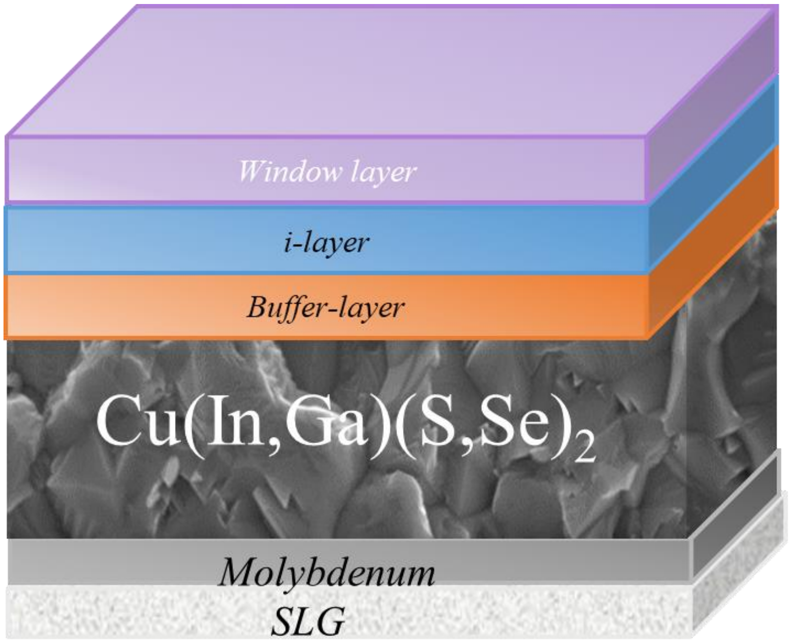


Figure 2.8: *Diagram of a Cu(In,Ga)(S,Se)$_2$ solar cell showing the structure of the device.*

In heterojunction devices, band offsets at the interface have a major impact on the device performance. Since a significant portion of this thesis focuses on Cu(In,Ga)S_2 and Cu-rich $CuInS_2$ and, a band alignment picture with CdS and Zn(O,S) buffer layer is presented based on literature reports [30, 95-98]. As there exists no unique definition, in this thesis, an interface has a positive conduction band offset (valence band offset) if the conduction band minimum (valence band maximum) energy of material on the left is lower than the material on the right, and vice-versa for a negative conduction band offset (valence band offset).

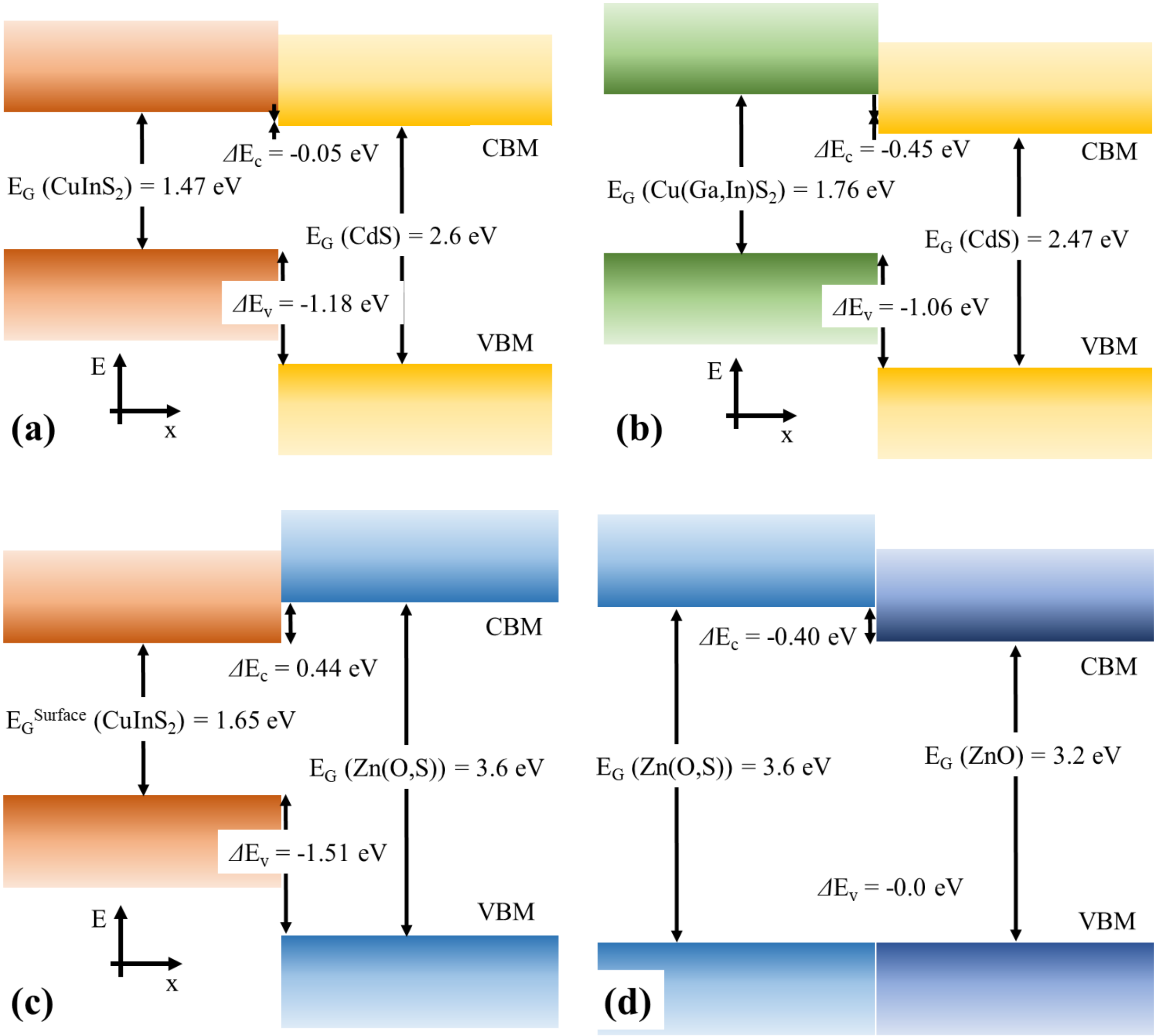


Figure 2.9: *Energy band diagram at the absorber buffer interface for (a) $CuInS_2$/CdS (b) Cu(In,Ga)S_2/CdS (c) $CuInS_2$/Zn(O,S). (d) Energy band diagram for Zn(O,S)/ZnO interface. The band diagram has been adapted from the reports [30, 95-98].*

Fig. 2.9a and 2.9b show the valence band and the conduction band offset at $CuInS_2$/CdS and Cu(In,Ga)S_2/CdS interface. The different bandgaps reported for CdS might be due to the fact that in these works the CdS is deposited *via* chemical bath deposition. And the deposited film might not be pure CdS but rather Cd(O,S). Depending upon the recipe they used, the concentration of O and S can be different in the films, as precursor concentration is known to affect the S/O ratio in the film.[99] Thereby, the deposited CdS film can have different band gaps depending upon the final S/O ratio in the film.[100] For both $CuInS_2$ and Cu(In,Ga)S_2 a negative valence band offset (VBO) is observed. This VBO acts as a barrier for the flow of holes from p to n-side of the junction and is beneficial for device performance. In the n-region, holes are minority carriers, and a barrier for holes would lead to a reduction of recombination in this region.[45] As for conduction band offset (CBO), a negative CBO is observed (Fig. 2.9b) for both $CuInS_2$ and $Cu(In,Ga)S_2$, which increases with an increase in Ga incorporation in $CuInS_2$. This form of band alignment results in an $E_{G,IF}$ with an energy value less than the bulk bandgap (E_G). A lower $E_{G,IF}$ leads to interface recombination becoming dominant. Consequently, the activation energy of recombination current decreases and therefore limits the $V_{OC,ex}$ of the device.[45] Therefore, to have a good device performance, the CBO should be within the range flat or positive so that $E_{G,IF}$ would be the same as the bulk bandgap. However, the CBO should not be higher than 0.4 eV, as the theoretical study by T. Minemoto show that the FF and J_{SC} of the device start to decrease above this value.[101] Thus, an ideal band alignment at the absorber/buffer interface would be a large cliff (negative) valence band offset and a small spike (positive) conduction band (≤ 0.4 eV).

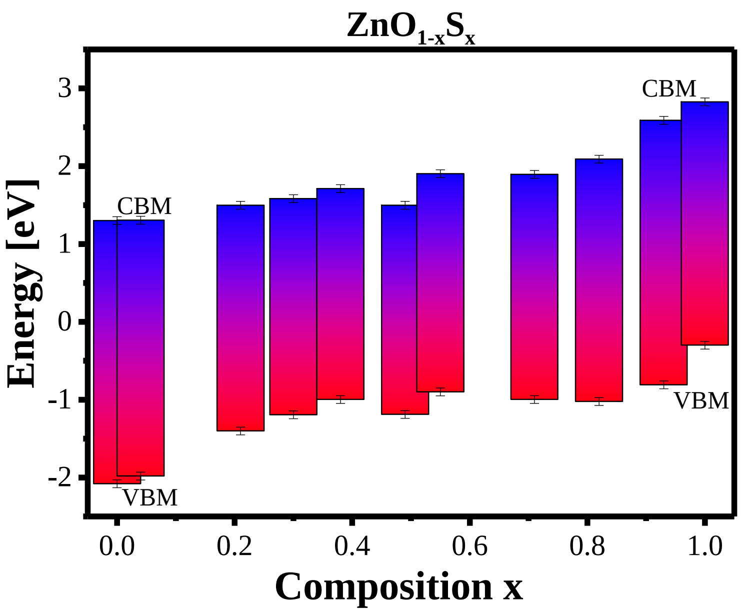


Figure 2.10: *Variation of bandgap (length of the bar), conduction band minimum (top end of the bar) and valence band maximum (bottom end of the bar) of* $ZnO_{1-x}S_x$ *as a function of composition* x. *The values are extracted from [102].*

Alternate buffer layers such as, Zn(O,S) has been utilized in the past to have optimum CBO at the absorber buffer interface (Fig. 2.9c).[96] This because, because by varying the S/O ratio, the conduction band minimum (CBM) energy and valence band maximum (VBM) energy can be tuned (Fig. 2.10),[102, 103] and hence an optimum CBO can be achieved. However, even the devices with an optimum band alignment are limited by interface recombination and will be discussed throughout this thesis. Finally, Fig. 2.9d depicts the valence band and conduction band offset at ZnO/Zn(O,S) interface, with a CBO of -0.4 eV and VBO of -0.2 eV.[97] Certainly, this value is for a particular [S]/[O+S]~0.7 ratio, since both valence band maxima and conduction band minima change with change in this ratio.[102, 103] For ZnO/CdS (not shown here) the CBO is from 0.1 eV to -0.3 eV and VBO is -0.96 eV to -1.2 eV.[104, 105] For chalcopyrite device performance, the CBO at the buffer/i-layer interface also plays an important role and will be discussed in the next sub-section.

2.2.2 Barriers in chalcopyrite solar cells

Throughout this work, we will encounter device architecture with different absorber buffer and i-layer combinations. These could lead to electrical barriers for charge transport at the absorber/buffer interface or the buffer/i-layer interface, provided the thermionic current over the barrier becomes less than the drift-diffusion current. Therefore, an elementary understanding of charge transport across these barriers is essential to the interpretation of the I-V curves and performance of solar cells. Below is a summary of how these barriers impact the device current. A more detailed description can be found in [45], which is the source of the presented discussion.

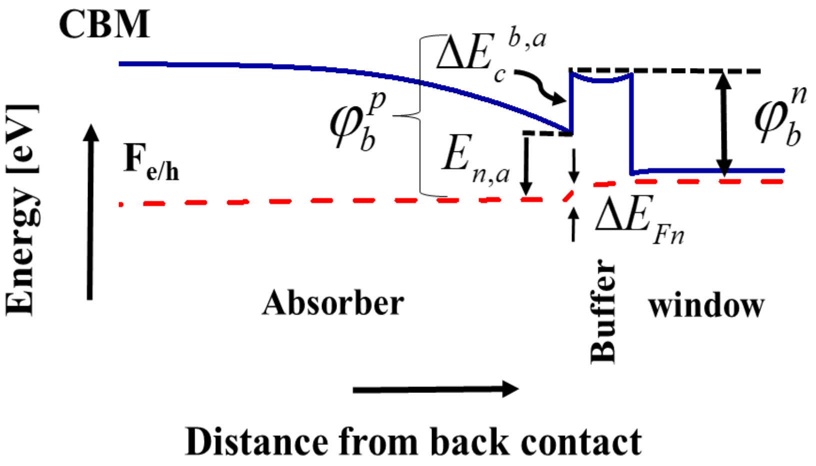


Figure 2.11: *Sketch of energy band diagram at the absorber buffer interface showing CBM and Fermi level of the device at forward bias.* φ_b^n *and* φ_b^p *are the barriers for injected and photogenerated electrons,* ΔE_{Fn} *is the drop in Fermi-level at the interface,* $E_{n,a}$ *is the position of electron Fermi-level from the absorber conduction band minima at the absorber/buffer interface and* $\Delta E_c^{b,a}$ *is the conduction band offset between the absorber and buffer. The figure is adapted from [45].*

Owing to its complex, multilayered structure and internal graded composition, thin-film solar cells often possess transport barriers other than SCR itself, which limits both diode and photogenerated current. Fig. 2.11 depicts the energy band diagram of the absorber/buffer/window layer stack (left to right) with positive CBO at the absorber/buffer interface and negative CBO at the buffer/window layer interface. Owing to the CBO at the absorber/buffer interface and buffer/window interface, there are two barriers present in the device: barrier for injected electrons (φ_b^n) from the window to absorber resulting from CBO at the buffer/window interface, and barrier for photogenerated electrons (φ_b^p) from the absorber to window resulting from CBO at the absorber/buffer interface (see Fig. 2.11).[45] Under non-equilibrium conditions, assuming thermionic emission prevails across this barrier, the total thermionic current in the device is given by: [45, 106]

$$J_{TE} = A_1^* T^2 \exp\left(\frac{-\varphi_b^n}{kT}\right) - A_2^* T^2 \exp\left(\frac{-\varphi_b^p}{kT}\right) \tag{2.37}$$

Here A_1^* and A_2^* are the effective Richardson constant for the absorber and window, T is the temperature in Kelvin, *k* is the Boltzmann constant, $\varphi_b^p = \varphi_b^n + \Delta E_{Fn}$ and at equilibrium $\varphi_b^p = \varphi_b^n$, *i.e.* the two barriers are equal. The ΔE_{Fn} is defined as the drop in electron Fermi level at the interface.[45] From Fig. 2.11 it can be seen that barrier for photogenerated carriers is equal to the sum of the position of electron Fermi-level ($E_{n,a}$) from the absorber conduction band minima at the absorber/buffer interface and the conduction band offset ($\Delta E_c^{b,a}$) between the absorber and buffer at the absorber/buffer interface, *i.e.* $\varphi_b^p = E_{n,a} + \Delta E_c^{b,a}$. Using $A^* \approx qv_{th}N_c/T^2$ [49, 106], where v_{th} is the thermal velocity of the electron and N_c is the density of states in the conduction band, and $\varphi_b^p = \varphi_b^n + \Delta E_{Fn}$ the above equation 2.37 can be re-written as:

$$J_{TE} = qv_r \left[N_{c,w} \exp\left(\frac{-\varphi_b^n}{kT}\right) - N_{c,a} \exp\left(-\frac{\Delta E_c^{b,a} + E_{n,a}}{kT}\right)\right] \tag{2.38}$$

$$J_{TE} = J_{0,TE} \left[\frac{N_{c,w}}{N_{c,a}} \exp\left(\frac{-E_{n,a}}{kT}\right)\left(\exp\left(\frac{\Delta E_{Fn}}{kT}\right) - 1\right)\right] \tag{2.39}$$

$$\text{with } J_{0,TE} = qv_{th}N_{c,a} \exp\left(-\frac{\Delta E_c^{b,a}}{kT}\right) \tag{2.40}$$

Here to derive equation 2.38, A_1^* is replaced by $qv_{th}N_{c,w}/T^2$ and A_2^* by $qv_{th}N_{c,a}/T^{2,}$ and we have assumed the same thermal velocity for both. $J_{0,TE}$ can be thought of as thermionic saturation current density, as in equation 2.39, it is the only term that remains constant for a particular structure under application of external illumination or voltage bias. From equation 2.39 it is clear that the sign of ΔE_{Fn} gives the flow of thermionic current. For a particular value of ΔE_{Fn}, any increase in the value of CBO between absorber and buffer will lead to a decrease in $J_{0,TE}$ and thereby decrease in the J_{TE}. Thus it is evident that J_{TE} can limit the J_{light} or J_{dark}, at a particular voltage or illumination condition provided the J_{TE} becomes less than the J_{light} or J_{dark}. As the barrier limits the current in the device, therefore, they can be thought of as an additional series resistance (R_B) in the device.

$$R_B = \frac{V_{ext}}{J_{TE}} = \frac{V_{ext}}{qv_r N_{c,w} \exp\left(\frac{-\varphi_b^n}{kT}\right) - qv_r N_{c,a} \exp\left(\frac{-\varphi_b^p}{kT}\right)} \tag{2.41}$$

As the barrier height φ_b^p increases, so does the series resistance in the device. A high series resistance results in a lower FF and hence lower PCE.[51, 107] As evident from equation 2.41, the R_B increases with the increase in φ_b^p $(or\ \varphi_b^n)$ and thus the FF of the device decreases (equation 2.18).

2.2.3 Metastability in chalcopyrite solar cells

The $Cu(In,Ga)S_2$ solar cells, much like $Cu(In,Ga)Se_2$ solar cell, show metastability after illumination or application of an external bias on the device.[33, 108-110] These metastabilities manifest themselves in the form of changes in electrical characteristics of the device before and after illumination or bias application, whether it be the persistent photoconductivity [109, 111, 112] or changes in current-voltage and capacitance measurements, which can last in the device from hours to days.[109, 110, 113, 114] Particularly, from a device performance point, illuminating a device for a prolonged duration with blue or red light has been known to cause metastable changes in the $V_{OC,ex}$ and FF of the device.[33, 110, 115] These metastable changes are related to $Cu(In,Ga)(S,Se)_2$ absorber alone, as devices with different buffer layers also display these changes.[116] Moreover, measurements with red light, which is not absorbed in the buffer or the window, also show these metastable changes, further supporting the argument.[117, 118] In literature, the improvement in the $V_{OC,ex}$ and FF after light soaking have been linked to two different phenomena, while the $V_{OC,ex}$ improvement is linked to a metastable increase in net carrier concentration in the absorber bulk,[113, 117] the FF improvement is related to a reduction of excessive concentration of negative charge states near the interface known as the ‘p^+ layer’.[119] Storing the device under dark reverts the carrier concentration back to the relaxed state value. The $V_{OC,ex}$ and FF is thereby reduced, and light soaking is needed to restore it. While the red light is absorbed deep in the bulk of the absorber and therefore primarily impacts the bulk, the blue light soaking impacts the region at or near the $Cu(In,Ga)(S,Se)_2$ buffer interface and is known to improve FF of the device.[114, 118, 120] In traditional devices with the CdS buffer layer, blue light is mostly absorbed in the buffer and in the front part of the absorber. Among the most commonly accepted explanation for improvement is the neutralization of acceptor defects near the interface and photodoping of buffer under blue light soaking.[121, 122] Both lead to an increase in SCR width and a decrease in the extraction barrier for the photogenerated carriers. The application of voltage bias has two distinctive impacts on the device I-V curves. While the reverse bias reduces the FF of the device, the forward bias is known to increase the FF of the device.[118] An increase in the concentration of acceptor defect in the p^+ layer during reverse bias and a decrease in their concentration during forward bias has been suggested to explain the I-V and capacitance observations among other models.[114] Recently, the changes in $V_{OC,ex}$ and FF have also been linked to changes in diode factor after illumination or bias application. It was suggested that the defects change their configuration from donor to acceptor leading to metastable changes in device I-V characteristic curves.[123]

The observed metastability in $Cu(In,Ga)(S,Se)_2$ devices is a direct consequence of defects with metastable energy levels. Point defects upon charge capture result in the formation of new energy states. These states are created because of large lattice relaxation, which mediates the transformation of the energy state near the vicinity of the defect by modifying the microscopic potential distribution near it. The most commonly evoked model is that of a Se-Cu di-vacancy complex (V_{Se}-V_{Cu}). Theoretical calculations predict a strong bond formation between neighboring atoms near the anion vacancy, *i.e.* a bond between In-In or Ga-Ga forms the bonding state, whereas the dangling In or Ga bonds form the anti-bonding states.[124] This defect complex is in its donor configuration in the bulk of the absorber. These states get converted in acceptor states upon illumination, increasing the net carrier concentration inside the absorber. On the contrary, near the interface, the complex defect is in its acceptor configuration. The photogenerated holes near the interface result in the inversion of acceptor configuration to donor configuration.

The presence of deep donor states (DX center) caused by In_{Cu} or Ga_{Cu} is also evoked as the cause of metastability in $Cu(In,Ga)(S,Se)_2$ devices.[125] The In_{Cu} point defect is an intrinsic shallow donor when present in its native substitutional configuration.[126] However, the state of this defect can be altered by the capture of two electrons, transforming it into a deep energy state (~0.3eV in $CuInSe_2$), also known as DX states.[127] A transition from this DX state to a shallow donor state thus requires overcoming a large energy barrier. Under illumination, the DX state can be reverted to a shallow donor state by the capture of photogenerated holes. The presence of DX states in $Cu(In,Ga)(S,Se)_2$ could also result in Fermi level pinning. The transformation of shallow state to DX states requires electron Fermi level to cross the energy level of DX state. This consequently pins the electron Fermi level at the energetic position of DX state. It must be noted that calculations by J. Pohl and K. Albe [128] find that the DX centers do not lead to pinning in $CuInSe_2$ and for $CuGaSe_2$ pinning level emerges at at a Fermi level of 1.16 eV above the valence edge. Therefore, it cannot be concluded whether the DX pinning state is present in $Cu(In,Ga)(S,Se)_2$ absorbers or not.

Chapter 3

Experimental details

The aim of this chapter is to provide details of the experimental procedure that are utilized to transform absorbers into the device and the characterization of the final device. This chapter addresses the experimental details of the procedure used for realizing a solar cell from the absorber to the solar cell and its characterization.

3.1 Device preparation

In this thesis $Cu(In,Ga)S_2$ and $CuInSe_2$ solar cells are partnered with CdS, Zn(O,S), ZnMgO and ZnSnO buffer layer. Physical vapor deposition methods are employed for absorber deposition. The chemical bath deposition technique is employed for deposition of CdS and Zn(O,S) buffer, whereas the atomic layer deposition technique is employed for ZnMgO and ZnSnO buffer layer deposition. For the deposition of the i-layer, *i.e.* intrinsic zinc oxide (i-ZnO) or aluminum-doped zinc magnesium oxide (Al:ZnMgO) and window layer, *i.e.* aluminum-doped zinc oxide (Al:ZnO), magnetron sputtering is employed. For nickel and aluminum (Ni-Al) contact and magnesium fluoride (MgF_2) anti-reflective coating, electron-beam evaporation was utilized.

While i-ZnO and Al:ZnO are traditional i-layer and window layer partners for chalcopyrite solar cells, the deployment of Al:ZnMgO as an i-layer and conductive transparent window layer on the solar cells was inspired from work done by Matej Hála under the project NOTO (New Optimised TCOs). A part of this work is published in [129-131] but the part regarding Al:ZnMgO deposition is not published anywhere. A summary of this work will be presented in chapter 5 where Al:ZnMgO will be introduced for the first time.

3.1.1 Physical vapor deposition of $Cu(In,Ga)S_2$ and $CuInSe_2$

Co-evaporation of $Cu(In,Ga)S_2$: Co-evaporation is a physical vapor deposition process where individual elements are evaporated onto the substrate. For the preparation of samples investigated here, three different co-evaporation growth processes were used: one-stage, two-stage and three-stage. A schematic illustration is provided in Fig. 3.1 for the three processes. In all these processes, co-evaporation of elements is executed under sulfur atmosphere by heating the alumina crucible with pyrolytic boron nitride liner, each containing copper, indium and gallium separately to a temperature above their melting points. During this deposition, the substrate (molybdenum covered soda lime glass (SLG)) temperature is fixed to a specific value depending on the growth process and the process stage. Before evaporation of any element in both one and two-stage process, a pre-sulfurization of molybdenum substrates at 590˚C is done to form a thin MoS_2 layer.

The one-stage process is utilized to prepare $CuInS_2$ polycrystalline absorber layers with both a Cu-rich and Cu-poor as grown stoichiometry. During the process after the pre-sulfurization, the substrate temperature is kept at approximately 590˚C and the metallic elements are evaporated simultaneously with a constant flux throughout the duration of deposition. A desired final stoichiometry is realised by varying the indium thermal source temperature.

The two-stage process is utilized to prepare $CuInS_2$ and $Cu(In,Ga)S_2$ absorber layers with as grown Cu-rich stoichiometry. For preparing $CuInS_2$ absorbers, during first stage after pre-sulfurization, indium sulfide precursor layer is deposited by evaporating constant flux of indium in sulphur atmosphere onto the surface of the substrate (kept at approximately 250 ˚C). Next, the indium evaporation is halted by closing the shutter and substrate temperature is ramped to 590 ˚C, after reaching this temperature, copper is evaporated in sulphur atmosphere with a constant flux onto the indium sulfide which results in the formation of $CuInS_2$. The $[Cu]/[In]>1$ stoichiometry is achieved by tuning the duration of second stage in the process. For preparing the $Cu(In,Ga)S_2$ absorbers, similar process is employed with evaporation of both indium and gallium in the first stage and only copper in the second stage. The second stage of this process aids the recrystallization of the chalcopyrite phase of $CuInS_2$ and results in increase of grain size.[132]

The three-stage process is utilized particularly to prepare $Cu(In,Ga)S_2$ absorber layers with a Cu poor as grown stoichiometry. The first two stages of this process are similar to the above two-stage process. In the first stage, indium and gallium are evaporated with constant flux onto the surface of the substrate (kept at 260˚C). In the second-stage, the both indium and gallium evaporation is halted and substrate temperature is ramped to approximately 570˚C, after reaching this temperature, copper is evaporated in sulphur atmosphere with a constant flux onto the indium gallium sulfide layer which results in the formation of $Cu(In,Ga)S_2$. During this stage to achieve better recrystallization, $[Cu]/[In+Ga]>1$ stoichiometry is achieved by tuning the duration of second stage in the process. Finally, to achieve [Cu]/[In+Ga]<1 stoichiometry, copper is evaporation is halted and gallium and indium are evaporated again. In both two and three-stage process, a change in emissivity of absorber caused by the formation of Cu_xS was used as a sign of transition to Cu-rich region in the films.[133]

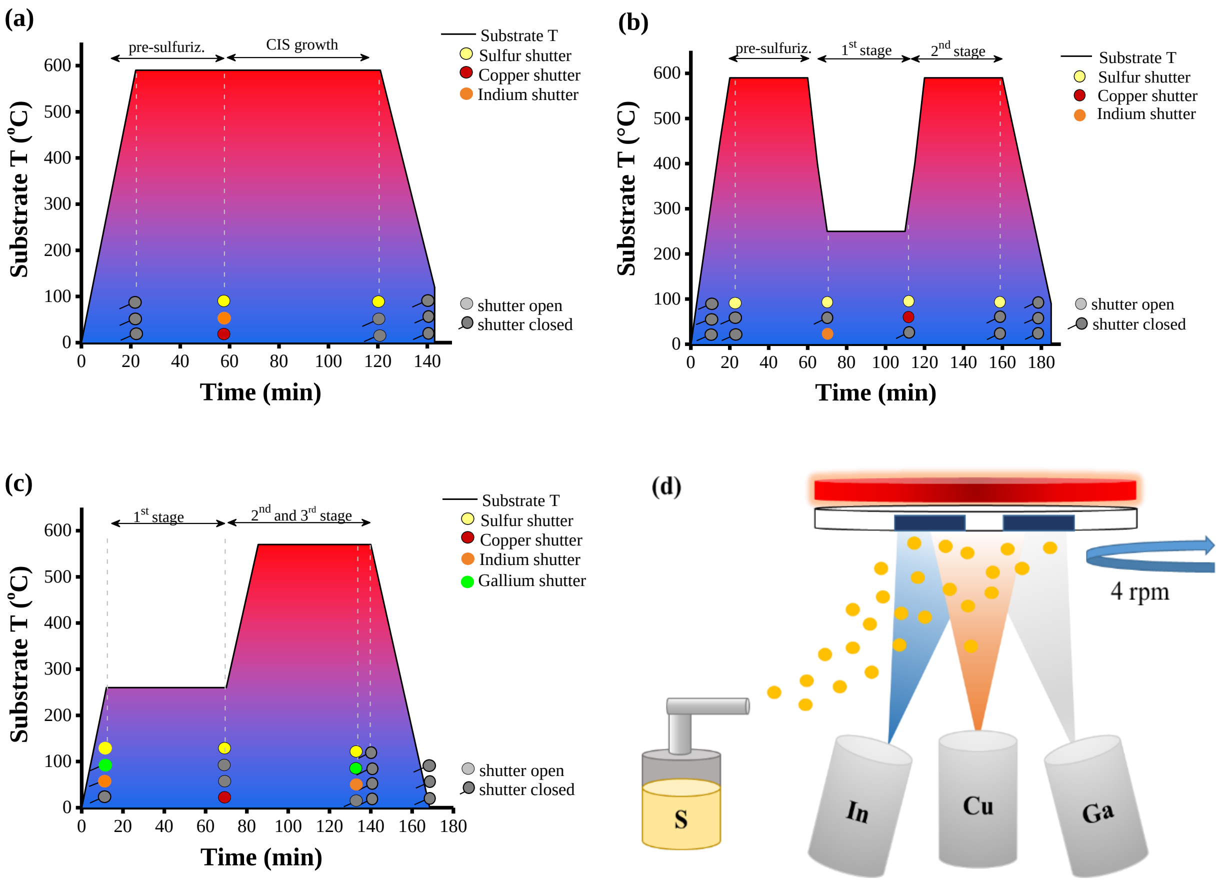


Figure 3.1: *Schematic illustration of growth process of (a) $CuInS_2$ via one-stage process (b) $CuInS_2$ via two-stage process (c) $Cu(In,Ga)S_2$ via three-stage process. (d) Representative schematic description of the deposition process.*

Molecular beam epitaxial deposition of $CuInSe_2$: For the preparation of polycrystalline thin films, $CuInSe_2$ absorbers discussed in chapter 6, a one-stage molecular beam epitaxial deposition process is utilized. In the deposition chamber, prior to film deposition, a base pressure of $2x10^{-8}$ Torr is achieved in the chamber. The copper and indium are then evaporated from effusion cells inside the physical vapor deposition chamber onto the substrates kept at 540 °C in a selenium atmosphere. The selenium flux was controlled using a valve cracker effusion cell. Different copper and indium fluxes were used to obtain 'Cu-rich' and 'Cu-poor' absorbers. The selenium flux was controlled using a valve cracker effusion cell.

3.1.2 Chemical bath deposition

Chemical bath deposition (CBD) is a commonly employed technique to deposit buffer layer for chalcogenide solar cells.[48, 134] Majority of the most recent record devices are realized with a CBD deposited buffer layer, whether it be CdS buffer layer or Zn(O,S) buffer layer.[9, 10, 135-138] In this work, CBD deposited CdS and Zn(O,S) buffer layer has been used as one of the partners of $CuInSe_2$ and $Cu(In,Ga)S_2$ absorbers. The use of Zn(O,S) is particularly important because the bandgap and hence the conduction band minima of Zn(O,S) can be tuned by adjusting the O/S ratio in the Zn(O,S) film.[102, 103]

The recipe for CdS buffer layer deposition is adapted from M.A. Contreras [139], and requires cadmium sulfate [$CdSO_4$] (2 mM), thiourea [CH_4N_2S] (50 mM) and ammonia [NH_4OH] (1.5 M). The procedure commences by first dissolving the $CdSO_4$ salt in half of the ammonia solution in a small beaker. This beaker is then covered with Parafilm tape and then ultra-sonicated for 15 seconds to dissolve the salt. This solution is then mixed with 179 ml of water, and the rest of the ammonia solution in a double-jacketed beaker maintained at 67 °C. After 30 seconds, the samples are introduced into this solution and the solution is constantly stirred using a magnetic stirrer. After three more minutes, the thiourea salt is introduced into this solution. The solution is then continuously stirred for 5-6 more minutes until the Molybdenum on the sides of the samples becomes brownish in color. At this point, the samples are taken out of the solution, rinsed with de-ionized water and blow-dried.

Two different recipes were used in this work to deposit Zn(O,S) thin films on the absorbers. The first recipe (BR1) is adapted from the work of S. Araoz and A. Ennaoui.[140, 141] The recipe has been known to produce $ZnO_{1-x}S_x$ with 'x'=0.8.[142] The recipe procedure requires zinc sulfate heptahydrate [$ZnSO_4.7H_2O$] (0.15M), thiourea CH_4N_2S (0.6M) and ammonia NH_4OH (4M). The procedure begins by mixing DI water and $ZnSO_4.7H_2O$ salt in a double-jacketed beaker. This solution then heated to and maintained at 74°C by circulating hot water under constant stirring. After 1 minute, CH_4N_2S salt is added to this solution, and the solution is allowed to heat for 3 minutes. Addition of NH_4OH follows thereafter, the samples are introduced into the bath when the white precipitates of $Zn(OH)_2$ dissolves completely. Usual deposition time is around 20 or 25 minutes yielding a Zn(O,S) layer of thickness around 30 or 50 nm.

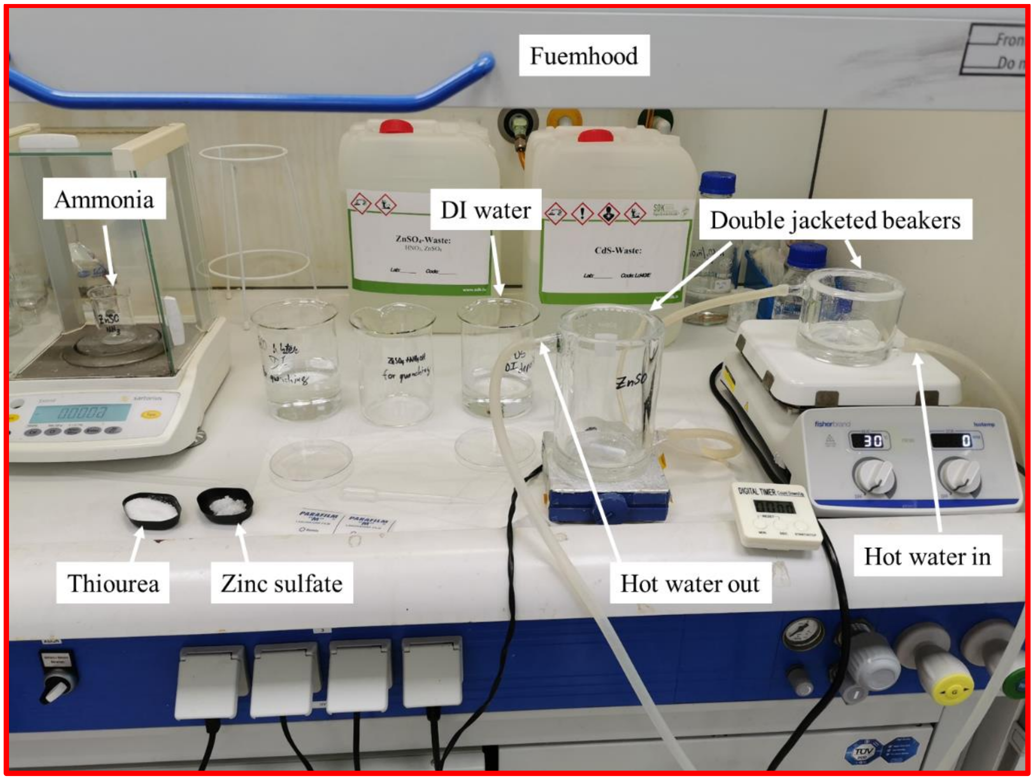


Figure 3.2: *Picture of chemical bath deposition setup showing various equipment, salts and solutions used in the process for depositing Zn(O,S) buffer layer.*

The second recipe (BR2) is adapted from C. Hubert and N. Naghavi.[143] The recipe has been known to produce $ZnO_{1-x}S_x$ with 'x'=0.7.[144] The recipe procedure requires the same reactants as for BR1, though, in a lower concentration, *i.e.* zinc sulfate heptahydrate [$ZnSO_4.7H_2O$] (0.1M), thiourea [CH_4N_2S] (0.4M) and ammonia [NH_4OH] (2M). In the process, first, two double-jacketed beakers (200 ml and 500 ml) are heated and maintained at 84°C by circulating hot water. In each of these beakers, salts of $ZnSO_4.7H_2O$ and CH_4N_2S are dissolved separately in 1/3 parts of water (total volume water used for deposition was 164 ml) and pre-heated for 10 minutes under constant stirring. After 10 minutes, the two solutions are mixed in a 500 ml single-walled beaker together with the NH_4OH. This solution is then transferred back to the bigger double-jacketed beakers. All the empty beakers, *i.e.* the single-walled beakers and the smaller double-jacketed beaker used in the last procedure, is rinsed with remaining DI water, which is then added to the main solution. Finally, the samples are immersed in the main solution, and the deposition process begins. The usual deposition time for deposition is around 10-12 minutes (or when the samples are no longer visible in the solution due to the formation of white $Zn(OH)_2$ precipitates), yielding a Zn(O,S) layer of thickness around 20 nm. The basic setup used in this procedure is shown in Fig. 3.2.

3.1.3 Atomic layer deposition

Apart from a few buffer layers, it is challenging to control the morphology and composition of chemical bath deposited buffer layers. Atomic layer deposition (ALD) has the ability to deposit controlled conformal layers with precise control on the composition of the films[145] and therefore has become popular for high-efficiency solar cell fabrication.[9, 20, 146] A short description of ALD using the review article of A.J.M. Mackus is presented ahead:[147] The deposition of thin films in ALD involves a sequence of self-terminating reactions. The ALD of binary material involves sequential steps of pulsing a reactant and co-reactant separated by purge steps, which is called a cycle. The reactant is usually a metalorganic compound containing the metal of interest, while the co-reactants are mostly H_2O, O_3, O_2 plasma.

In contrast, the ALD of a ternary material involves alternating cycles of two binary processes, called the supercycle approach. The supercycle is defined as the minimum number of cycles of individual binary materials repeated to get a mixed material over the course of the ALD process. Cycle ratio or pulse ratio is defined as the ratio of the number of cycles of one binary process in an ALD supercycle to the total number of cycles in a supercycle. For example, in a Zn_nMg_mO ALD supercycle process, the supercycle would consist of m MgO ALD cycles and n ZnO cycles in one supercycle. The pulse or cycle ratio of MgO is m/(m+n), whereas for ZnO would be n/(m+n).

In this thesis, two different ALD deposited buffers ($Zn_{1-x}Mg_xO$ and $Zn_{1-x}Sn_xO$) are used as an alternate buffer partner for $Cu(In,Ga)S_2$ absorbers. The devices with these buffer layers are discussed in chapter 4 in section 4.2. The two buffer layers $Zn_{1-x}Mg_xO$ and $Zn_{1-x}Sn_xO$ were developed respectively by P. Gnanasambandan of Luxembourg Institute of Science and Technology and T. Törndahl of Angstrom Laboratory Uppsala University.

The $Zn_{1-x}Mg_xO$ buffer deposition is carried out using BENEQ TFS 500 ALD tool. The detailed deposition is reported in [148]. As precursors, diethylzinc (DEZ), Bis(cyclopentadienyl), magnesium $Mg(Cpt)_2$ and DI water (as co-reactant) are used for ZnO and MgO, respectively, with nitrogen gas (N_2) as the carrier and purge gas. The $Mg(Cpt)_2$ precursor was heated at 75-80 °C to achieve high enough vapor pressure. The deposition of $Zn_{0.7}Mg_{0.3}O$ film is carried out at a chamber temperature of 130 °C. In contrast, deposition of $Zn_{0.77}Mg_{0.23}O$, $Zn_{0.73}Mg_{0.27}O$ and $Zn_{0.63}Mg_{0.37}O$ film is carried out at a chamber temperature of 150 °C using supercycle approach, *i.e.* alternating

ZnO cycles (DEZ/H_2O) and MgO cycles (Mg$(Cpt)_2$/H_2O) with a ratio chosen in order to give the expected composition. Two different temperatures were used, as at the time of writing this thesis, the process for $Zn_{0.77}Mg_{0.23}O$, $Zn_{0.73}Mg_{0.27}O$ and $Zn_{0.63}Mg_{0.37}O$ could not be optimized for lower temperatures. The MgO and ZnO cycles are repeated accordingly to achieve the required composition and thickness. For determining the thickness of ALD deposited ZnMgO buffer layer, a Si wafer was placed alongside the Cu(In,Ga)S_2 samples in each run, the thickness of ZnMgO film on Si wafer was then determined by ellipsometer using an effective medium approximation model.

The $Zn_{1-x}Sn_xO$ buffer layer deposition is carried out using a Microchemistry F-120 ALD tool. As precursors, DEZ, tetrakis (dimethylamino) tin (TDMASn) and DI water (as co-reactant) are used for ZnO and SnO, respectively, with N_2 as the carrier and purge gas. The deposition of $Zn_{0.8}Sn_{0.2}O$ is carried out at 105 °C and 120 °C, as temperature variation during the deposition process is known to alter the bandgap of the film,[149] and therefore, the conduction band minimum energy of the film,[150] which is required to probe the optimum band alignment with Cu(In,Ga)S_2 solar cells (discussed in chapter 4). To achieve required composition of x-value around 0.2 and thickness of 30 nm, approximately one SnO (TDMASn/H_2O) cycle and one ZnO (DEZ/H_2O) cycle were repeated 750 times. The thickness of ZnSnO layers was by x-ray reflectivity measurements performed on the fused silica glass, which was placed in the reactor together with the Cu(In,Ga)S_2 samples in each run.

3.1.4 Magnetron sputtering

Magnetron sputtering is employed for depositing transparent conductive thin films (i-layer and window layers), namely: i-ZnO, Al:ZnMgO and Al:ZnO onto buffer coated absorbers for completing solar cells. Before discussing the deposition process, it is worth discussing the prospective of Al:$Zn_{1-x}Mg_xO$ as it is unconventional to use it as an i-layer and window layer. The Al:$Zn_{1-x}Mg_xO$ can be used primarily to improve electrical transport (as it is possible to tune the CBM [151]), and secondly for high transparency in the ultraviolet (UV) region of the solar spectrum. Alloying ZnO with MgO films has been known to increase the bandgap of resulting $Zn_{1-x}Mg_xO$ from 3.2 eV (ZnO) to 7.8 eV (MgO).[152] Through photoelectron studies, T. Minemoto et al. have found that the increase in bandgap is caused by shifting of CBM of the $Zn_{1-x}Mg_xO$ towards vacuum level.[151] Thus, $Zn_{1-x}Mg_xO$ could serve as a perfect i-layer partner for Cu(In,Ga)S_2 solar cells. In our lab, Matej Hála, under the project NOTO, explored $Zn_{1-x}Mg_xO$, Al:$Zn_{1-x}Mg_xO$ as a replacement to i-ZnO and Al:ZnO in order to have better UV transparency for ZnO based transparent conducting oxides. The following is a short summary of the work done under the NOTO project.

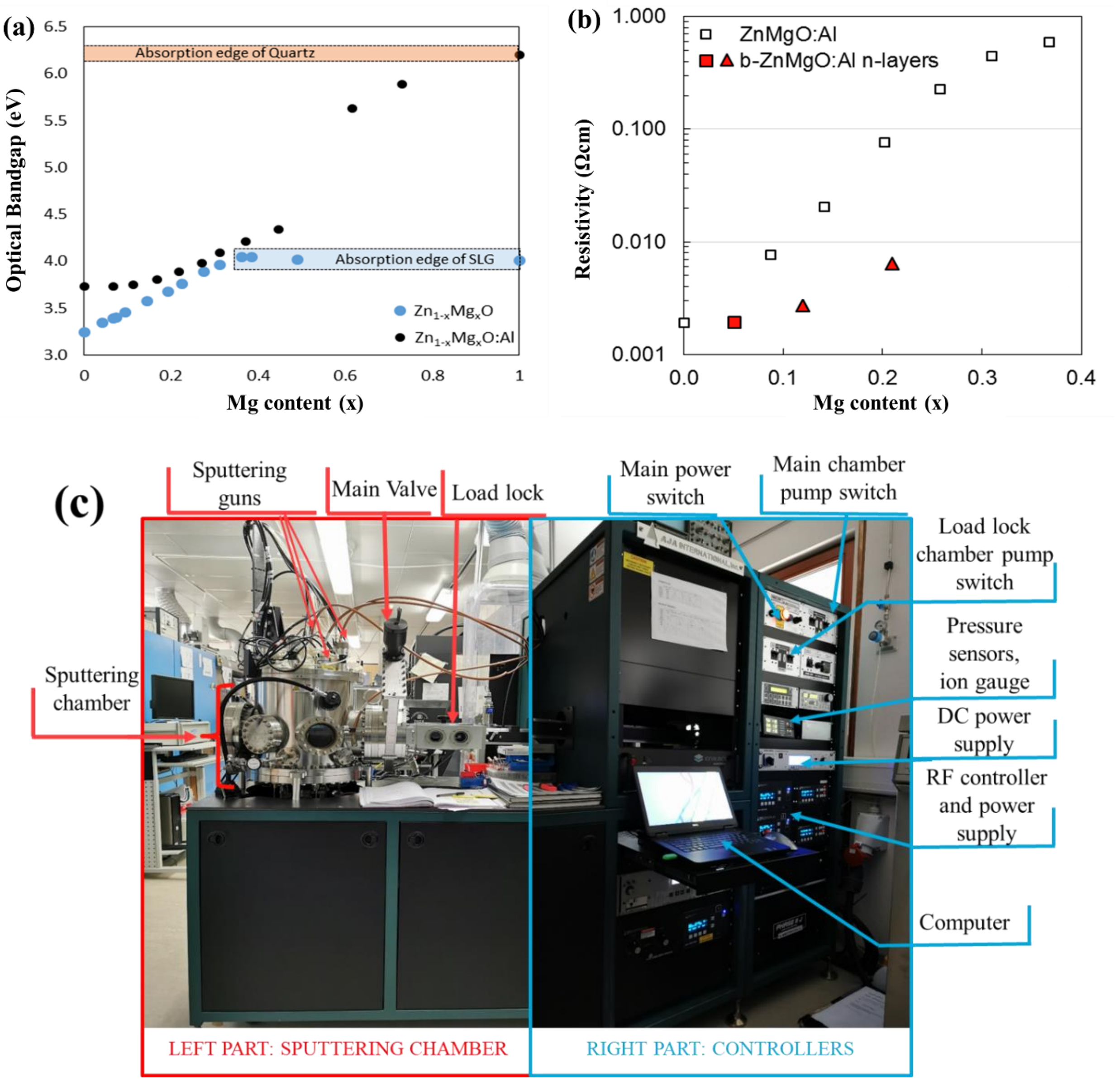


Figure. 3.3: *(a) Optical band gap as a function of Mg content in the $Zn_{1-x}Mg_xO$ and Al:$Zn_{1-y}Mg_yO$ films grown on quartz glass. The black dots stand for Al:$Zn_{1-x}Mg_xO$ films deposited by co-sputtering Al:MgO with ZnO and blue dots stand for $Zn_{1-x}Mg_xO$ films deposited by co-sputtering MgO with ZnO. (b) the resistivity of Al:$Zn_{1-x}Mg_xO$ and biased-$Zn_{1-y}Mg_yO$:Al films as a function of Mg content in the films. The empty square symbols stand for the 380 nm thick Al:$Zn_{1-x}Mg_xO$ films and the filled square circle symbols stand for the 400nm thick biased-$Zn_{1-x}Mg_xO$ films sputtered at a substrate bias of 16V and 9V respectively.[153] (c) Picture of magnetron sputtering tool used for depositing window layer.*

The $Zn_{1-x}Mg_xO$ films were prepared by co-sputtering ZnO and MgO, and Al:$Zn_{1-x}Mg_xO$ films by co-sputtering ZnO and Al:MgO. For achieving different Mg content in the films ZnO target power was set to a constant value of 125 W and MgO (Al:MgO) target power was varied to achieve different Mg content in $Zn_{1-x}Mg_xO$ (Al:$Zn_{1-x}Mg_xO$) films. Fig. 3.3a shows the absorption edge as a function of Mg content in the films, whereas Fig. 3.3b shows the resistivity of these films as a function of Mg content in the films. Clearly, Al:$Zn_{1-x}Mg_xO$ films have a higher bandgap compared to ZnO films, and depending upon whether the substrate stage is biased or not during the deposition, they display different resistivity. The difference in the resistivity of the films deposited with or without substrate biasing for a particular Mg content increases with the increasing Mg content in the films. Particularly for Mg > 0.2, both very conductive and resistive films can be obtained for the same composition. Therefore, the Al:$Zn_{1-x}Mg_xO$ films are utilized as i-layer in this thesis and window layer (in another study which is still undergoing at the time of writing this thesis). The unbiased Al:$Zn_{1-x}Mg_xO$ could help in decreasing the barrier at the buffer/i-layer, as these films have higher CBM, which reduces the CBO at the buffer/i-layer interface. This would lead to an improvement in FF and consequently the PCE of the device. In addition, the use of Al:$Zn_{1-x}Mg_xO$ as an alternate to ZnO i-layer would also improve the transparency of the device in UV region, and therefore J_{SC} and consequently PCE of the devices.

In this thesis, AJA magnetron sputtering system ORION 8 unit is used for depositing i-layer and window layer and is shown in Fig. 3.3c. The system consists of five sputtering guns: one DC and four RF guns. The system has three power sources: one for DC and two for RF. For i-ZnO and Al:ZnO deposition, undoped i-ZnO and 2 wt % Al_2O_3 doped ZnO 2-inch target were sputtered onto the samples respectively at a power of 125 W and 140 W. However, for Al:$Zn_{0.75}Mg_{0.25}O$ deposition, 2 wt % Al_2O_3 doped MgO and i-ZnO were co-sputtered at a power of 80 W and 110 W, respectively. Except for sputtering power, the deposition conditions remain the same for i-ZnO, Al:ZnO and Al:$Zn_{0.75}Mg_{0.25}O$ i-layer and window layer deposition process. First, the sputtering chamber is pumped down to a base pressure of 1×10^{-7} Torr or lower. Then the vacuum chamber is filled with argon gas (99.99 %) with a pressure of 10 mTorr. The pressure is maintained with the help of a mass flow controller. Desired composition of Al:$Zn_{0.75}Mg_{0.25}O$ was achieved by tuning the Al:MgO target power. Subsequently, a radio frequency (RF) power of 25 W is applied to the targets (to strike the targets and produce plasma inside the chamber). The targets are then ramped up to their desired power (125 W for i-ZnO deposition, 140 W for Al:ZnO deposition and 80 W and 110 W for Al:$Zn_{0.75}Mg_{0.25}O$ deposition) with a rate of 1 W/s. Finally, the argon pressure is lowered to 1 mTorr and the sample shutter is opened to start the deposition. The desired thickness of the window layer is achieved by adjusting the duration of sputtering. Although the reported powers hold true for depositions performed on absorbers presented in this thesis, in general, the sputtering power needs to be adjusted for Al:$Zn_{0.75}Mg_{0.25}O$ occasionally. This is because with each deposition, as the two targets get consumed, the sputter rate from each target changes and hence the composition of the final film. To check for the composition of grown films, every time a piece of molybdenum-coated glass is kept as witness samples, which is measured with electron dispersive spectroscopy.

3.1.5 Electron beam evaporation

To make electrical contacts on the devices, Ni-Al grids are evaporated on top of the magnetron sputtered Al:ZnO. The grids are evaporated using Oerlikon Leybold Univex 300 electron beam evaporation tool, which is shown in Fig. 3.4. The tool is also used to deposit anti-reflective coating (ARC) of MgF_2 on best devices.

For Ni-Al grids deposition, the samples covered grid mask are introduced into the bell jar. The jar is then pumped down to a vacuum of $4x10^{-5}$ Torr or lower. To achieve the desired thickness of grids (10 nm of Ni and 3 μm of Al) on the samples, Ni and Al pellets are evaporated using an electron beam. An accelerating voltage of 10 kV and a current of 72 mA and 48 mA is used respectively to evaporate Ni and Al metal pellets. The total evaporation time of the metal sources depends upon the desired thickness and is monitored using a quartz crystal monitor.

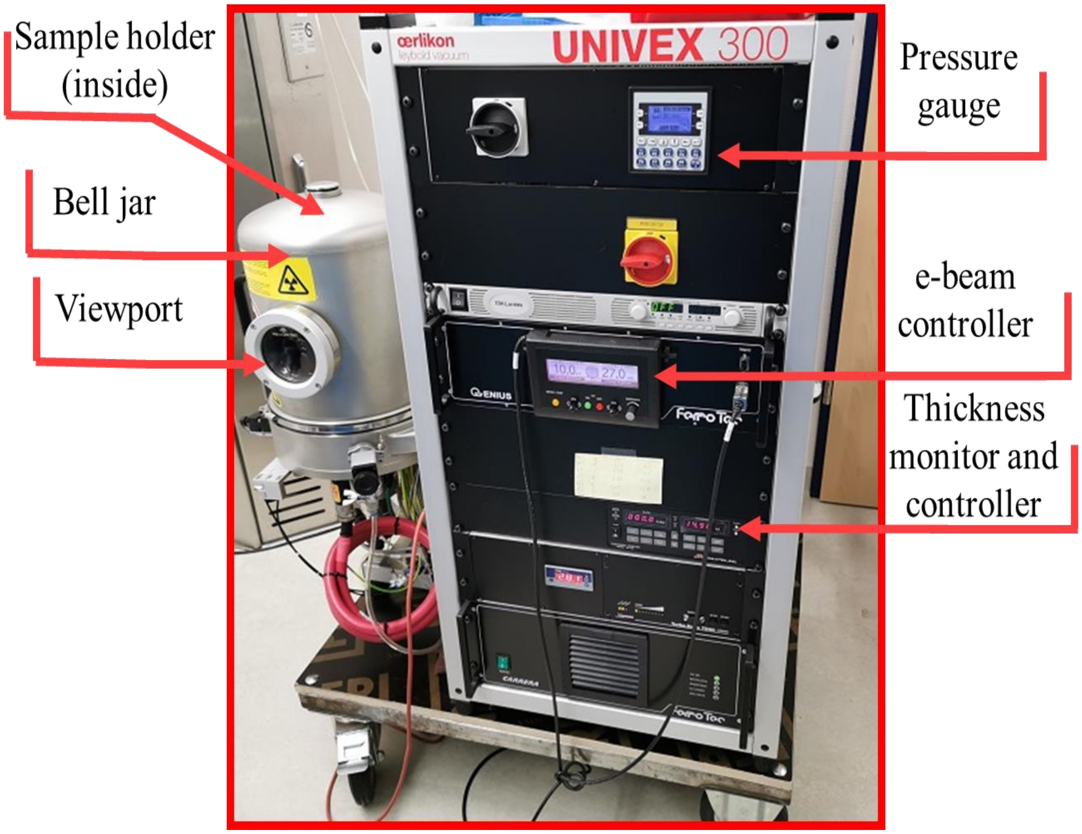


Figure 3.4: *Picture of electron-beam evaporation tool used for depositing Ni-Al grids and MgF_2 ARC.*

For coating solar cells with ARC, MgF_2 was evaporated onto the uncovered solar cells. The pellets of MgF_2 were evaporated using a relatively low accelerating voltage of 4 kV and current of 6 mA. The required thickness of MgF_2 for a corresponding solar cell was determined by equation below[154]:

$$t = \frac{\lambda}{4n} \tag{3.1}$$

where t is the required ARC thickness to minimize the reflection peak at the wavelength λ and n is the refractive index of the MgF_2 at that particular wavelength and can be found in [155]. In a device, there can be many wavelengths where the reflection is highest. However, to have maximum gain in EQE and hence J_{SC}, the thickness of ARC must be chosen for a λ where both the reflection and number of photons are highest. Fig. 3.5a shows the EQE and refection spectra of an exemplary device. In the region where the photons are absorbed by the absorber only, the reflection is maximum at a wavelength of 416 nm and 518 nm (see red curve). However, the ARC is optimized for the wavelength 518 nm because at this particular wavelength, the solar spectrum has a higher number of photons (see Fig. 3.5b). A reduced reflection at this wavelength would lead to a higher gain in J_{SC}, compared to the situation if the ARC is optimized for 416 nm.

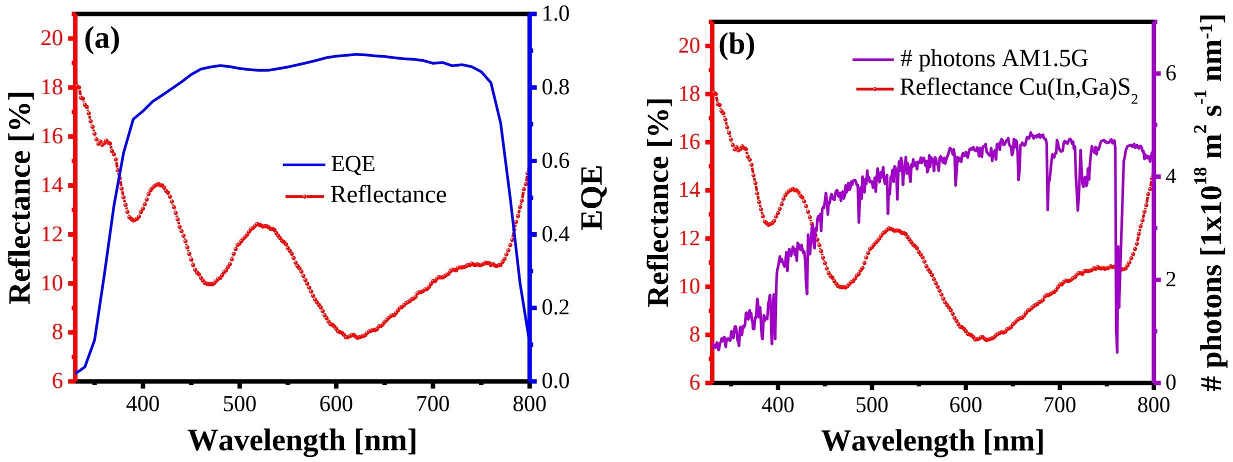


Figure 3.5: *(a) Reflectance (left in red) and EQE (right in blue) of an exemplary Cu(In,Ga)S_2 device plotted as a function of wavelength. (b) Reflectance (left in red) of an exemplary Cu(In,Ga)S_2 device plotted as a function of wavelength and number of photons (right in purple) in AM1.5G corresponding to each wavelength.*

3.2 Device characterization

3.2.1 $V_{OC,in}$ measurements

Although $V_{OC,in}$ measurements reported in this thesis were not performed by me, they are an essential part of this thesis. The $V_{OC,in}$ values are used constantly in this thesis from chapter 4-6, to calculate the interface V_{OC} deficit. Therefore, it is worth having a short summary on how $V_{OC,in}$ is measured for the samples discussed in this thesis. The detailed procedures are can be found in the thesis of Dr. Max Wolter or Dr. Alberto Lomuscio.[26, 156]

Also I would like to mention that the $V_{OC,in}$ measurements presented in this thesis were performed by Dr. Alberto Lomuscio for $CuInS_2$ and Damilola Adeleye for Cu(In,Ga)S_2.

Measuring the $V_{OC,in}$ at a given illumination (which is usually at illumination intensity equal to one sun) of a sample at a particular temperature requires the knowledge of the radiative band-to-band recombinations at that temperature. This can be achieved by absolute calibrated photoluminescence (PL) measurements.[83, 157] In our lab, these measurements are carried out in a home-built system using a steady-state excitation *via* either a CW diode laser of 405 nm wavelength for Cu(In,Ga)S_2 absorbers or a CW diode laser of 663 nm wavelength for $CuInS_2$ as the excitation source. To measure the $V_{OC,in}$, first, on the raw PL data, spectral and intensity corrections are performed. To do so, the raw PL data of the respective laser is acquired through two off-axis mirrors, which is spectrally resolved and detected using a monochromator and Si-charge coupled detector, respectively. "*Spectral and intensity corrections are subsequently applied on the raw PL data. The spectral correction is performed with a commercial calibrated halogen lamp. The intensity correction entails the measurement of the laser beam diameter with a charged-couple device (CCD) camera and the laser power by a photodiode power meter. The photon flux from the laser is calculated and adapted to the AM 1.5 solar spectrum photon flux above the bandgap, thus, an illumination corresponding to 'one sun' for the corresponding bandgap is used on the samples. The corrected spectrum is transformed into the energy domain and assessed using Planck's generalized law:[158]*

$$Y_{PL}(E) = \frac{1}{4\pi\hbar^3 c^2} \frac{a(E)E^2}{\exp\left(\frac{E - qV_{OC,in}}{kT}\right) - 1} \tag{3.2}$$

E is the photon energy, a(E) is the absorptivity of the absorber, ħ is the Planck constant, c is the speed of light, T is the temperature and C is constant containing all other constants. The above equation 3.2 describes the dependence of the absolute photon flux density (Y_{PL}) as a function of absorptivity, temperature, and $V_{OC,in}$. At energies sufficiently higher than the bandgap of the absorber, the a(E) can be approximated to unity and the above equation can thus be reshuffled to give the following form:

$$Y_{PL}(E) \approx \frac{E^2 \exp\left(\frac{E - qV_{OC,in}}{kT}\right)}{4\pi\hbar^3 c^2} \rightarrow \ln\left(\frac{Y_{PL}}{CE^2}\right) = -\frac{E - qV_{OC,in}}{kT} \tag{3.3}$$

The $V_{OC,in}$ is extracted from a fit of the high-energy wing of the semi-logarithmic plot of the Y_{PL} divided by C and E^2 where absorptivity is assumed unity and temperature is fixed to 298 K.[83] (taken directly from our manuscript [159]). Fig. 3.6a depicts exemplary calibrated PL spectra of $CuInS_2$ absorber measured using the procedure as described above, and Fig. 3.6b depicts the corresponding transformed PL spectra using Planck's generalized law and the fit to extract the $V_{OC,in}$.[157]"

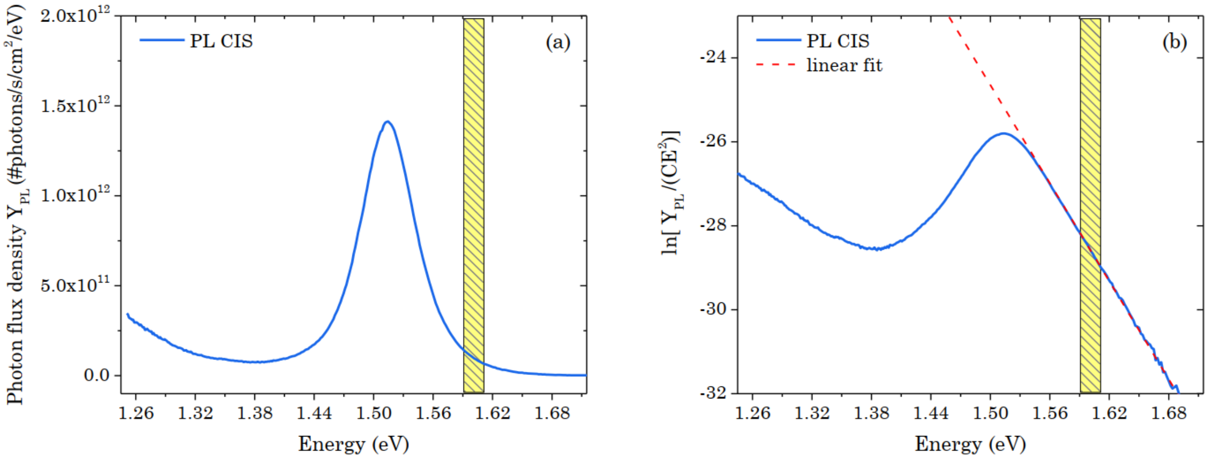


**Figure 3.6:* (a) absolute photon flux density (Y_{PL}) of a $CuInS_2$ sample plotted over energy; (b) semi-logarithmic plot of the PL flux density (divided by C which is a constant and energy squared E^2) plotted over energy together with a linear fit of the high energy wing. In both cases the fitting range is highlighted with a patterned box which lies at about 100 meV above the PL peak. (* taken from the thesis of A. Lomuscio [26]).*

3.2.2 I-V measurements

In section 2.1.2, I-V characteristic of an ideal solar cell was discussed. Fig. 3.7 shows the setup used to measure the I-V characteristic of solar cells discussed in this thesis. The setup consists of an OAI AAA solar simulator paired with a Keithley 2400 source meter. A Xenon short-arc lamp is used as the light source. The solar cell is measured by placing it on the sample stage maintained at 298 K with the help of a Peltier stage and then four-point contacts are made on the front and back contact of the solar cell. With the help of a Keithley source meter, a voltage sweep is applied on the device in the forward or reverse direction, where the forward direction means voltage sweep form a negative voltage bias to increasing positive voltage bias, usually from -0.5V to 1.0 V and reverse direction means voltage sweep in the other direction. At each voltage point, device current is recorded under dark and illumination conditions. Thus yielding the dark and illuminated I-V curve, which is used to extract I-V characteristic of solar cell. To make sure the illumination intensity is equal to AM 1.5G, the intensity of the light source is calibrated with the help of a certified reference Si solar cell. For this, the I-V characteristic of the reference cell is measured using the solar simulator. To calibrated the light source to 100mW/cm^2, the source current is set to a value that results in device I-V characteristics similar to the certified parameters. In this thesis light soaking (LS) under open-circuit conditions was also performed on some of the solar cells, as LS led to an improvement in device PCE. For this, the sample was kept on the solar simulator sample stage under AM1.5G for a desired time, and no contacts were made to keep the device in open-circuit voltage conditions.

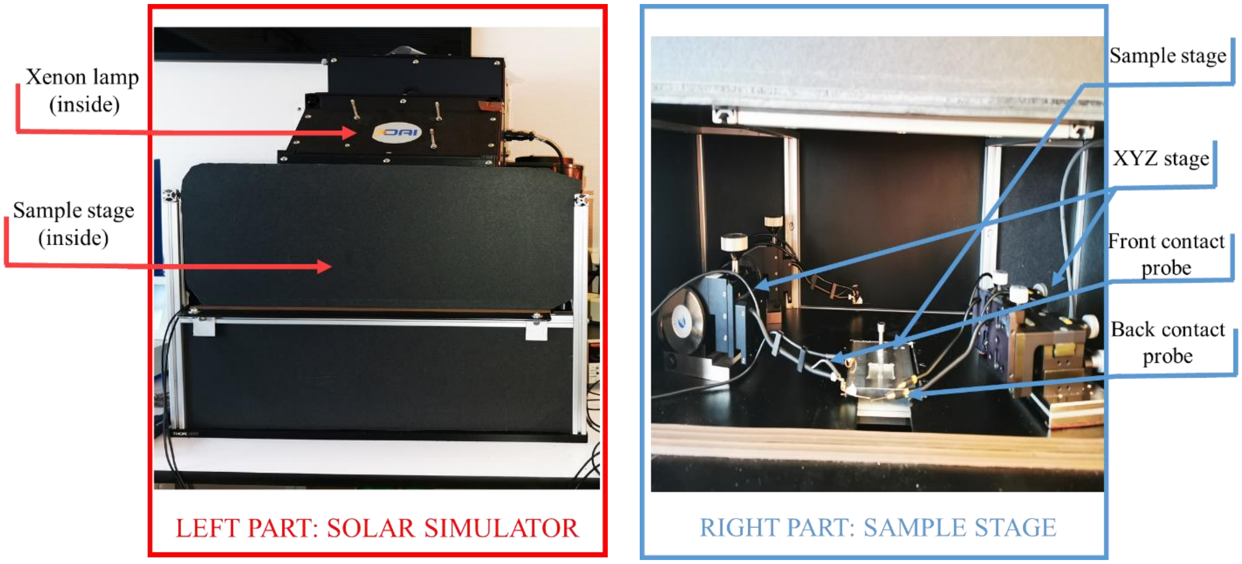


Figure 3.7: *Picture of I-V characterization setup consisting of a light source calibrated to intensity equal to 100 mW/cm*^{2}*, sample holder and 4-point contacts.*

3.2.3 External quantum efficiency measurements

Regarding the measurement setup, for solar cells discussed in this thesis, the EQE measurements were performed using a homemade QE measurement tool shown in Fig. 3.8. The system consists of Bentham lamp power sources, halogen and xenon lamps as a light source together with a Scitec optical chopper, which chops the light with a certain on-off frequency, thus leading to light with ac frequency. This is done to filter out the noise that might be produced from the artificial light. A Bentham grating monochromator is used to illuminate the sample with a particular wavelength, and SRS a lock-in amplifier is used to measure the signal. For measuring the reference spectrum of the setup, two reference detectors were used: Si-detector for wavelength region 300-1100 nm, and Indium-Gallium-Arsenide (InGaAs) detector for wavelength region 1100-1600 nm. The short circuit current of these two diodes is measured first to calculate their EQE. For this a spectral sweep of optically chopped monochromatic light in the wavelength region of interest is made, which results in a measured current at zero bias voltage. This current is transformed into voltage by a current to voltage convertor by driving it though a shunt resistor. This voltage output is then fed to the lock-in amplifier together with the synchronization output of the chopper controller as a trigger. This amplified signal is again converted back to current and then read and displayed by the computer as current and transformed EQE. The EQE transformation is done by comparing the measured current of reference diodes to already known current and EQE data of Physikalisch-Technische Bundesanstal (PTB) measured reference diode (PTB diode). PTB themselves acquires EQE data by measuring the spectral response SR (*i.e.* current produced per unit optical power incident) and transforming that into EQE using following formula:[160]

$$SR = \frac{dJ_{sc}(E)}{d\Phi(E)}\frac{1}{E} = \frac{qEQE}{E} \tag{3.4}$$

where $d\Phi(E)$ is the incident photon flux in cm^{-2}s^{-1} in the energy interval dE and dJ_{sc}(E) is the short circuit current measured corresponding that energy interval measured by PTB.

The EQE of Si and InGaAs reference detector is calculated using the SR equation as follows:

$$\frac{SR_{PTB}}{SR_{ref}} = \frac{dJ_{sc,PTB}(E)}{d\Phi(E)}\frac{1}{E} * \frac{d\Phi(E)}{dJ_{sc,ref}(E)}\frac{1}{E} = \frac{qEQE_{PTB}}{E} * \frac{E}{qEQE_{ref}} \tag{3.5}$$

$$\Rightarrow \frac{SR_{PTB}}{SR_{ref}} = \frac{dJ_{sc,PTB}(E)}{dJ_{sc,ref}(E)} = \frac{EQE_{PTB}}{EQE_{ref}} \tag{3.6}$$

$$\Rightarrow EQE_{ref} = EQE_{PTB}\frac{dJ_{sc,ref}(E)}{dJ_{sc,PTB}(E)} \tag{3.7}$$

In a similar manner as for reference diodes, the EQE of solar cell is calculated by measuring the current of solar cell by placing it on the sample stage and then making four point contacts on front and back contact of the solar cell using the equation:

$$EQE_{Cell} = EQE_{ref}\frac{dJ_{sc,Cell}(E)}{dJ_{sc,ref}(E)} \tag{3.8}$$

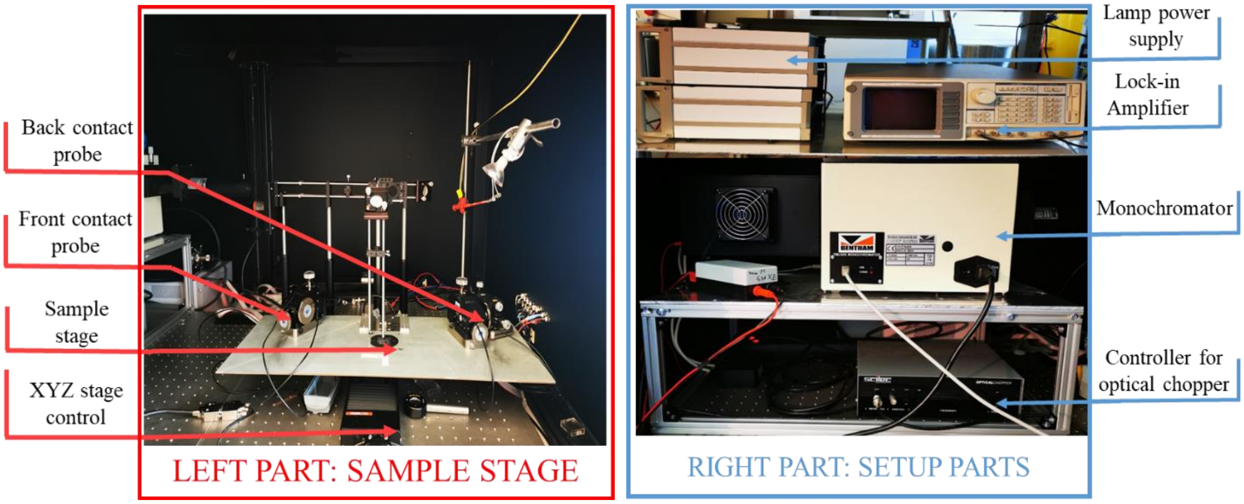


Figure 3.8: *Picture of external quantum efficiency measurement setup.*

3.2.4 I-VT and capacitance measurements

Both temperature dependent I-V (I-VT) measurements and capacitance measurements are performed in a homemade setup, which is shown in Fig. 3.9. This setup is different from the standard I-V measurements setup. The main constituents of the setup are halogen lamp, sample chamber, CTI closed cycle-cryostat, Pfeiffer vacuum pump, Agilent inductance-capacitance-resistance (LCR) meter and Keithley source meter (not shown in the figure). To measure the I-VT, the samples are mounted in a closed-cycle cryostat pumped down to a base pressure of $<4\text{x}10^{-3}$ Torr. The cold mirror halogen lamp is set to an illumination intensity equivalent to 100 mW/cm^2 by adjusting the height of the lamp from the solar cell to get the same J_{SC} as measured under the solar simulator. The temperature of the sample is controlled using a coldfinger of the cryostat located directly below the sample stage in the sample chamber. The I-V measurements at different temperatures are performed using a Keithley source meter. For the capacitance measurements, the same setup is used; just the cables of the Keithley source meter are switched with the LCR meter cables. Using an LCR meter a frequency sweep in the range f = 20 Hz to 2 MHz with a controlled small-signal ac voltage pulse of 30 mV rms is applied to the sample (sometimes under illumination with a light source or under an applied DC bias for C-V measurements), and the conductance and the capacitance are recorded. To ensure complete darkness during both capacitance and dark I-V measurements, the sample chamber is completely covered from all sides using a black cloth on the sides and a shutter on the top. An accurate determination of temperature is achieved by using a Si-diode sensor glued onto an identical glass substrate and placed just adjacent to the sample.

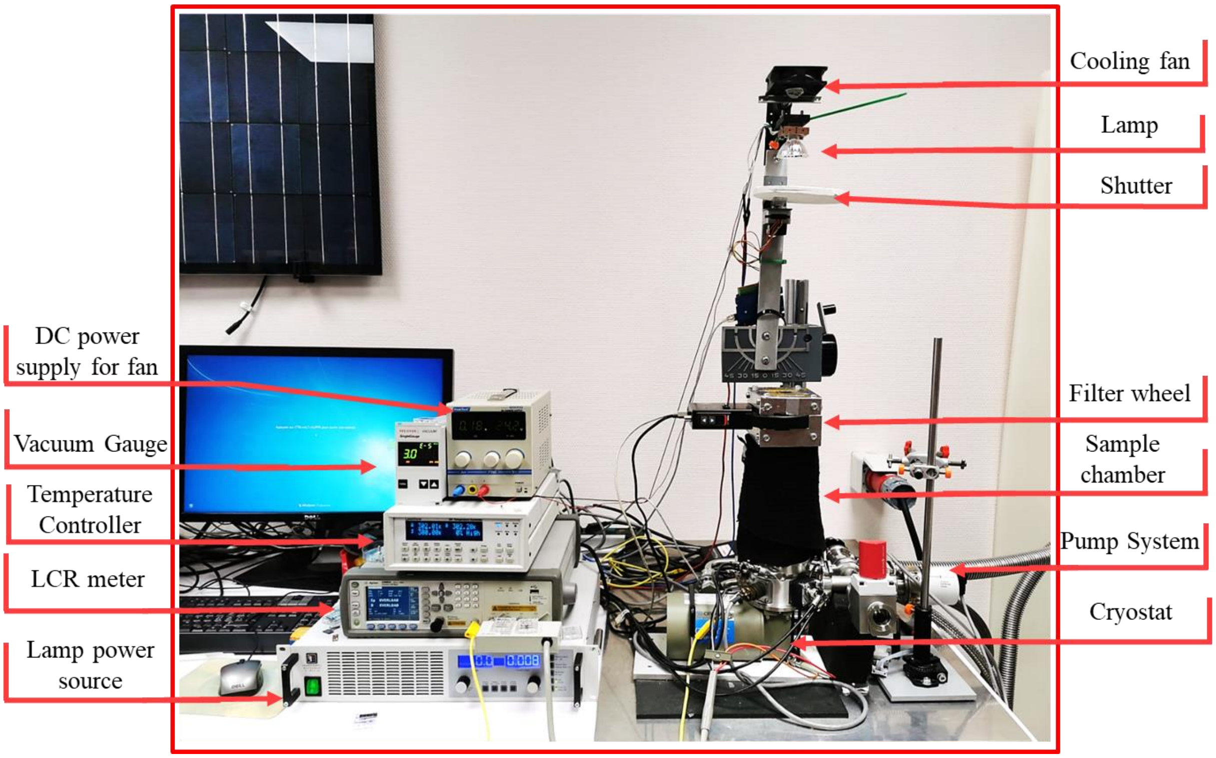


Figure 3.9: *Picture of I-VT and capacitance measurement tool showing different parts of the setup. The setup also contains a Keithley source measuring unit to measure current and voltage that is not shown in this picture.*

3.3 Photoelectron emission spectroscopy

Section 4.3 of this thesis discusses band energetic measurements for $CuInS_2$ absorber, Zn(O,S) buffer and $CuInS_2$/Zn(O,S) interface using photoelectron emission spectroscopy. The relative valence band maximum (VBM) energy, conduction band minimum (CBM) energy, Fermi level position and band bending is measured with the help of x-ray photoelectron spectroscopy (XPS), hard x-ray photoelectron spectroscopy (HAXPES), ultraviolet photoelectron spectroscopy (UPS) and inverse photoelectron spectroscopy (IPES). In photoelectron spectroscopy (PES), photons impinge onto the surface of the sample under investigation, where they interact with electrons in the sample.[161, 162] These electrons are then ejected into the vacuum *via* the photoelectric effect, where they are detected. The energy of these detected electrons depends upon the chemical state of the sample. In this thesis, three techniques are used to probe the occupied electronic states: HAXPES (~6 keV), XPS (~1.25 keV), which can excite and probe both the core and valence states with an energy resolution of ~0.2 eV to 0.9 eV and the UPS (5-100 eV) can excite and probe only the valence states. Due to a lower energy resolution of the HAXPES and XPS (~0.2 eV to 0.9 eV), these techniques are used to probe only the core levels of the samples, whereas the valence band is probed with UPS due to a higher energy resolution (0.1 eV). On the contrary, in the IPES, the conduction band or the unoccupied states in the sample are investigated by injecting electrons of varying kinetic energy from an electron gun. The injected electrons relax to unoccupied conduction band states where they radiatively recombine and release a photon. The energy of this photon is measured w.r.t. to Fermi level energy.[163]

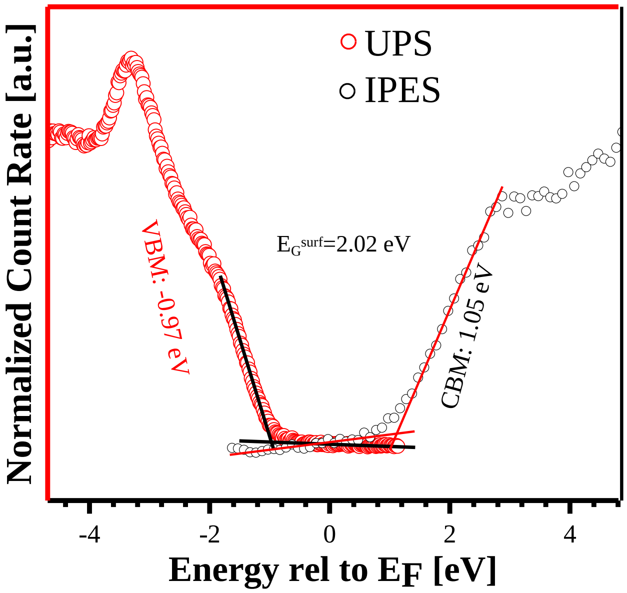


Figure 3.10: *Exemplary UPS and IPES spectra of $CuInS_2$ used to extract the VBM and CBM values. The linear portion of the valence (conduction) band is extrapolated to the baseline line. The intercept on the baseline gives the energy of the valence band edge (conduction band edge) w.r.t. the Fermi level.*

To probe the band alignment at the interface, a two-step procedure is followed: first the VBM (CBM) of the absorber and buffer surface, *i.e.* $CuInS_2$, Zn(O,S) surface, is measured with respect to (w.r.t.) Fermi level using UPS (IPES). This is done by extrapolating the steep linear edge of the valence band (conduction band) to the baseline, for example see Fig. 3.10. Next, since the band bending due to junction formation leads to a shift in VBM (CBM) position from the Fermi level near the surface and in XPS (HAXPS), the core level binding energy of all the elements shifts with the band bending.[164] Therefore, with the help of the XPS (HAXPS) measurements, interface induced band bending (IIBB) is measured to compensate for this shift. This is accomplished by measuring the core-level binding energy of the sample before buffer deposition (to get core-level energy of $CuInS_2$ without IIBB), and with a thin (to get core-level energies of $CuInS_2$ and Zn(O,S) with IIBB) and a thick Zn(O,S) buffer deposition (to get core-level energy of Zn(O,S) without

IIBB). An increase in core level binding energy suggests downward band bending, whereas a decrease in core level binding energy suggests upward band bending. The VBO (CBO) can therefore be extracted using the formula:[165]

$$\mathrm{VBO} = \mathrm{VBM}_{\mathrm{Zn(O,S)}} - \mathrm{VBM}_{\mathrm{CuInS_2}} - \mathrm{IIBB}$$

$$\mathrm{CBO} = \mathrm{CBM}_{\mathrm{Zn(O,S)}} - \mathrm{VBM}_{\mathrm{CuInS_2}} - \mathrm{IIBB}$$

Where subscripts correspond to $CuInS_2$ and Zn(O,S), with the sign convention of VBM < 0 and CBM > 0 w.r.t. Fermi level which is the reference point, *i.e.* zero energy point.

In the following, a short description of the setup used to measure the band alignment at the $CuInS_2$/Zn(O,S) is provided. Jakob Bombsch of Helmholtz-Zentrum Berlin für Materialien und Energie GmbH performed all the photoelectron measurements.

3.3.1 XPS and UPS measurements

Laboratory excitation sources Specs XR 50 Mg K_α (1253.56 eV) and Prevac VUV5000 He II (40.8 eV) were used for XPS and UPS measurements. A ScientaOmicron Argus CU electron analyzer was used to detect the photoelectrons and analyze the spectrum. An experimental energy resolution of 0.9 eV was achieved for Mg K_α source by setting the pass energy for the core level detail spectra to 20 eV. An energy resolution of approximately 0.1 eV was achieved for the He II measurements by setting the pass energy to 4 eV. The grounded Au foil was used for both XPS and UPS binding energy (BE) calibration by referencing the Au $4f_{7/2}$ peak to the binding energy of 84.00 eV and the Fermi edge of Au foil to the binding energy of 0.00 eV, respectively. The XPS, UPS and IPES analysis of samples was done in a chamber with base pressure 5×10^{-9} mbar.

In addition to XPS and UPS measurements, HAXPES experiments were also performed on $CuInS_2$/Zn(O,S) samples at the National Institute for Materials Science (NIMS) contract beamline BL15XU1 of the Super Photon ring-8 GeV (Spring-8) electron storage ring.[166] An excitation source having photon energy 5.95 keV, which was calibrated using the Si (111) crystal of a double crystal monochromator, was used to obtain the HAXPES spectra. An experimental energy resolution of 0.25 eV for all HAXPES spectra by setting the pass energy for the core level detail spectra to 200 eV. A grounded clean Au foil was used for binding energy calibration by referencing the Fermi edge to the binding energy of 0.00 eV.

3.3.2 IPES measurements

Inverse photoelectron spectroscopy (IPES) measurements were performed using a Kimball Physics Inc. EGPS-1002E electron gun with BaO coated filament and an OmniVac IPES1000 channeltron-based counter. IPES spectra were recorded in isochromat mode (*i.e.* using a bandpass filter to measure photons of constant energy, varying the energy of the incident electrons) with the detected photon energy calibrated to 6.69 eV using the Fermi edge of a clean, grounded Au foil. The kinetic energy of the electrons used for excitation was swept from 5-15eV in 0.1 eV steps with a total dwell time (*i.e.*, time per energy at each scan) of 20 s/step.

3.4 Numerical simulations: SCAPS-1D

In section 2.1 we have seen that a solar cell can be described by drift and diffusion equations. These equations can be solved numerically to simulate the behavior of a solar cell under a certain set of conditions. For this, the highly proclaimed solar cell capacitance simulator (SCAPS-1D) is used in this thesis, which solves the one-dimensional Poisson and continuity equation for electron and hole, using appropriate boundary conditions at the interface and the contact. The software is developed at the Department of Electronics and Information Systems (ELIS) of the University of Gent, Belgium, under Marc Burgelman.[167] It can simulate electrical characteristics of a solar cell such as I-V, EQE, capacitance-voltage (C-V), capacitance-frequency (C-f) curves, band diagrams, carrier generation and recombinations and even more.

Simulating the electrical characteristics of a device requires the following steps:

1. Launch the SCAPS-1D software (freely available online). After launching the program, the user interface pops up (Fig. 3.11).

2. To simulate the device, the structure of the solar cell needs to be defined. For this user need to input the layers included in the device structure by clicking on the ‘set problem’ button. Apart from left and right contact, SCAPS allows inserting 7 layers in one solar cell structure and 6 interfaces.

3. After defining the layers, accurate optical and electrical material parameters must be inserted corresponding to each layer. These parameters can be found in the literature.


SCAPS 3.3.10 Action Panel

Working point
Temperature (K) 300.00
Voltage (V) 0.0000
Frequency (Hz) 1.000E+6
Number of points 5

Series resistance: yes / no; 1.00E+0 Rs Ohm.cm^2
Shunt resistance: yes / no; Rsh 1.00E+3; Gsh 1.00E-3 S / cm^2

Illumination: Dark Light

Spectrum file name: AM1_5G 1 sun.spe
Short wavel. (nm) 200.0
Long wavel. (nm) 4000.0
Transmission (%) 100.000
Neutral Density 0.0000
Incident (or bias) light power (W/m2): sun or lamp 0.00; after cut-off 0.00; after ND 0.00

G(x) model: Constant generation G
Ideal Light Current in G(x) (mA/cm2) 20.0000
Transmission of attenuation filter (%) 100.00
Ideal Light Current in cell (mA/cm2) 0.0000

Action					number of points		
☐ I-V	V1 (V)	0.0000	V2 (V)	0.8000	41	0.0200	increment (V)
☐ C-V	V1 (V)	-0.8000	V2 (V)	0.8000	81	0.0200	increment (V)
☐ C-f	f1 (Hz)	1.000E+2	f2 (Hz)	1.000E+6	21	5	points per decade
☐ QE (IPCE)	WL1 (nm)	300.00	WL2 (nm)	900.00	61	10.00	increment (nm)

Problem file: new problem

SCAPS 3.3.10 Solar Cell Definition Panel

illuminated from : right / left
apply voltage V to : left contact / right contact
current reference as a: consumer / generator

Layers: left contact (back); CIGSu; ZnMgO; ZnO; Al-ZnO; add layer; right contact (front)

Interfaces: CIGSu / ZnMgO

Info on graded parameters only available after a calculation

Problem file
c:\Program Files (x86)\Scaps3309\def\
CIGSu no grading ALD manuscript.def
last saved: 3-8-2021 at 8:41:16

Remarks (edit here)
SCAPS 3.3.10 ELIS-UGent: Version scaps3310.exe, dated 10-04-2021, 11:22:08 Problem defini
last saved by SCAPS: 03-08-2021 at 08:41:16

This problem definition file has been distributed with all SCAPS versions since SCAPS 2.0, 1998
Here this old def file is saved in the format now used by SCAPS2.8 .

Figure 3.11: *The user interface of SCAPS-1D, on top, is the action panel and on the bottom is the cell definition panel where solar cell structure is defined.*

4. SCAPS can simulate the device at various working conditions such as different temperatures, voltage bias, frequency and illumination intensity. Therefore proper working conditions at which the user wants to simulate the device properties must be set to get desired device characteristics.

5. Finally, the in ‘action’ panel-specific action such as simulating I-V, EQE, C-V or C-f curve needs to be specified. Once all this is done, simulation can be done by clicking on the ‘Calculation: single shot’ button in the interface, which runs the program.

In this thesis, two types of solar cells are simulated $Cu(In,Ga)S_2$ solar cell (Chapter 5) and $CuInSe_2$ (Chapter 6) solar cells. The device parameters to simulate them are reported in appendices 5 and 6.

Other software which are available but not used in this thesis are AMPS (Analysis of Microelectronic and Photonic Structures), PC1D (personal computer 1-dimensional simulator), AFORS-HET (automat for simulation of Heterostructure) and ASA (Advanced Semiconductor Analysis).

Chapter 4

$Cu(In,Ga)S_2$ solar cell

Most of the results presented here have been published by us in [73] or are under review [159]. Some of the text has been taken verbatim from these manuscripts and has been marked clearly using a different font style.

4.1 Interface V_{OC} deficit in $Cu(In,Ga)S_2$

4.1.1 Cu-rich $Cu(In,Ga)S_2$ vs. Cu-poor $Cu(In,Ga)S_2$: Influence of buffer layer

The absorbers used to prepare Cu-poor $Cu(In,Ga)S_2$ devices in this section were grown using the 3-stage growth, whereas for the Cu-rich $Cu(In,Ga)S_2$ absorbers, the 2-stage growth process was preferred due to its superior morphology compared to the 1-stage process (see Fig. A4.1a). These absorbers were subjected to the necessary KCN etching, *i.e.* a 10 % KCN etching for 5 minutes for Cu-rich absorber and a 5% KCN etching for 30 seconds for Cu-poor absorber before depositing CdS and Zn(O,S) buffer layers. Since it is possible to produce $Cu(In,Ga)S_2$ absorbers with similar $V_{OC,in}$ under the Cu-rich and the Cu-poor conditions (see Fig. A4.1b), in order to have a fair comparison, the Cu-rich and the Cu-poor absorbers with similar optoelectronic quality, *i.e.* $V_{OC,in}$ and E_G were preferred. The absorbers were transformed into the devices with either Zn(O,S) buffer layer (BR1) or CdS buffer layer together with standard i-ZnO and Al:ZnO window layer (as explained in section 3.1). Since the devices prepared with Zn(O,S) buffer recipe used here displayed signs of electrical barriers, devices with CdS buffer were also prepared. Because, as discussed in section 2.2.1, CdS and Zn(O,S) have a different band alignment at the absorber buffer interface with $Cu(In,Ga)S_2$. Therefore, it could help differentiate between electrical barriers at the absorber/buffer interface, from the barrier present elsewhere in the device, such as; the back contact barrier, barrier due to conduction band grading (see section 4.2.4) present in the device, and help comprehend the I-V characteristics of the device better.

The devices with Zn(O,S) buffer were subjected to annealing on a hot plate at 200 °C for 10 minutes under a fume hood. This is done because high-temperature air annealing is known to improve the device performance of the Cu-poor $Cu(In,Ga)Se_2$/Zn(O,S) devices.[168, 169] For the devices presented here also, annealing improves the device performance (see table A4.1). However, it has a dramatically different impact on the $V_{OC,ex}$ of the devices: for the Cu-rich Cu(In,Ga)S_2/Zn(O,S) device, the $V_{OC,ex}$ decreases (Fig. A4.2 and table A4.1), something that has been observed for Cu-rich $CuInS_2$ solar cells prepared with Zn(O,S) buffer layer (see Fig. A4.1c) and even with Cu-rich $CuInSe_2$ solar cells prepared with CdS buffer layer as well[170], whereas for the Cu-poor Cu(In,Ga)S_2/Zn(O,S) $V_{OC,ex}$ increases (see table A4.1).

Fig. 4.1a and b show the I-V characteristics of the best Cu-rich and Cu-poor Cu(In,Ga)S_2 devices, respectively. The I-V parameters of the best devices along with the measured $V_{OC,in}$ values are summarized in table 4.1. In general, the Cu-poor Cu(In,Ga)S_2 devices possess a higher J_{SC}, $V_{OC,ex}$ and FF, and therefore, a higher PCE, as compared to their Cu-rich counterparts (table 4.1) independent of the buffer layer used. The devices also have a low deficit between the $V_{OC,in}$ and $V_{OC,ex}$ suggesting a better translation of $V_{OC,in}$ into device performance (see Fig. 4.1c). Among the Cu-poor devices, the Zn(O,S) buffer layer device exhibits a PCE of 9.5 %, whereas the CdS buffer layer device exhibits slightly lower PCE ~8.5 %. The higher PCE can be majorly attributed to a higher J_{SC} and $V_{OC,ex}$ despite the low FF possessed by the device, compared to the CdS device. The higher J_{SC} in the Zn(O,S) device can be understood easily by observing the EQE spectrum of the two devices (see Fig. 4.1c). Compared to the CdS device Zn(O,S) device exhibits a higher EQE response in the blue region. The CdS device, due to absorption by the CdS buffer layer below 520 nm, results in a lower EQE response in the blue region. Consequently, the Zn(O,S) device possesses a higher J_{SC} compared to CdS device. The lower FF in Zn(O,S) device originates from the rollover present in the first quadrant of the I-V curve, which is a sign of barrier for injected electrons φ_b^n and is absent in CdS device. As discussed in section 2.2.2, this barrier results in an additional series resistance element in the device, which leads to a lower FF. The Cu-rich devices show very poor device performance, which is majorly due to a very high deficit between $V_{OC,in}$ and $V_{OC,ex}$, suggesting poor translation of $V_{OC,in}$ into electrical performance.

Among the Cu-rich devices, the Cu(In,Ga)S_2/CdS buffer layer device performs better in all aspects compared to the Cu-rich Cu(In,Ga)S_2/Zn(O,S) device unlike the Cu-poor devices, where the opposite is true. Surprisingly, the Cu-rich Cu(In,Ga)S_2/Zn(O,S) device does not display the rollover in the I-V curve, unlike its Cu-poor counterpart. However, despite this, the device has a poor FF along with a poor J_{SC} and $V_{OC,ex}$., which might be due to high recombinations in the device.

Moreover, the EQE of this device is relatively low compared to other devices (see Fig. 4.1c), which could also be a sign of high surface recombination in the device.[171]

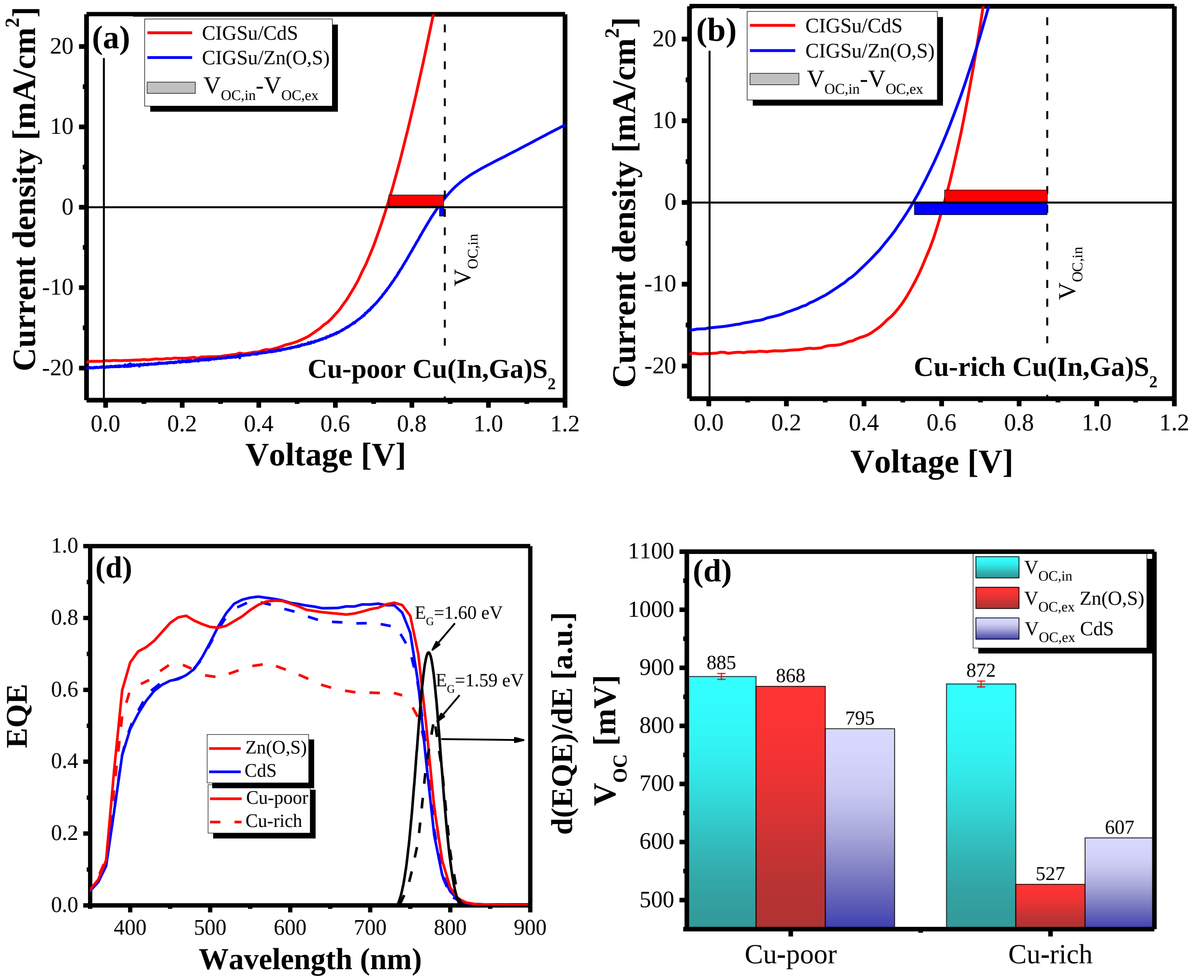


Figure 4.1: *I-V curve of Cu(In,Ga)S_2 device prepared with (a) Cu-rich absorber and (b) Cu-poor absorber with different buffer layer (c) EQE of the corresponding devices. (d) Bar of $V_{OC,in}$ of bare Cu(In,Ga)S_2 absorber and $V_{OC,ex}$ of best Cu(In,Ga)S_2 device.*

Table 4.1: *I-V characteristics of best Cu-rich and Cu-poor Cu(In,Ga)S_2 device with either Zn(O,S) or CdS buffer layer. The reported $V_{OC,in}$ values are extracted from calibrated PL measurement on the absorbers without any buffer coating on top as explained in section 3.2.1.*

	PCE (%)	FF (%)	J_{SC} (mA/cm^2)	$V_{OC,ex}$ (mV)	$V_{OC,in}$ @1sun (mV)	$V_{OC,in} – V_{OC,ex}$ (mV)	$E_G – E_a$ (meV)
Cu-poor/Zn(O,S)	9.5	54.9	19.9	868	885	17	0
Cu-poor/CdS	8.5	60.7	19.1	732	885	153	180
Cu-rich/Zn(O,S)	3.5	42.6	15.4	527	872	345	610
Cu-rich/CdS	6.7	59.7	18.5	607	872	265	430

Although all the devices possess similar $V_{OC,in}$, they have very different $V_{OC,ex}$ and as a consequence, a different deficit between $V_{OC,in}$ and $V_{OC,ex}$ (see Fig. 4.1d). From table 4.1, it becomes clear that the performance of a solar cell depends heavily on the deficit between the $V_{OC,in}$ and $V_{OC,ex}$. Moreover, as this deficit decreases the PCE increases, showing just how crucial it is for device performance. Since $V_{OC,in}$ measurement provides the information regarding the recombination processes in bulk but fails to capture the details at the interface as observed by Babbe et al.[87], it might be that the deficit between $V_{OC,in}$ and $V_{OC,ex}$ originates from the interface recombinations. Therefore, to comprehend the root cause of the deficit, the I-VT measurements were performed to reveal the dominant charge carrier recombination mechanism in the devices as explained in section 2.1.2. Fig. 4.2a and b shows the $V_{OC,ex}$ measured at different temperatures (dots in the figure) and the linear extrapolation of $V_{OC,ex}$ to 0 K, which gives the E_a for the dominating recombination path in the device (see section 2.1.2). For Cu-poor Cu(In,Ga)S_2/Zn(O,S), the temperature-dependent $q{\cdot}V_{OC,ex}$ extrapolates to the E_G of the absorber (obtained from $\frac{d(EQE)}{dE}$ analysis see Fig. 4.1c [64]), suggesting interface passivation and a device that is dominated by bulk recombination. However, for the Cu-poor Cu(In,Ga)S_2/CdS, Cu-rich Cu(In,Ga)S_2/CdS and Cu-rich Cu(In,Ga)S_2/Zn(O,S) the $q{\cdot}V_{OC,ex}$ extrapolates to a value less than the $E_{G,}$ giving activation energy (E_a) of 1.42 eV, 1.16 eV and 0.98 eV, respectively. As discussed in section 2.1.2, when E_a value is less than the E_G, it suggests that these devices are dominated by interface recombinations. For CdS devices, it is not surprising, as photoelectron studies have predicted cliff at the Cu(In,Ga)S_2/CdS interface[95, 98]. Assuming the devices do not suffer from Fermi-level pinning, the E_a values of these devices should correspond to their respective $E_{G,IF}$ (as explained in section 2.1.2). Therefore, from the predicted value of cliff in these studies ~0.4-0.5 eV[95, 98], it can be inferred that the CdS devices should have an $E_{G,IF}$ and therefore E_a ~1.1-1.2 eV. However, this is only true for Cu-rich CdS devices and not for Cu-poor CdS devices (see Fig. 4.2).

For the Cu-rich Zn(O,S) device, it is surprising that the E_a is not equal to the E_G. Assuming the surface bandgap is the same for the Cu-rich and Cu-poor Cu(In,Ga)S_2 absorber, the Cu-rich Zn(O,S) device should also have an E_a equal to the E_G. As they both should have same band alignment, and therefore, the same interface bandgap. This of course, assumes that there is no Fermi-level pinning in the device. In fact, similar observations have been made for Cu(In,Ga)S_2 devices prepared with ZnMgO buffer layer (see Fig. A4.3 in appendix) and also for Cu(In,Ga)Se_2 with CdS buffer layer,[32] where Cu-poor devices have an E_a equal to the E_G. In contrast, Cu-rich devices have an E_a less than the E_G. The above observations suggest that all Cu-rich Cu(In,Ga)S_2 devices either have different band alignment at the absorber/buffer interface than Cu-poor Cu(In,Ga)S_2 devices or they suffer from Fermi-level pinning. In light of these results, it is safe to say that there is a need to probe the energetic band alignment at the Cu(In,Ga)S_2/buffer interface to have a clearer picture of the band alignment. Other than this, it seems that the deficit between $V_{OC,in}$ and $V_{OC,ex}$ is directly correlated to the deficit between the E_G and E_a, because as one increases, so does the other (see table 4.1). This makes it fairly evident that the deficit between $V_{OC,in}$ and $V_{OC,ex}$ is directly related to interface recombinations in the device. Since it is now established that the V_{OC} deficit is caused by interface recombinations, henceforth, in this thesis, this deficit will be referred to as interface V_{OC} deficit.

A deeper investigation is required to understand why Cu-rich Cu(In,Ga)S_2 or, for that matter Cu-rich chalcopyrite solar cells suffer from interface recombination even though prima facie they seem not to suffer from negative CBO at the absorber/buffer interface. We will do so in the following chapters. For now, we will focus on improving the PCE of Cu-poor Cu(In,Ga)S_2 devices further.

To summarize: the Cu-poor Cu(In,Ga)S_2 devices possess a low interface V_{OC} deficit, particularly with the Zn(O,S) buffer layer, whereas Cu-rich Cu(In,Ga)S_2 devices possess a high interface V_{OC} and consequently a lower PCE compared to Cu-poor devices. All devices except the Cu-poor Cu(In,Ga)S_2/Zn(O,S), suffer significantly from interface recombinations. The Cu-poor

Cu(In,Ga)S_2/Zn(O,S) device, does not suffer from interface recombinations and consequently has the highest $V_{OC,ex}$ and highest PCE.

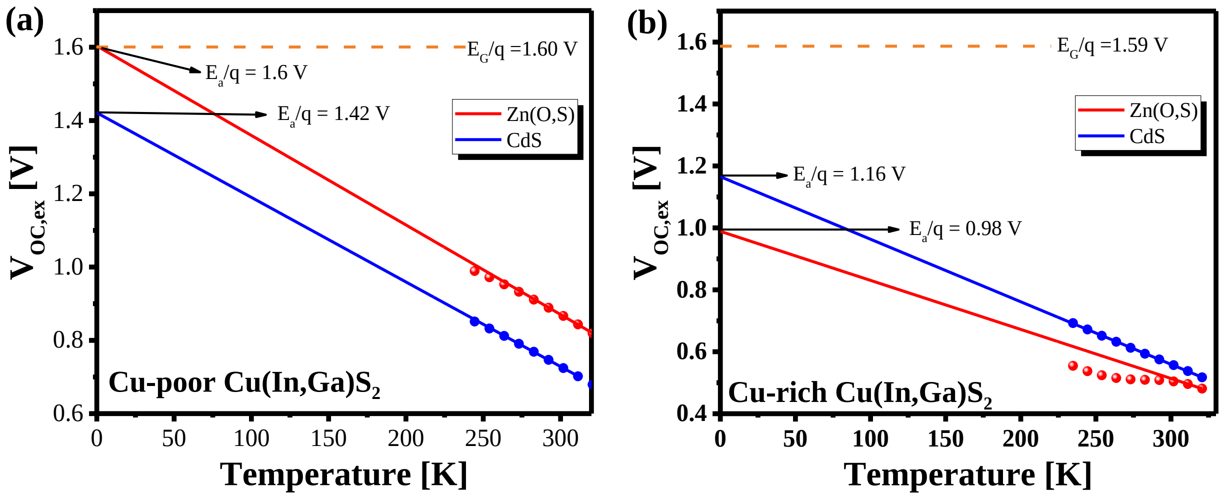


Figure 4.2: *$V_{OC,ex}$ plotted as a function of temperature for (a) Cu-poor (b) Cu-rich Cu(In,Ga)S_2 devices with Zn(O,S) and CdS buffer layer.*

4.1.2 High-efficiency Cu-poor Cu(In,Ga)S_2 device with Zn(O,S) buffer

Based on the earlier results on Cu-poor Cu(In,Ga)S_2 device, another batch of the device was fabricated to have high-efficiency devices. Since the best Cu-poor device suffers from low FF, probably due to a high barrier for injected electrons φ_b^n (Fig. 2.12a), an alternate i-layer with higher CBM was explored to improve the FF. Three devices were made: 1. Cu(In,Ga)S_2 with Zn(O,S) (BR1) buffer and ZnO i-layer, 2. Cu(In,Ga)S_2 with Zn(O,S) (BR1) buffer and Al:$Zn_{0.75}Mg_{0.25}O$ i-layer, and for comparison purpose only 3. Cu(In,Ga)S_2 with CdS buffer layer and ZnO i-layer. The procedure for preparing the devices is exactly the same as explained in section 3.1. Devices 1 and 2 were annealed at 200 °C on a hot plate for 10 minutes under a fume hood in the air immediately after buffer deposition and prior to i-layer deposition. In contrast, no annealing was performed for device 3, as it deteriorates the PCE of the device (see table A4.1). Unlike the devices discussed at the beginning of this section, the annealing was performed prior to the i-layer deposition because annealing of the full device leads to unwanted rollover in the first quadrant (see Fig. 4.1a and Fig. A4.2). However, annealing the device before i-layer deposition seems to solve the problem. Annealing also has a significant impact on the $V_{OC,in}$ of the device. While the deposition of Zn(O,S) buffer layer does not alter the $V_{OC,in}$, annealing the device after buffer deposition leads to a significant drop ~26 mV in $V_{OC,in}$ (see Fig. A4.4).

The I-V characteristic curves of three devices are presented in Fig. 4.3a. It must be noted here that the devices display light soaking and hysteresis behavior in I-V curves, *i.e.* different I-V characteristic curves when in the forward measurement direction and reverse measurement direction (for example, see Fig. A4.5). Therefore, the curves presented here are measured in the reverse direction after 30 minutes of light soaking under open-circuit voltage conditions as this gives the best PCE (for measurement direction definition and light soaking procedure, see section 3.2.2). In fact, all the devices studied in this thesis displayed light soaking and hysteresis behavior. Therefore, only the best I-V curves are presented, which is usually after 30 minutes of light soaking measured either in forward or reverse measurement direction. Among all the devices, the Zn(O,S) device prepared with Al:$Zn_{0.75}Mg_{0.25}O$ i-layer displays superior I-V characteristics (J_{SC}, $V_{OC,ex}$, FF and consequently PCE) over all other device (see table 4.2). For devices prepared with i-ZnO i-layer, the CdS device possesses significantly higher FF, which can be attributed to lower buffer/i-layer CBO at the interface (as discussed in section 2.2.2 and see discussion in section 4.2.4).

Moreover, as expected CdS device exhibits a high ~90 mV interface V_{OC} deficit. Comparatively, other devices exhibit a lower but still a significant interface V_{OC} deficit: 35 mV for device prepared with Zn(O,S)/i-ZnO structure and 50 mV for the Zn(O,S)/Al:ZnMgO structure. This despite the $q \cdot V_{OC,ex}$ extrapolates to E_G of the Cu(In,Ga)S_2 for Zn(O,S) devices (see Fig. 4.2a). In fully optimized Cu(In,Ga)Se_2 solar cells, the interface V_{OC} deficit is less than 10 mV,[172] whereas, in devices with non-optimized transport layers that do not suffer from interface recombination, the deficit can be 60 mV,[83] close to what is observed here for Cu(In,Ga)S_2 devices prepared with Zn(O,S) buffer layer.

Moreover, while device 1 with i-ZnO layer exhibits a PCE of 12 %, device 2 with Al:ZnMgO i-layer exhibits a PCE of 14 % without the ARC, *i.e.* a relative 16 % gain in efficiency, which mainly originates from a 19 % higher FF compared to the device 1 with ZnO i-layer. With a ~95 nm thick MgF_2 ARC layer on device 2, the PCE increases further to 15.1 % (see Fig. 4.3b). Barring the world record device from the Solar Frontier group, this is the highest ever reported efficiency for Cu(In,Ga)S_2 device. The gain in the device PCE after ARC coating comes from improvement in J_{SC} and FF of the device (see table 4.2). The necessary annealing step after buffer deposition causes the degradation of absorber optoelectronic quality, resulting in a $V_{OC,in}$ loss of about ~26 mV in the device (Fig. A4.4). Moreover, due to non-optimized contacts an $V_{OC,ex}$ ~26 mV is lost (as $V_{OC,ex}$ loss = Interface V_{OC} deficit – $V_{OC,in}$ loss). The two losses together lead to an interface V_{OC} deficit of ~52 mV. If these losses can be avoided to an extent in the fully optimized devices, a $V_{OC,ex}$ of 40 mV can be gained, and consequently, a device with a PCE ~ 16 % can be achieved.

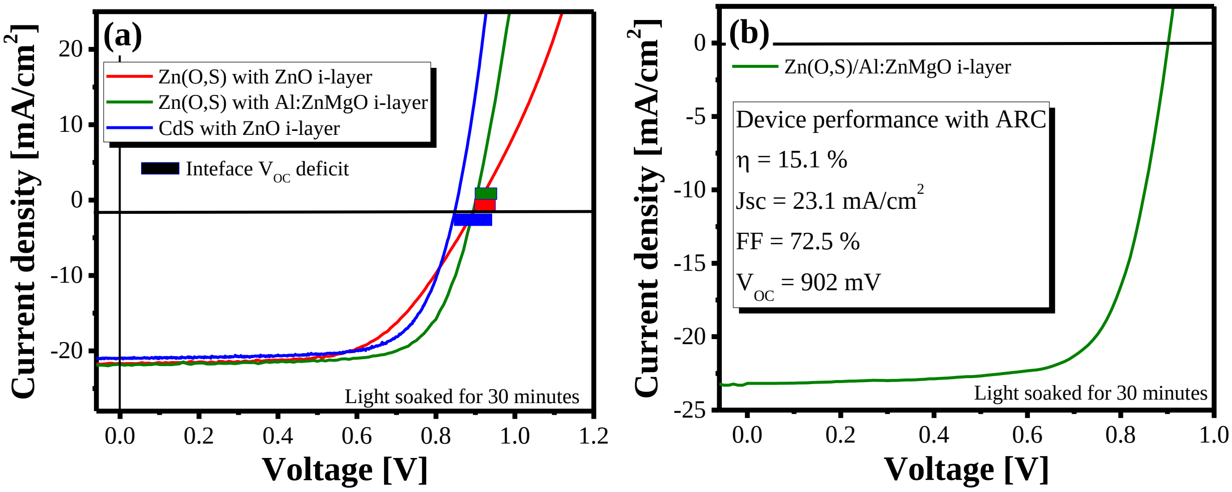


Figure 4.3: *(a) I-V characteristic curves of $Cu(In,Ga)S_2$ device prepared with CdS buffer layer and standard ZnO and Al:ZnO i-layer in blue, in red, is the device with Zn(O,S) buffer and ZnO i-layer, and in olive is the device with Zn(O,S) buffer and Al:ZnMgO i-layer. For all the devices Al:ZnO transparent conducting oxide layer is used as the window layer. (b) I-V characteristic curve of the $Cu(In,Ga)S_2$ device prepared with Zn(O,S) buffer and Al:ZnMgO i-layer after ~95 nm MgF_2 ARC coating. All the curves presented in this figure are after light soaking for 30 minutes.*

Table 4.2*: I-V characteristic of best $Cu(In,Ga)S_2$ devices made with CdS and Zn(O,S) buffer. For Zn(O,S) buffer, two different i-layer were used, for one device i-ZnO and for the other Al:ZnMgO. The reported $V_{OC,in}$ values are extracted from calibrated PL measurement on the absorbers without any buffer coating on top as explained in section 3.2.1.*

Buffer layer	**i-layer**	**PCE (%)**	**FF (%)**	**J_{SC} (mA/cm^2)**	**$V_{OC,ex}$ (mV)**	**$V_{OC,in}$ @1sun (mV)**	**$V_{OC,in}$ -$V_{OC,ex}$ (mV)**
CdS	ZnO	12.8	71.6	21.0	854	942	88
Zn(O,S)	ZnO	12.0	60.6	21.7	912	947	35
Zn(O,S)	Al:ZnMgO	14.1	72	21.8	901	951	50
Zn(O,S)	Al:ZnMgO with ARC	15.1	72.5	23.1	902	951	51

To summarize: the I-V results conclude that the Cu-poor $Cu(In,Ga)S_2$ absorbers can result in high PCE devices, provided the CdS buffer can be replaced with a buffer having optimum band alignment with $Cu(In,Ga)S_2$, so as to suppress the interface recombinations in the device and improve the PCE of the device. Moreover, since replacing the buffer changes the band alignment at the buffer/window interface, it is also imperative to explore alternate window layers to not suffer from FF losses due to high CBO at the buffer/window interface.

4.2 ZnMgO and Al:ZnMgO: Alternate buffer and i-layer for Cu(In,Ga)S_2 solar cells

The results of the previous section have established the potential of Cu-poor Cu(In,Ga)S_2 absorbers to produce high-efficiency devices with a high $V_{OC,ex}$, provided the rollover in I-V can be mitigated, and even higher efficiencies can be achieved by reducing the $V_{OC,in}$ degradation and interface V_{OC} deficit. In the case of Cu(In,Ga)S_2/Zn(O,S) device, the degradation in $V_{OC,in}$ seems to be originating from the necessary additional annealing step (~200 °C for 10 minutes) required to make good working devices. Therefore, in this section, the atomic layer deposited $Zn_{1-x}Mg_xO$ buffer layer is used as a substitute for Zn(O,S), as it does not require additional high-temperature annealing to achieve a good device performance (will be shown shortly). To mitigate the possibility of buffer/i-layer transport barrier as observed earlier, Al:$Zn_{0.75}Mg_{0.25}O$ is explored here as the i-layer partner for the ZnMgO buffer. The impact of varying Mg composition in $Zn_{1-x}Mg_xO$ buffer layer and substitution of i-ZnO by magnetron sputtered Al:$Zn_{0.75}Mg_{0.25}O$ or atomic layer deposited $Zn_{0.77}Mg_{0.23}O$ on Cu(In,Ga)S_2 device properties is explored. The interface V_{OC} deficit, and for this purpose, the $V_{OC,in}$ values obtained from calibrated PL measurements are discussed together with $V_{OC,ex}$ of the devices with different Mg concentrations in the ZnMgO films. On the completed devices, current-voltage measurements and external quantum efficiency measurements are performed to extract the device electrical characteristics. Numerical simulations are performed to comprehend the influence of electrical barriers on device current density-voltage (I-V) characteristics of the fabricated devices.

With minor modifications, sections 4.2.1 to 4.2.5 is taken directly from the submitted manuscript [159].

4.2.1 Device fabrication

Let us start by discussing the device fabrication process. The device preparation schematic starting from absorber until window deposition is presented in Fig. 4.4. The absorbers used in this part of the study are 3-stage Cu-poor Cu(In,Ga)S_2 absorbers, with as-grown average stoichiometry varying between [Cu]/[In+Ga] (CGI) ~0.93-0.97 and average [Ga]/[Ga+In] (GGI) ~0.12-0.22. For these absorbers, a variation in the $V_{OC,in}$ value across the absorbers grown in the same run and even on the same absorber was observed (see Fig. A4.6). The interface V_{OC} deficit is calculated by taking the difference between $V_{OC,in}$ measured on the spot within the area of the device whose $V_{OC,ex}$ is used to calculate the deficit. For this, the $V_{OC,in}$ is measured for all the absorbers at different spots prior to buffer deposition. Much like previous sections, here too, interface V_{OC} deficit will be used as a benchmark for comparison among different samples.

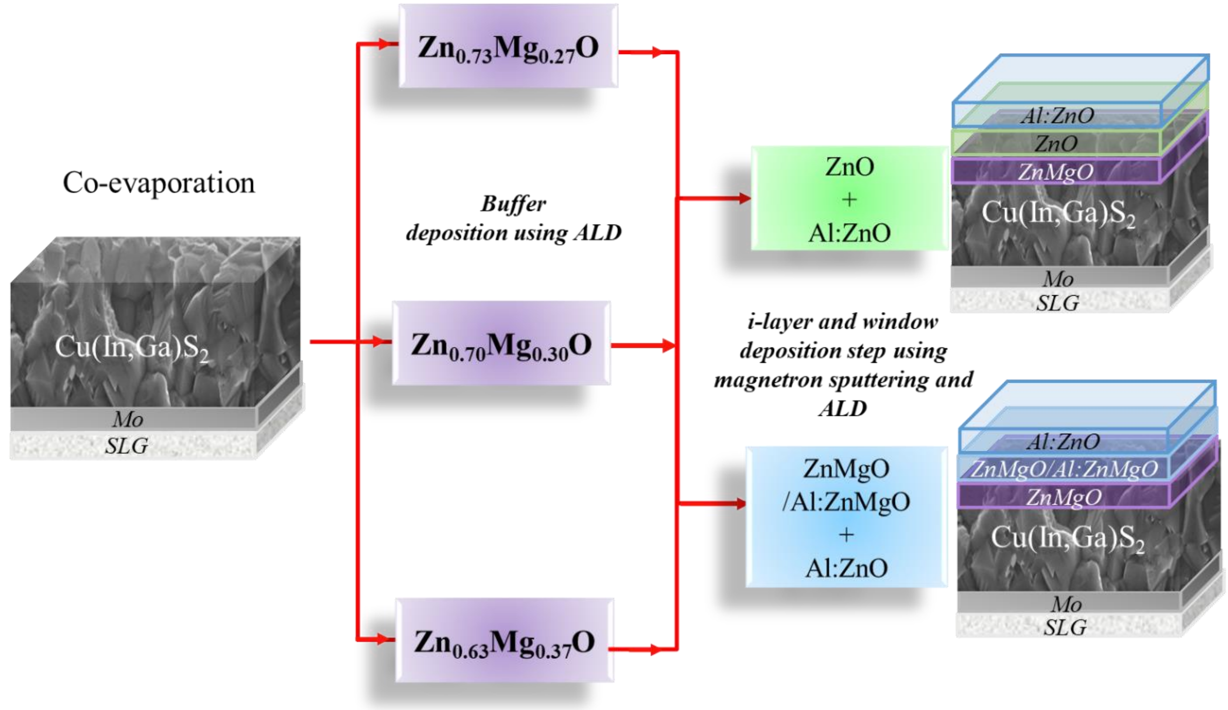


Figure 4.4: *Experimental schematic showing the device fabrication process. The* $Cu(In,Ga)S_2$ *absorbers are first processed with* $Zn_{1-x}Mg_xO$ *buffer layer with 27, 30 and 37 % Mg content, followed by deposition of either ZnO+Al:ZnO window layer or Al:*$Zn_{1-x}Mg_xO$*+Al:ZnO or* $Zn_{1-x}Mg_xO$*+Al:ZnO window layer.*

Prior to buffer deposition, all the absorbers were etched in 5 % KCN solution for 30 seconds to remove any oxides, followed by rinsing and storing in de-ionized water to prevent air exposure, as this could lead to degradation in $V_{OC,in}$ of chalcopyrite absorbers as observed previously.[83, 173] Immediately before introduction to the atomic layer deposition (ALD) reactor, the samples were blow-dried with nitrogen gas to remove the water layer from the samples. The atomic layer deposition of $Zn_{1-x}Mg_xO$ buffer was carried out exactly as explained in section 3.1.3. Depending upon the required composition, the MgO and ZnO supercycle was repeated to achieve a thickness of 30 nm. Since Mg incorporation was observed to be slightly lower than the pulse ratio, to get the desired ratio, higher Mg cycles per ZnO cycle are required. For example, $Zn_{1-x}Mg_xO$ with x = 0.27, would ideally require m Mg cycles and n ZnO cycles, where m/n ≈ 0.37. However, here 2 MgO cycles over 5 ZnO cycles (*i.e.* m/n ≈ 0.4) was repeated 21 times to achieve a thickness of about 26 nm.

Depending upon the device structure, a 70 nm thick i-layer was deposited using either ALD (for $Zn_{0.77}Mg_{0.23}O$) or magnetron sputtering (for i-ZnO and Al:$Zn_{0.75}Mg_{0.25}O$). The process for the deposition of $Zn_{0.77}Mg_{0.23}O$, and i-ZnO and Al:$Zn_{0.75}Mg_{0.25}O$ remains the same as explained in section 3.1.3 and 3.1.4, respectively. Finally, after i-layer deposition, the standard transparent conductive window layer (Al:ZnO) was sputtered and Ni-Al grids were evaporated onto the samples using e-beam evaporation. On each sample, several devices of area ~0.5 cm^2 were realized by mechanical scribing.

4.2.2 Effect of Mg content in the buffer on device low surface GGI device properties

The experiments were performed on two sets of $Cu(In,Ga)S_2$ absorbers, one with as grown $Cu(In,Ga)S_2$ average stoichiometry of [Cu]/[In+Ga] (CGI) ~ 0.93 and [Ga]/[Ga+In] (GGI) ~ 0.12, and a near-surface stoichiometry GGI ~ 0.12, and the other with average CGI ~ 0.97 and GGI ~ 0.22, and a near-surface GGI ~ 0.45.

Fig. 4.5a shows I-V characteristics of the devices prepared with absorbers having the lower GGI. The different curves correspond to devices made with $Zn_{0.73}Mg_{0.27}O$, $Zn_{0.7}Mg_{0.3}O$ and $Zn_{0.63}Mg_{0.37}O$ buffer layers, with either ZnO (dash-dotted) or Al:$Zn_{0.75}Mg_{0.25}O$ (solid) as the i-layer, deposited by sputtering. The I-V parameters are reported in table 4.3 along with $V_{OC,in}$ obtained by measuring PL on the spot inside the scratched device area. Among all the devices, the $Cu(In,Ga)S_2$ device prepared with ZnMgO buffer layer with x = 0.27 and Al:$Zn_{0.75}Mg_{0.25}O$ i-layer exhibits the highest PCE, owing to a high FF ~68 %. In general, for all the devices, the PCE deteriorates with increasing Mg content in the buffer primarily due to deterioration of the FF, independent of the i-layer used. When comparing a particular ZnMgO buffer composition, the i-ZnO devices show lower PCE than the Al:$Zn_{0.75}Mg_{0.25}O$ devices. The J_{SC} of all the devices is essentially unchanged by the buffer and is almost the same for all the devices.

Fig. 4.5b shows the variation of PCE, FF and the deficit between $V_{OC,in}$ and $V_{OC,ex}$ of the devices. A direct co-relation between the PCE and FF is fairly obvious from this chart. The PCE drops with increasing Mg content in buffer layers which can be majorly attributed to a loss in FF, as evident in I-V curve of devices (Fig. 4.5a). The observed drop in FF of the devices is because of the 'S shape' of the I-V curves, which becomes more prominent as the Mg content increases. Consequently, the maximum power point shifts to lower values as can be observed in Fig. 4.5a. Moreover, with increasing Mg content in the buffer, an increase in the interface V_{OC} deficit is observed, particularly in the devices prepared with i-ZnO. This indicates an increased $V_{OC,in}$ loss near the $Cu(In,Ga)S_2/Zn_{1-x}Mg_xO$ interface, which might originate from a gradient in electron quasi-Fermi level either in the vicinity of absorber surface (see section 6.3)[174] or within the contact layer.[35, 175] This even though the E_a of dominant recombination pathway obtained from $V_{OC,ex}$ vs T plot is ~E_G (see Fig. A4.3). Similar interface V_{OC} losses have also been observed in selenide solar cells with non-optimized contact layers.[83] Thus, it can be concluded that i-ZnO is not a good partner for ZnMgO buffer layer independent of Mg concentration in the buffer. Also, a high Mg concentration ≥ 0.27 in $Zn_{1-x}Mg_xO$ buffer is also bad for device performance. In both cases, a reduction in FF is observed. While for the former, it is due to an increase in injection barrier, for the latter, it is due to an increase in extraction barrier, as will be shown in section 4.2.4.

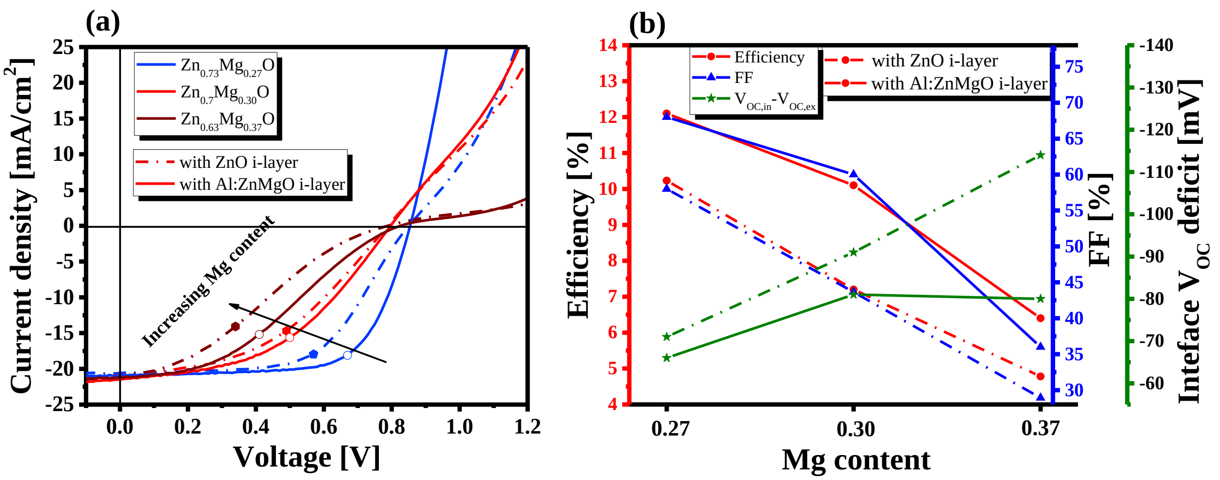


Figure 4.5: *(a)* I-V *curve of devices with different Mg content in ZnMgO buffer layers. The circles and dots show the maximum power point for each device. (b) Scatter chart of device PCE (left axis), fill factor (right axis) and interface* V_{OC} *deficit (second right axis) vs. different Mg content in ZnMgO buffer layers. The solid lines represent the device with i-Al:ZnMgO+Al:ZnO layer and the dotted lines represent the device with i-ZnO+Al:ZnO layer on top of the buffer.*

Table 4.3: *I-V characteristic of best Cu(In,Ga)S_2 devices made with $Zn_{1-x}Mg_xO$ buffer with x~ 0.27, 0.30 and 0.37 and with sputter deposited i-ZnO layer or Al:ZnMgO i-layer and Al:ZnO window layer.*

$Zn_{1-x}Mg_xO$	**PCE (%)**	**FF (%)**	**J_{SC} (mA/cm^2)**	**$V_{OC,ex}$ (mV)**	**$V_{OC,in}$ @1sun (mV)**	**$V_{OC,in}$ -$V_{OC,ex}$ (mV)**
x=0.27 Al:ZnMgO i-layer	12.1	68	20.9	854	920	68
x=0.27 ZnO i-layer	10.1	58	20.6	850	921	71
x=0.3 Al:ZnMgO i-layer	10.1	60	21.2	796	877	81
x=0.3 ZnO i-layer	7.2	44	20.9	785	876	91
x=0.37 Al:ZnMgO i-layer	6.4	36	21.5	825	905	80
x=0.37 ZnO i-layer	4.8	29	21.0	787	901	114

4.2.3 Effect of Mg content in the buffer on high surface GGI device properties

In the previous section, the effect of Mg content in the $Zn_{1-x}Mg_xO$ buffer and Al:$Zn_{1-x}Mg_xO$ i-layer on Cu(In,Ga)S_2 device performance with low near-surface GGI was explored. This section explores the impact of varying Mg content in $Zn_{1-x}Mg_xO$ buffer layer on the devices prepared with a high near-surface GGI Cu(In,Ga)S_2 devices. Investigating the device properties of high near-surface GGI absorbers is particularly interesting, as a high GGI towards the front surface compared to the bulk has been found to increase the $V_{OC,in}$ of the absorbers[176] and decrease the deficit between the theoretical maximum $V_{OC,in}$ or $V_{OC,in}^{SQ}$[177].

Fig. 4.6a shows the influence of near-surface GGI on the $V_{OC,in}$ of the corresponding absorbers. The $V_{OC,in}$ is plotted as a function of near-surface GGI of Cu(In,Ga)S_2 absorbers having an average CGI of 0.97 and an average GGI of 0.22, 0.18 and 0.12 corresponding to the absorbers with near-surface GGI of 0.45, 0.25 and 0.18, respectively. Only absorbers with the same average CGI are compared because the CGI in the Cu(In,Ga)S_2 absorber also influences the $V_{OC,in}$. It has been found that with decreasing CGI from 1.29 to 0.93, a suppression in deep defect peak around 1.1 eV in the PL spectrum of Cu(In,Ga)S_2 is observed.[73] Therefore, a fair comparison is only possible if similar CGI absorbers are compared. Moreover, as the absorbers possess different bandgaps (the band to band PL peak position) 1.56 eV, 1.59 eV and 1.57 eV, on the right axis the deficit between $V_{OC,in}^{SQ}$ and $V_{OC,in}$ is also plotted. From the chart, it is clear that with increasing surface GGI, the $V_{OC,in}$ increases. Moreover, the deficit between $V_{OC,in}^{SQ}$ and $V_{OC,in}$ decreases with increasing GGI. This shows that the improvement in $V_{OC,in}$ originates from the improved optoelectronic quality of the absorbers and not as a consequence of increased bulk bandgap. Hence, devices with a high surface GGI can lead to high $V_{OC,ex}$ and consequently high PCE in devices.

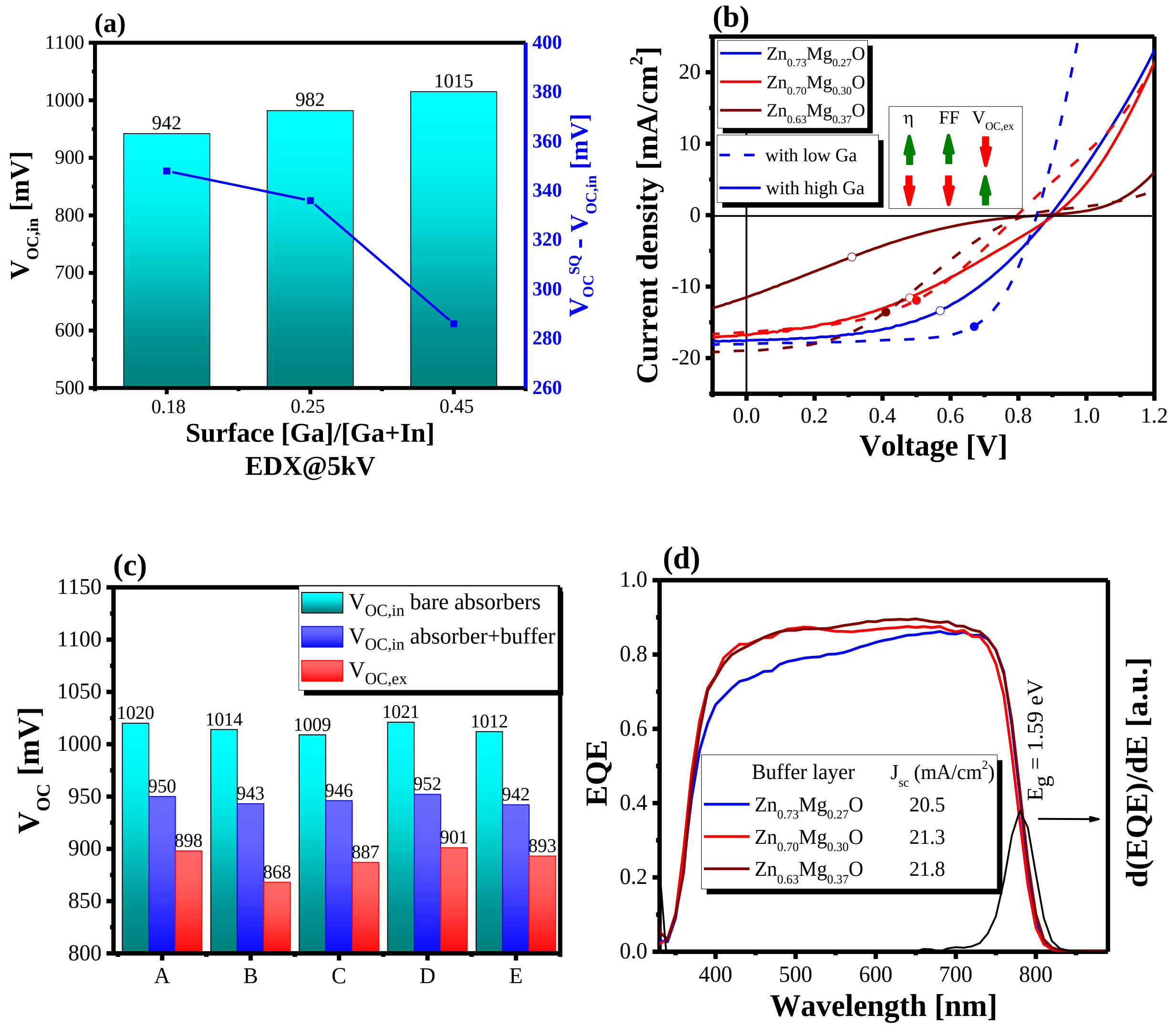


Figure 4.6: *(a) Bar chart showing qFLs as a function of surface GGI in the absorber (left axis) together with scatter chart of the deficit between Shockley–Queisser* V_{OC} *[177] corresponding to the bulk bandgap obtained using the photoluminescence and qFLs/e as a function of surface GGI. (b) I-V curve of the devices prepared with high near-surface GGI ~ 0.45 (solid lines) and low near-surface GGI ~ 0.12 (dashed lines) absorbers prepared with different Mg content in ZnMgO buffer layers. The arrows depict the general trend in I-V parameters whether they increase 9in green) or decrease (in red) with near-surface GGI in the absorber. (c) Bar chart of* $Cu(In,Ga)S_2$ *absorber (near-surface GGI ~0.45) showing* $V_{OC,in}$ *of bare absorber,* $Cu(In,Ga)S_2$ *absorber with ALD deposited* $Zn_{0.73}Mg_{0.27}O$ *and open-circuit voltage of final device measured on different spots namely A, B, C, D and E on the same sample. A degradation in* $V_{OC,in}$ *of absorber has been observed whenever the absorber is annealed during the buffer deposition or after the buffer deposition. (d) The corresponding EQE curves of the devices with high surface GGI. In the legend, the* J_{SC} *obtained by integrated EQE is obtained (see section 2.1.3).*

Table 4.4: *I-V characteristic of best Cu(In,Ga)S_2 devices prepared with different surface GGI absorbers and different Mg content in $Zn_{1-x}Mg_xO$ buffer layer. Two different sets of absorbers were used to make these devices, one having stoichiometry [Cu]/[In+Ga] (CGI) ~ 0.93 and bulk [Ga]/[Ga+In] (GGI) ~ 0.12 and a surface GGI ~ 0.12, and the other having stoichiometry CGI ~ 0.97 and GGI ~ 0.22 and a surface GGI ~ 0.44.*

$Zn_{1-x}Mg_xO$	PCE (%)	FF (%)	J_{SC} (mA/cm²)	$V_{OC,ex}$ (mV)	$V_{OC,in}$ @1sun (mV)	$V_{OC,in}$ -$V_{OC,ex}$ (mV)
x=0.27 GGI~0.12	10.4	68	18.0	854	920	68
x=0.27 GGI~0.45	7.6	48	17.5	893	1012	119
x=0.30 GGI~0.12	6.0	46	16.4	796	877	81
x=0.30 GGI~0.45	5.7	38	16.5	905	1013	108
x=0.37 GGI~0.12	5.6	36	18.9	825	905	80
x=0.37 GGI~0.45	1.8	18	11.5	872	1016	144

Based on the above observations, Cu(In,Ga)S_2 devices were fabricated with high near-surface GGI ~ 0.45 and average GGI ~ 0.22 absorbers with three different Mg content in the $Zn_{1-x}Mg_xO$ buffer (x= 0.27, 0.30 and 0.37) and Al:$Zn_{0.75}Mg_{0.25}O$ i-layer and Al:ZnO window layer. It must be noted that even though both absorbers have different GGI near the surface, they have the same band to band PL peak ~ 1.57 eV, *i.e.* they have the same bandgap. The I-V characteristic curves of these devices along with those of low near-surface GGI (~ 0.12) devices made with the same buffer and i-layer are presented in Fig. 4.6b (solid and dashed curves, respectively). Although an increase in near-surface GGI leads to an increase in $V_{OC,in}$, the improved $V_{OC,in}$ of the absorbers are not transformed into an improved device performance (Fig. 4.6b). This is partially due to a drop in the $V_{OC,in}$ of the absorbers after ALD buffer deposition (Fig. 4.6c), and the rest of it is not entirely transformed into $V_{OC,ex}$, due to contact losses. The loss in $V_{OC,in}$ after buffer deposition might be due to the degradation of the absorber at higher temperatures (~150 °C), which is essential for $Zn_{1-x}Mg_xO$ buffer deposition (at lower temperatures, uniform films could not be deposited). Similar degradation had been observed for absorbers covered with chemical bath deposited Zn(O,S) buffer after annealing at 200 °C for 10 minutes (see Fig. A4.4). Therefore, it seems that even 150 °C is a high enough temperature to result in $V_{OC,in}$ loss in the $Cu(In,Ga)S_2$ device.

The increase in the surface GGI also leads to a decrease in FF compared to low GGI devices, hence, leading to lower efficiencies (table 4.4). This is because the 'S shape' in the fourth quadrant and the rollover in the first quadrant becomes more prominent in high surface GGI devices with an increase in the Mg content in the buffer layer. For an Mg content of 0.37, the J_{SC} drops to ~ 11 mA/cm^2 suggesting a strong barrier for extraction of photogenerated carriers, which is also not observed for low surface GGI absorber. Thus, it seems that the high surface GGI is the cause for the strong 'S shape' together with the rollover. The effect of GGI along with the Mg content in buffer and i-layer will be discussed shortly using numerical simulations.

Astonishingly, the EQE of the devices with high surface GGI shows no sign of photocurrent blocking (Fig. 4.6d), unlike the observation in the I-V characteristics of the device.[178] Such a scenario occurs when there is a barrier for photogenerated carriers in the device. The current density in quantum efficiency measurements is rather small, and it can pass through the barrier. In contrast, the high current density of AM1.5G in I-V measurements cannot pass through the barrier because the J_{ph} at short-circuit conditions is larger than the J_{TE}.[48]

4.2.4 Numerical simulations for electrical barriers

The I-V curves of the devices with Mg ≥ 0.3 in the buffer layer exhibit 'S shape' in the fourth quadrant and a rollover at forward bias above their $V_{OC,ex}$ (Fig. 4.5a). This is a typical sign of an extraction and injection barrier at the front or back contact.[48, 179] For the devices studied here, the back contact barrier can be excluded because if the 'S shape' or the rollover was caused by the back contact barrier, it should have also been observed in the device with $Zn_{0.73}Mg_{0.27}O$ buffer layer. This, of course, assumes that ALD buffer deposition does not change the back contact or absorber properties near the back contact. Therefore, the front contact barrier is the only viable cause for the 'S shape' and rollover in these devices. Assuming thermionic emission is the limiting current across this barrier, the thermionic current in the device across the barrier can be described by equations 2.38 and 2.39 and which are also given below:

$$J_{TE} = qv_r \left[N_{c,w} \exp\left(\frac{-\varphi_b^n}{kT} \right) - N_{c,a} \exp\left(-\frac{\Delta E_c^{b,a} + E_{n,a}}{kT} \right) \right] \tag{2.38}$$

$$J_{TE} = J_{0,TE} \left[\frac{N_{c,w}}{N_{c,a}} \exp\left(\frac{-E_{n,a}}{kT} \right) \left(\exp\left(\frac{\Delta E_{Fn}}{kT} \right) - 1 \right) \right] \tag{2.39}$$

In above devices, φ_b^p = $E_{n,a}$ + $\Delta E_c{}^{b,a}$ is the barrier height from Cu(In,Ga)S_2 to window layer which is the energetic difference between CBM of $Zn_{1-x}Mg_xO$ at the Cu(In,Ga)S_2/$Zn_{1-x}Mg_xO$ interface and electron Fermi level at the Cu(In,Ga)S_2/$Zn_{1-x}Mg_xO$ interface. φ_b^n is the barrier height from the window layer to Cu(In,Ga)S_2, which is the energetic difference between conduction band minima of $Zn_{1-x}Mg_xO$ buffer at the Cu(In,Ga)S_2/$Zn_{1-x}Mg_xO$ interface and the electron Fermi level in the window layer. The value of φ_b^p and φ_b^n, and therefore, J_{TE} is influenced by the position of electron Fermi-level at the Cu(In,Ga)S_2/$Zn_{1-x}Mg_xO$ interface and in the window layer, which can be influenced by many factors. Among them, the relevant ones here are the CBO Cu(In,Ga)S_2/$Zn_{1-x}Mg_xO$ interface, CBO at the $Zn_{1-x}Mg_xO$/i-layer interface. For example, Fig. 4.7 depicts simulated band diagrams of devices with two different structures: 1. Cu(In,Ga)S_2/ZnMgO/ZnO/Al:ZnO (dash-dotted line Fig. 4.7) with a CBO of 0.2 eV at the Cu(In,Ga)S_2/ZnMgO interface, -0.4 eV at the ZnMgO/ZnO interface and no CBO at the ZnO/Al:ZnO interface.

2. Cu(In,Ga)S_2/ZnMgO/Al:ZnMgO/Al:ZnO (solid line Fig. 4.7) with a CBO of 0.2 eV at the Cu(In,Ga)S_2/ZnMgO interface, -0.2 eV at both ZnMgO/Al:ZnMgO and Al:ZnMgO/Al:ZnO interfaces.

Here we have assumed that Al:ZnMgO has a CBM 0.2 eV higher than ZnO. Even though CBO between the buffer and window layer is the same -0.40 eV for the two devices, the barrier height is different in each case. For device 1 it is 0.510 eV, whereas for device 2 it is 0.678 eV. A similar increase in φ_b^p and φ_b^n is expected with the addition of Mg to

$Zn_{1-x}Mg_xO$ buffer layer, as the Mg incorporation to $Zn_{1-x}Mg_xO$ is known to increase the CBM of the films.[151] As pointed out in section 2.2.2, whether or not the barrier limits the J_{light} and J_{dark} current depends upon the J_{TE} at a particular illumination and voltage bias condition. In the devices studied above, we vary either the CBM of the buffer or the CBM of the i-layer (*i.e.* 'x' in $Zn_{1-x}Mg_xO$). Therefore, to better differentiate and comprehend the impact of these two barriers on the device I-V characteristics, let us look at the effect of these two barriers with the help of the SCAPS 1-D simulator, first separately and then together. Below are three scenarios: with only varying CBO at the absorber/buffer interface with constant CBO at the buffer/i-layer, varying CBO at the buffer/i-layer interface with constant CBO at the absorber/buffer interface, and finally carrying CBO at the absorber/buffer and buffer/i-layer interface. This particularly helps distinguish the effect of CBO at the absorber/buffer interface and buffer/i-layer interface on the I-V curves of the device, which is a prior not very clear from equations 2.38 and 2.39. The parameters used for these simulations are reported in table A4.2.

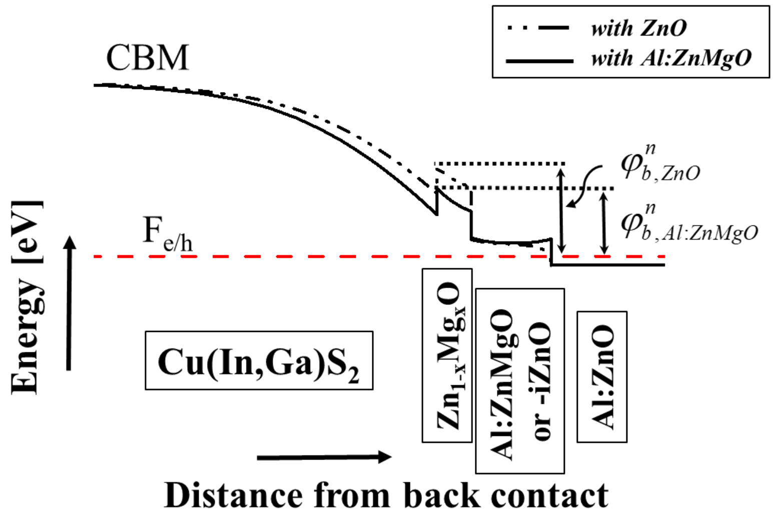


Figure 4.7: *Simulated band energy band diagram of* $Cu(In,Ga)S_2$ *device having a CBO of 0.2 eV at* $Cu(In,Ga)S_2$*/ZnMgO interface with Al:ZnMgO (solid) and ZnO (dash dotted lines) i-layer. For simulating Al:ZnMgO device a CBO of -0.2 eV is introduced at both ZnMgO/Al:ZnMgO interface and Al:ZnMgO/Al:ZnO interface. For simulating i-ZnO device a CBO of -0.4 eV is introduced at ZnMgO/i-ZnO interface and without any CBO at i-ZnO/Al:ZnO interface.*

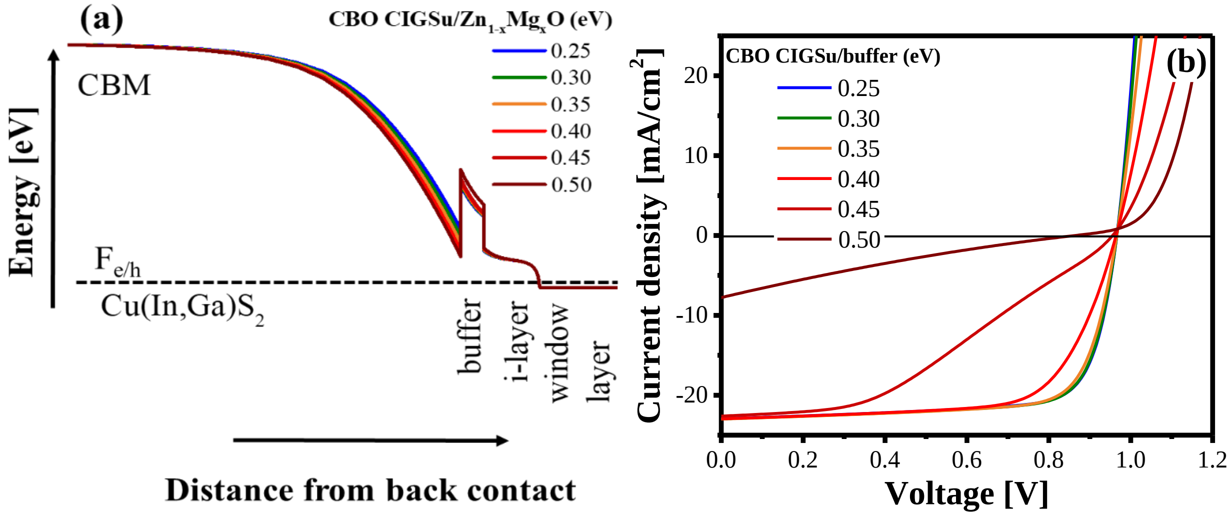


Figure 4.8: *Simulated band diagram and I-V curves of Cu(In,Ga)S₂ device with (a) and (b) varying CBO at Cu(In,Ga)S₂/buffer interface maintaining a constant CBO (-0.2 eV) at buffer/i-layer interface and no CBO at the i-layer/window layer.*

Let us start by looking at the impact of CBO at the absorber/buffer interface ($\Delta E_c^{b,a}$) alone on device I-V. While there is no experimental equivalent of this in this study, it does help us differentiate the effect of CBO at the absorber/buffer from the CBO at the buffer/i-layer (window layer) interface. For this, a Cu(In,Ga)S_2 device is simulated in SCAPS-1D, where only the CBM energy of the buffer is varied *via* changing its electron affinity. To exclude effects of change in CBO at the buffer/i-layer interface, CBO of -0.2 eV is maintained at the interface with no band offset at the i-layer/window layer. The CBO at the Cu(In,Ga)S_2/buffer interface is varied from 0.25 eV to 0.45 eV. The equilibrium band diagram and the I-V characteristics are then simulated and are presented in Fig. 4.8a and b, respectively.

It can be seen that a high CBO at the Cu(In,Ga)S_2/buffer interface >0.40 eV leads to an leads to an 'S shape' in the fourth quadrant, *i.e.* an extraction barrier, and for CBO ≥ 0.50 eV we even see J_{SC} and $V_{OC,ex}$ being affected. The 'S shape' originates from a high φ_b^p for CBO > 0.4 eV, *i.e.* a high barrier for photogenerated carriers as evident in Fig. 4.8a. Let us understand how this leads to a 'S shape' in the fourth quadrant. Under illumination at short circuit conditions, ΔE_{Fn} is large enough to have a net $J_{TE} > J_{light}$. Consequently, the photocurrent flowing from the absorber to the buffer is not limited. However, under forward bias application, the ΔE_{Fn} decreases (see Fig. 4.9), and so does the J_{TE} (see equation 2.39). At a certain bias, when $J_{TE} < J_{light,}$ the barrier becomes active and starts limiting the maximum photocurrent passing through the device. Thus, leading to a 'S shape' in the fourth quadrant of the I-V curve.

It must be noted that although such a device with high φ_b^p as evident from Fig. 4.8b exhibits 'S shape' and consequently a very low FF, it does not exhibit rollover in the first quadrant as observed in Fig. 4.5a.

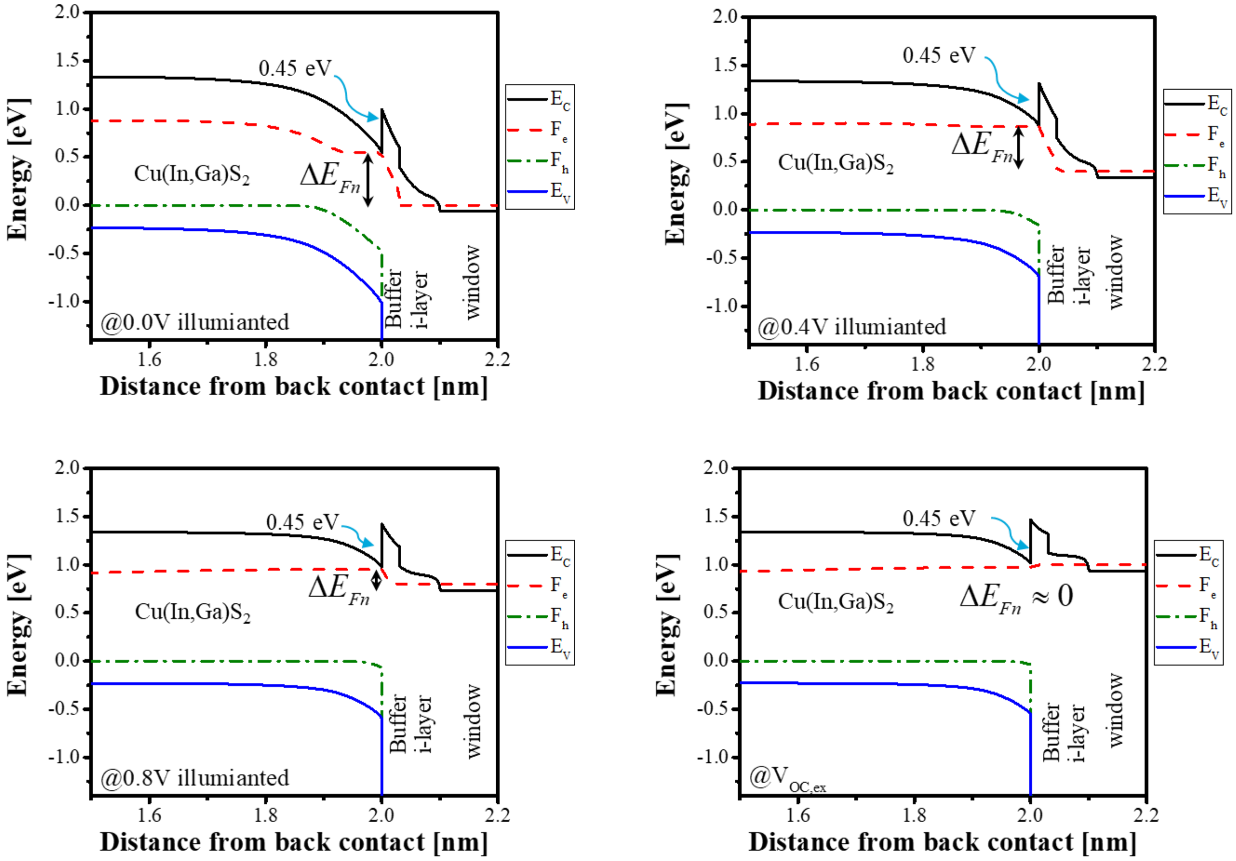


Figure 4.9: *Simulated band diagram of Cu(In,Ga)S$_2$ device under illumination at various applied voltage bias showing the variation of drop-in electron Fermi level. The device has a CBO of 0.45 eV at the absorber/buffer interface and -0.20 eV at the buffer-i-layer interface.*

Next, let us look at the impact of CBO at the buffer/i-layer interface on the device I-V characteristics with no CBO at the Cu(In,Ga)S_2/buffer interface. The Cu(In,Ga)S_2 device is simulated with different CBO at the buffer/i-layer interface, maintaining flat CBO at the Cu(In,Ga)S_2/buffer interface. The barrier φ_b^n was varied by varying the CBM of the i-layer keeping the CBM of buffer layer fixed at a value equal to CBM of absorber (*i.e.* with equal electron affinity). Such a device can be envisioned experimentally by varying Mg content in the ZnO i-layer without altering the Mg content in the $Zn_{1-x}Mg_xO$ buffer layer.

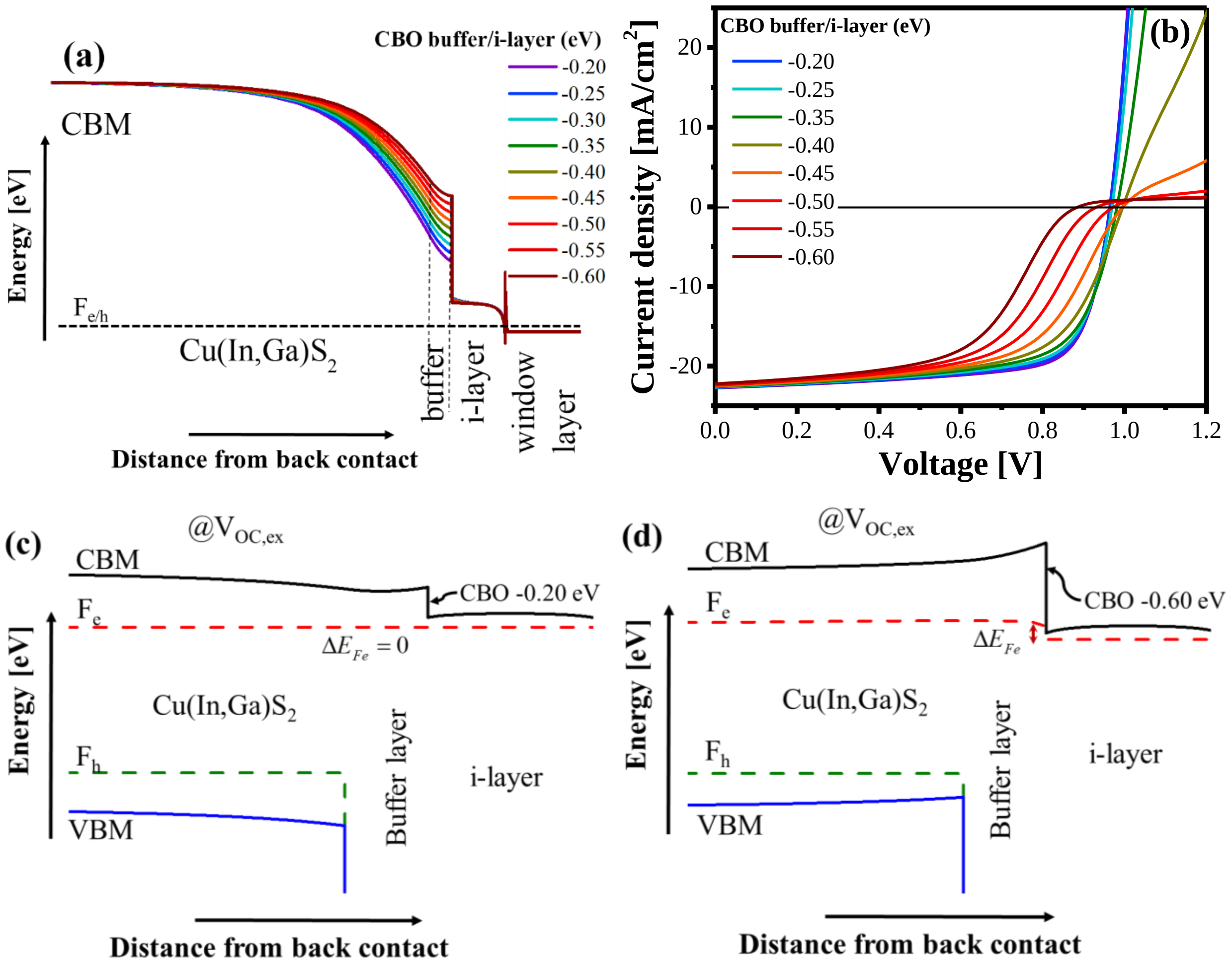


Figure 4.10: *Simulated band diagram and I-V curves of Cu(In,Ga)S_2 device with (a) and (b) varying CBO at buffer/i-layer interface by changing the CBM of the i-layer and keeping the CBM of Cu(In,Ga)S_2 and buffer layer at a fixed value to get a flat CBO at Cu(In,Ga)S_2/buffer interface. (c) and (d) shows the simulated band diagram of Cu(In,Ga)S_2 device at $V_{OC,ex}$ with -0.20 eV CBO and -0.60 eV CBO at the buffer i-layer, respectively.*

Fig. 4.10a and b show the simulated band diagram and the I-V characteristics of such a device. The device exhibits a drop in FF and even $V_{OC,ex}$ for very high negative CBO > 0.40 eV at the buffer/i-layer interface. The drop in FF is a direct consequence of an 'S shape' in the form of a strong rollover in the first quadrant. While the drop in $V_{OC,ex}$, originates from a drop in electron Fermi level at the interface, which is not present in devices that have low CBO at the buffer/i-layer interface (see Fig. 4.10c and d), the rollover is observed because the $E_{n,a}$, *i.e.* the position of electron Fermi-level at the interface, which increases with increasing negative CBO at the buffer/i-layer interface (see Fig. 4.10a). Consequently, thermionic current J_{TE} decreases. As the negative CBO at the buffer/i-layer interface and consequently $E_{n,a}$ or φ_b^n increases, a higher potential drop is required in between the window and the buffer layer to derive the same amount of J_{TE} through the device as for the lower negative CBO (as observed in Fig. 4.10b). The barrier thus acts as a series resistance in the device. This additional series resistance leads to a drop in FF as discussed in section 2.1.2. Moreover, the series resistance increases as the $E_{n,a}$ increases see section 2.2.2. It must be noted that when compared to the device with a high $\Delta E_c^{b,a}$ Fig. 4.8a, the drop in FF is not that substantial in these devices (see Fig. 4.10b).

Finally, Fig. 4.11a and b shows the simulated band diagram and the I-V characteristics of the $Cu(In,Ga)S_2$ device with varying CBO at the $Cu(In,Ga)S_2/Zn_{1-x}Mg_xO$ interface and $Zn_{1-x}Mg_xO$/i-layer interface, *i.e.* a varying φ_b^p and φ_b^n. Experimentally such a situation could be achieved by varying the Mg content in the $Zn_{1-x}Mg_xO$ buffer layer and keeping the Mg content fixed in the i-layer. Such a scenario most accurately fits the experimental part of this study. Assuming the increased bandgap in Al:ZnMgO i-layer is due to increased CBM energy, two device structures are simulated: one where the CBO at the $Cu(In,Ga)S_2/Zn_{1-x}Mg_xO$ was varied from 0.05 eV to 0.40 eV, which consequently results in a -0.25 eV to -0.60 eV CBO at the $Zn_{1-x}Mg_xO$/i-layer (assumed Al:ZnMgO). Other, where the CBO at the $Cu(In,Ga)S_2/Zn_{1-x}Mg_xO$ was varied from 0.05 eV to 0.40 eV, consequently resulting in a -0.45 eV to -0.80 eV CBO at the $Zn_{1-x}Mg_xO$/i-layer (assumed i-ZnO). This was achieved by varying just the CBM of the buffer layer and keeping the CBM of the i-layer fixed at a value (4.4 eV and 4.6 eV, respectively for Al:$Zn_{1-x}Mg_xO$ and i-ZnO).

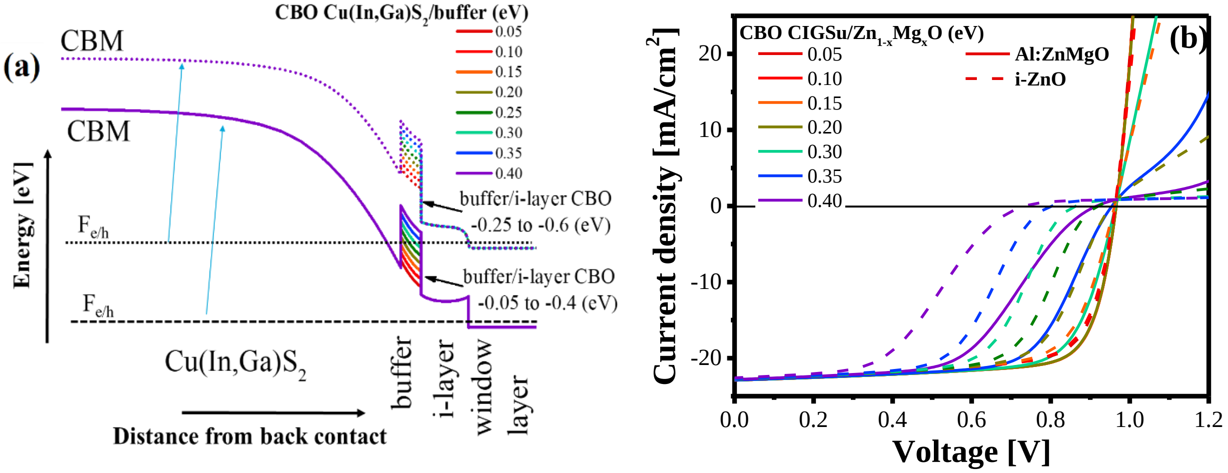


Figure 4.11: *Simulated band diagram and I-V curves of Cu(In,Ga)S_2 device with (a) and (b) varying conduction band minima position of buffer (assumed $Zn_{1-x}Mg_xO$) with either i-ZnO (dotted lines) or Al:$Zn_{0.75}Mg_{0.25}O$ (solid lines). With i-ZnO the CBO at $Zn_{1-x}Mg_xO$/i-layer interface varies between -0.25 eV to -0.60 eV, whereas for Al:$Zn_{0.75}Mg_{0.25}O$ it varies between -0.05 eV to -0.40 eV, the band diagrams for the two cases have been plotted with an offset for better clarity.*

The simulated I-V curves display both a reduction in FF and $V_{OC,ex}$, as the CBO at the Cu(In,Ga)S_2/$Zn_{1-x}Mg_xO$ interface increases beyond a specific value which is different for both structures. For the Al:ZnMgO i-layer device, a significant drop in FF and a slight drop in $V_{OC,ex}$ is observable for CBO ≥ 0.35 eV, whereas for the ZnO i-layer device, the drop is observable even for CBO of 0.20 eV and increases as CBO increases (see Fig. 4.11b). This partly explains why the interface V_{OC} deficit is higher for ZnO devices. For high CBO, the low FF in these devices originates from a combination of both: a 'S shape' in the fourth quadrant and a rollover in the first quadrant. As explained before, for high CBO, under the application of a forward bias, ΔE_{Fn} decreases, and so does the J_{TE} (see equation 2.39). At a certain bias $J_{TE} < J_{light}$, the barrier becomes active and starts limiting the maximum photocurrent passing through the device. Thus, leading to an 'S shape' in the fourth quadrant of the I-V curve. The rollover is caused by a large φ_b^n, at bias above $V_{OC,ex}$ $J_{TE} < J_{light}$, and limits the current in the device. To drive the diode current, a significant drop in ΔE_{Fn} is required, which is achieved at the expense of applied voltage.

The 'S shape' and rollover increases with increasing CBO at the $Cu(In,Ga)S_2/Zn_{1-x}Mg_xO$ interface, leading to a significantly reduced FF in the device. Moreover, for the same CBO at the $Cu(In,Ga)S_2/Zn_{1-x}Mg_xO$, the i-ZnO device shows a significantly stronger distortion in the I-V curve (see Fig. 4.11b). This is exactly what is observed in Fig. 4.5a. For the same Mg content in $Zn_{1-x}Mg_xO$ buffer layer, we observe a stronger 'S shape' and rollover in the ZnO i-layer device compared to Al:ZnMgO i-layer device. The stronger 'S shape' and rollover and thus a lower FF in the ZnO i-layer device originate due to a higher φ_b^n in the device as shown before in Fig. 4.7. Therefore, it is safe to conclude that the loss in device PCE with high Mg content in the buffer originates from a high φ_b^n which limits the J_{light} in the device.

While the above simulations and discussion explain very well the I-V curves of low surface GGI $Cu(In,Ga)S_2$ absorbers, it does not explain the observed differences between the I-V curves of the low and high GGI $Cu(In,Ga)S_2$ devices (Fig. 4.6), particularly the one with $Zn_{0.63}Mg_{0.37}O$ buffer layer. The two devices differ only in surface GGI, with the high surface GGI device exhibiting a stronger 'S shape' in the fourth quadrant and a very poor J_{SC}.

Other than the already discussed increase in CBM energy of the buffer layer, an alternative cause of the 'S shape' in the fourth quadrant in I-V curves could be an increased CBM energy of the $Cu(In,Ga)S_2$ absorber towards the surface, *i.e.* front conduction band grading (Fig. 4.12a). The band-edge measurements with photoelectron spectroscopy combined with near-edge x-ray absorption fine structure measurements show that an increase in Ga concentration increases the CBM of the $Cu(In,Ga)S_2$ absorber.[98] Therefore, a front conduction band grading could be observed in devices with a significant increase in GGI concentration towards the front surface, like the one discussed previously in section 4.2.3 with bulk GGI ~ 0.22 and surface GGI ~ 0.44. This would consequently result in a barrier for the electrons photogenerated in the bulk of the absorber.

In the following, the impact of surface bandgap grading on I-V curves is explored using SCAPS. For simulating these curves, the electron affinity at the surface of $Cu(In,Ga)S_2$ was varied from 4.4 eV to 4.0 eV and the bandgap was varied from 1.57 eV to 1.97 eV keeping the bulk electron affinity and bandgap fixed at 4.4 eV and 1.57 eV, respectively. Also, for simulating these curves, the electron affinity of buffer and i-layer was fixed at 4.4 eV so that no additional barrier is present for photogenerated electrons. The front grading is introduced by using the power law with an exponent of 20 when defining the composition of the absorber. For bandgap and electron affinity, a linear dependence on composition is set. Although the absorbers used to prepare devices here had a graded [Ga]/[In+Ga] (GGI) composition with a higher GGI concentration towards the molybdenum contact and the front interface (see Fig. 4.12b), to focus solely on the impact of front Ga grading, only a variation in electron affinity and bandgap towards the front was simulated. As such, the variation of electron affinity and bandgap of the absorber in the simulated device shown in Fig. 4.12c takes the polynomial function of the form:

For bandgap $$y = a + b^*x^m \tag{4.1}$$

For electron affinity $$y = a - b^*x^m \tag{4.2}$$

where, y is the variable bandgap (electron affinity), a is a constant equal to the set bulk bandgap (electron affinity), *i.e.* 1.57 eV (4.4 eV) in the structure, x is the distance from the back contact which varies from 0.0 to 2.0 micrometer (μm), b is the pre-factor which is different for different conditions (in the example where surface band gap is 1.97 eV and electron affinity is 4.0 eV it is 3.81×10^{-7} eV/μm) and m is the exponent which was set equal to 20 for these simulations.

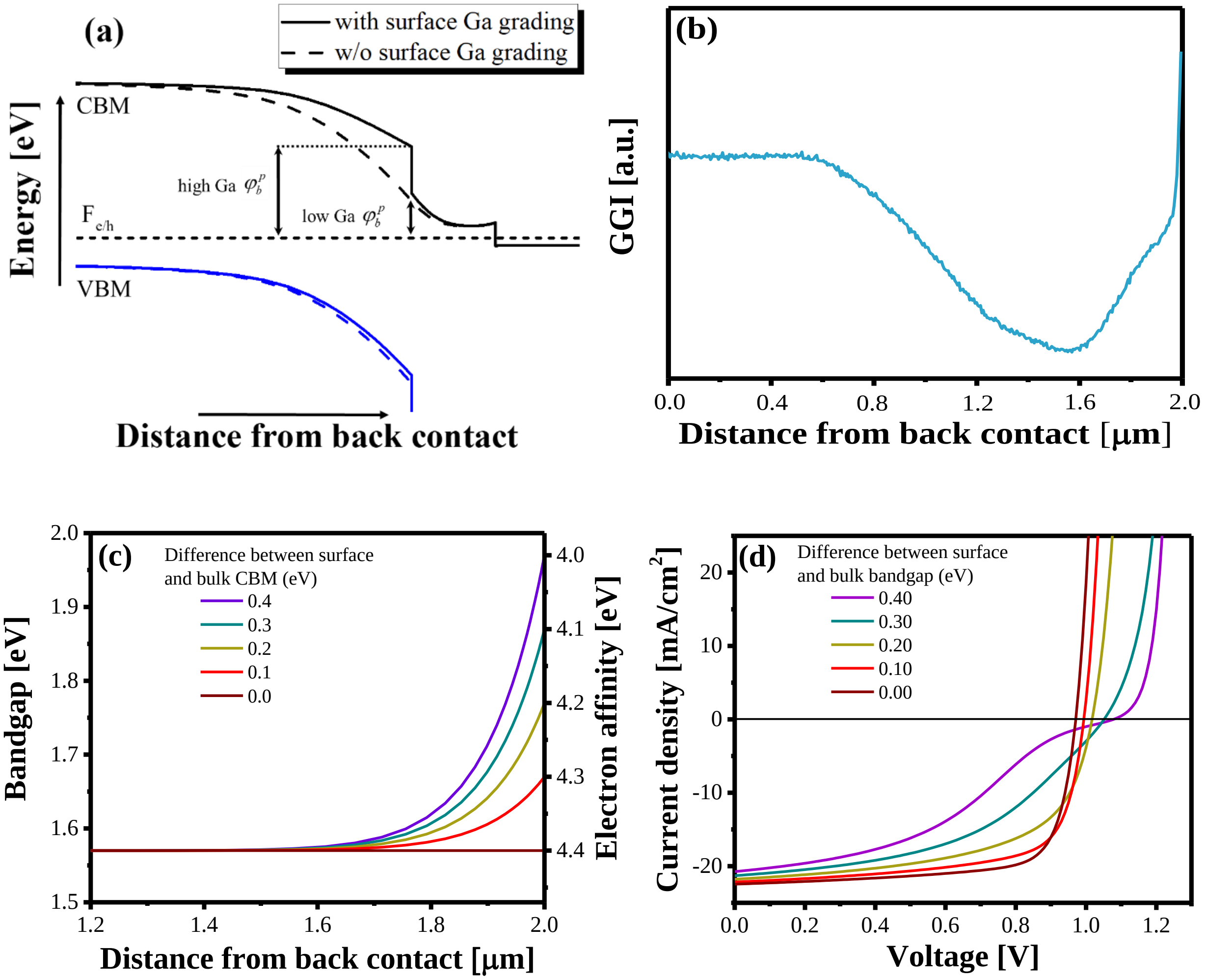


Figure 4.12: *(a) Simulated band diagram of Cu(In,Ga)S_2 with (solid lines) and without (dashed lines) surface CBM grading used to simulate the effect of high GGI towards the surface. The gradient is introduced by using a polynomial law as explained in equations 4.1 and 4.2. (b) [Ga]/[Ga+In] profile of a Cu-poor Cu(In,Ga)S_2 absorber grown using 3-stage co-evaporation process measured using secondary ion-mass spectroscopy. (c) Bandgap and electron affinity profiles as a function of distance from back contact that is used to simulate the effect of CBM grading in the device. The bulk bandgap and electron affinity is kept constant at 1.57 eV and 4.4 eV, and the surface bandgap and electron affinity is varied from 1.57-1.97 eV and 4.4-4.0 eV, respectively. (d) Corresponding simulated I-V curves of a device with varying CBM grading towards the surface.*

Fig. 4.12d shows the simulated I-V characteristics of the devices with a different GGI concentration at the surface (always increasing towards the surface). As the surface bandgap and along with it the CBM increases, a decrease in FF along with a reduction in J_{SC} is observed. For a difference of 400 meV between the bulk and surface CBM, a clear 'S shape' is observed in the fourth quadrant, suggesting that the bandgap grading acts as a barrier in the device. This is because, compared to the device without GGI grading, the graded device has a higher φ_b^p (Fig. 4.12a) and consequently a lower J_{TE}. Moreover, when an additional barrier for photogenerated carriers is present, such as a conduction band spike at the absorber/buffer interface, the 'S shape' becomes even more prominent as the barrier height increases, further leading to an even lower J_{TE}. This scenario is simulated in Fig. 4.13a and b, where the band diagram and I-V curves of devices with different CBO at the $Cu(In,Ga)S_2$/$Zn_{1-x}Mg_xO$ interface are simulated while keeping the electron affinity of i-layer fixed at 4.4 eV and window layer at 4.6 eV. For a CBO of -0.1 eV and 0.0 eV, there is a very minute difference in the I-V curves in the fourth quadrant as in both cases the φ_b^p depends upon the surface Ga concentration only. However, for CBO > 0.0 eV, φ_b^p increases by an amount equal to the CBO and consequently, a lower J_{light} due to limiting J_{TE} is observed for the same applied voltage, which decreases as the CBO increases. This resembles the situation in Fig. 4.6b, where a lower J_{light} is observed for high Mg content for the same applied voltage. Thus, a combination of high GGI, a conduction band spike at the absorber/buffer interface leading to a high φ_b^p results in an I-V shape like the one observed for high GGI devices with $Zn_{0.63}Mg_{0.37}O$ buffer layer.

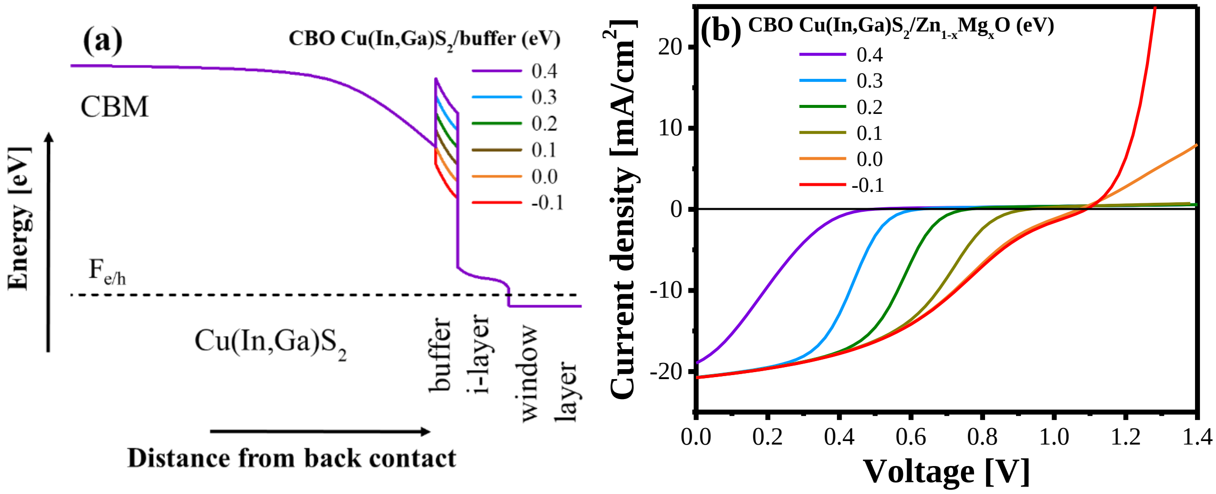


Figure 4.13: *(a) and (b) Simulated equilibrium band diagram displaying CBM and Fermi level and I-V curves of a graded CBM* $Cu(In,Ga)S_2$ *device with varying CBO at the* $Cu(In,Ga)S_2$*/buffer interface from -0.1 to 0.4 eV. The device has CBM 0.4 eV higher at the surface compared to the bulk, with the depth profile as plotted in Fig. 4.10c.*

4.2.5 ALD vs. sputter-deposited i-layer

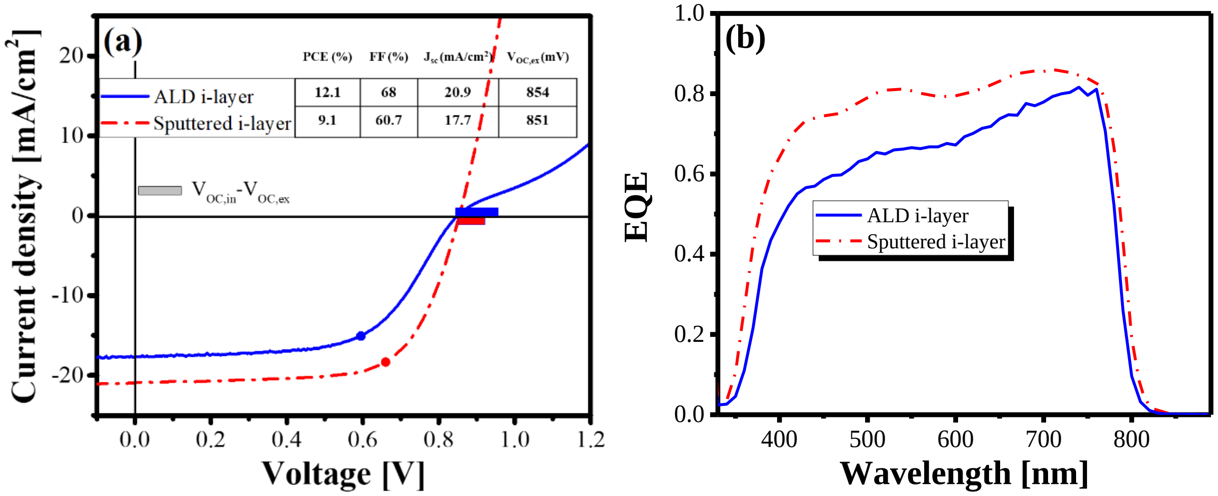
From the above discussion, the $Zn_{0.73}Mg_{0.27}O$ buffer layer emerges as the best partner for $Cu(In,Ga)S_2$ devices resulting in the highest PCE in the device. Next, in this thesis, as a partner for this buffer layer, ALD deposited $Zn_{0.77}Mg_{0.23}O$ i-layer was also investigated as an alternative to $Al:Zn_{0.75}Mg_{0.25}O$ sputtered i-layer. The results of these investigations are presented in the following subsection.

Fig. 4.14a shows the I-V curve of $Cu(In,Ga)S_2$ device fabricated with ALD deposited $Zn_{0.73}Mg_{0.27}O$ buffer layer and ALD deposited $Zn_{0.77}Mg_{0.23}O$ i-layer. Sputtered Al:ZnO is still used as the transparent conductive window layer. For comparison, the I-V curve of the device with ALD deposited $Zn_{0.73}Mg_{0.27}O$ buffer layer and sputtered $Al:Zn_{0.75}Mg_{0.25}O$ i-layer is plotted in the same figure. As evident, the ALD deposited i-layer is inferior to sputtered i-layer in terms of the FF and J_{SC} of the device. Though it may seem that $V_{OC,ex}$ for both devices is similar, it is not true as both devices do not possess similar $V_{OC,in}$. The device with ALD deposited i-layer exhibits a $V_{OC,in}$ of 957 mV, and therefore, has a higher interface V_{OC} deficit ~ 100 mV compared to 68 mV possessed by the device prepared using sputtered i-layer, which has a $V_{OC,in}$ of 920 mV (see the bar in the I-V plot). The higher interface V_{OC} deficit in the ALD deposited i-layer device might be caused by a larger degradation of the absorber. The degradation in $V_{OC,in}$ of $Cu(In,Ga)S_2$ device has been earlier related to high-temperature annealing of the device during or after the buffer deposition, which is independent of whether the device is prepared using chemical bath deposited Zn(O,S) buffer layer or atomic layer deposited $Zn_{1-x}Mg_xO$ buffer layer (see Fig. A4.8). In the case of ALD deposited i-layer, the degradation is higher since the buffer and i-layer deposition process requires the absorber to be at 150 °C for ~6 hours. In contrast, the device prepared with sputtered Al:ZnMgO requires only the buffer deposition 3 hours as there is no i-layer ALD deposition step involved.

To understand the loss in J_{SC}, the EQE of the device is measured and is plotted in Fig. 4.14b. The EQE of the device drops as the wavelength decreases, causing a loss in J_{SC} of the device. In comparison, this drop is much weaker in the case of sputtered $Al:Zn_{0.75}Mg_{0.25}O$ i-layer device. This loss indicates poor collection near the absorber/buffer interface. This could happen if the absorber is only weakly doped, *i.e.* the p = n point is deep in the absorber, and near the interface, there is a high recombination probability for holes.[178] The photogenerated holes near the interface recombine while drifting towards the back contact, consequently the EQE, and therefore, the J_{SC} drops. It is conceivable that the long ALD deposition time has reduced the absorber doping or increased the defects at the absorber-buffer interface.

For the ALD deposited $Zn_{0.77}Mg_{0.23}O$ i-layer device, the loss in FF can be attributed directly to a high R_s in the device ~ 9.8 Ω-cm^2 compared to ~ 2.8 Ω-cm^2 in the sputtered Al:$Zn_{0.75}Mg_{0.25}O$ i-layer device. The R_s was extracted using the I-V fit routine as described in section 2.1.2. The high R_s originates from the barrier at the buffer/i-layer interface as evident from the rollover observed in the first quadrant of the I-V curve. A higher barrier φ_b^p in the ALD deposited $Zn_{0.77}Mg_{0.23}O$ i-layer device might be either due to the presence of bigger cliff at the buffer/i-layer interface or a lower position of electron Fermi level near the $Cu(In,Ga)S_2$/ZnMgO interface. Since i-layers have almost similar Mg concentration, it can be assumed that the CBO at the buffer/i-layer interface is the same in both devices. Therefore, the rollover must originate from a lower position of electron Fermi level near the $Cu(In,Ga)S_2$/ZnMgO interface. The possible causes could be an increase in absorber doping or a decrease in doping towards the n-side of the junction, which makes the inversion near the interface weaker.

At the time of writing this thesis, no detailed analysis was done to compare the carrier concentration in the absorber or n-layer stack of ALD deposited $Zn_{0.77}Mg_{0.23}O$ i-layer and sputtered Al:$Zn_{0.75}Mg_{0.25}O$ i-layer. Nonetheless, the I-V results do conclude that the sputtered Al:$Zn_{0.75}Mg_{0.25}O$ is the superior i-layer choice for $Cu(In,Ga)S_2$ solar cells.



	PCE (%)	FF (%)	J_{sc} (mA/cm^2)	$V_{OC,ex}$ (mV)
ALD i-layer	12.1	68	20.9	854
Sputtered i-layer	9.1	60.7	17.7	851

Figure 4.14: *(a) I-V curve and (b) EQE curve of the Cu(In,Ga)S_2 device prepared with $Zn_{0.73}Mg_{0.27}O$ buffer layer with either ALD deposited $Zn_{0.73}Mg_{0.27}O$ i-layer or sputtered Al:$Zn_{0.75}Mg_{0.25}O$ i-layer. The bar represents the interface V_{OC} deficit, and the dots represent the maximum power point. Inset of figure is the table of the device I-V characteristic values.*

At this point in the thesis, the optimized ZnMgO buffer and i-layer conditions were known. Therefore, a final set of Cu(In,Ga)S_2 devices with ALD deposited $Zn_{0.73}Mg_{0.27}O$ buffer layer and sputtered Al:$Zn_{0.75}Mg_{0.25}O$ i-layer were fabricated. The absorbers used for this study had a slightly higher Ga concentration in bulk GGI ~ 0.18 with a surface GGI ~ 0.25 compared to earlier devices, possessing a $V_{OC,in}$ of 986 mV and an E_G ~ 1.63 eV obtained by $\frac{d(EQE)}{dE}$ analysis (see Fig. A4.9). The I-V characteristic of the device with ARC coating and after light soaking for 30 minutes under open-circuit conditions is presented in Fig. 4.15, whereas the device I-V curve without ARC coating can be found in Fig. A4.9. For ARC coating, 98 nm thick MgF_2 film was deposited on the device using e-beam evaporation. The thickness was calculated for minimizing reflections at 540 nm using equation 3.1 according to the procedure described in section 3.1.4. The device exhibits a PCE of 14.0 % with a $V_{OC,ex}$ of 943 mV, and an interface V_{OC} deficit of 43 mV. This is the highest PCE and $V_{OC,ex}$, among all the ZnMgO devices fabricated in this thesis.

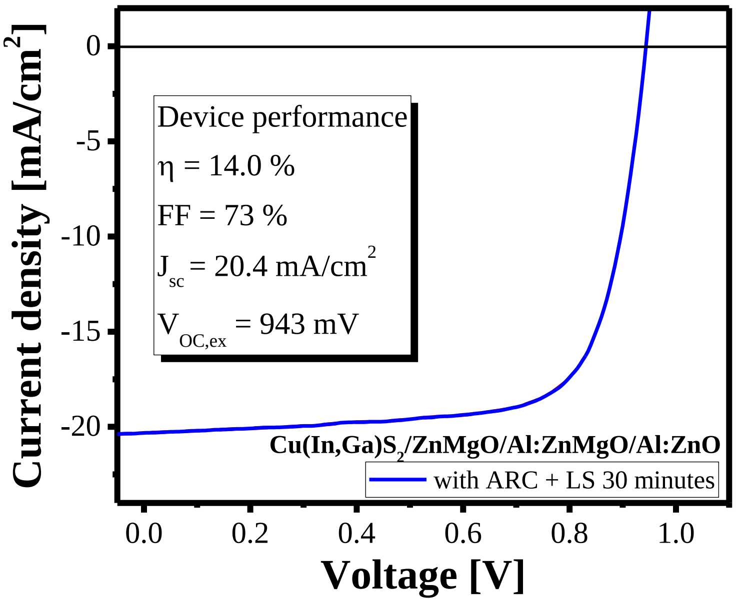


Figure 4.15: *I-V curve of the best device prepared with* $Zn_{0.73}Mg_{0.27}O$ *buffer layer together with Al:ZnMgO i-layer layer and Al:ZnO window layer. The curve is obtained for a device with an anti-reflective coating of* MgF_2 *and light-soaked for 30 minutes under open-circuit conditions.*

To summarize, a combination of atomic layer deposited $Zn_{1-x}Mg_xO$ buffer layer with 'x'=0.27 and sputtered Al:$Zn_{1-x}Mg_xO$ i-layer with 'x'=0.25 delivers highly efficient ~14 % Cu(In,Ga)S_2 devices with E_G ~ 1.63 eV. A high Mg content ≥ 0.3 in the $Zn_{1-x}Mg_xO$ buffer results in FF loss in the device. The loss originates from the presence of high injection and extraction barriers in the device due to a large positive CBO at Cu(In,Ga)S_2/ZnMgO interface and a large negative CBO at the ZnMgO/i-layer interface. Comparatively, sputtered Al:ZnMgO outperformed atomic layer deposited ZnMgO i-layer in terms of device performance. A degradation in $V_{OC,in}$ value was found and speculated to originate from the high-temperature deposition process of ALD $Zn_{1-x}Mg_xO$ films in the devices.

4.3 ZnSnO: Another alternate buffer for Cu(In,Ga)S_2 solar cell

In the previous section, even in the atomic layer deposited ZnMgO devices, a drop in $V_{OC,in}$ in buffer coated Cu(In,Ga)S_2 device was found compared to the $V_{OC,in}$ of Cu(In,Ga)S_2 without any buffer layer. The drop in $V_{OC,in}$ is likely related to high temperatures used for ZnMgO deposition. Ideally, it would be interesting to make devices with ZnMgO buffer deposited at a lower temperature to achieve a higher $V_{OC,ex}$ and PCE. However, at the time of writing this thesis, the ZnMgO buffer recipe at lower temperatures was still being developed.

Besides ZnMgO, ZnSnO is also a promising buffer layer and has helped achieve a $V_{OC,ex}$ of 1 V for $CuGaSe_2$ devices.[180] Moreover, the buffer can be deposited at relatively lower temperatures than ZnMgO, around 90-120 °C. Therefore, with the aim to reduce the drop in $V_{OC,in}$ during buffer deposition, Cu-poor $Cu(In,Ga)S_2$ devices with two different ZnSnO buffer recipes (*i.e.* 30 nm $Zn_{0.8}Sn_{0.2}O$ film deposited at 105 °C and the 30 nm $Zn_{0.8}Sn_{0.2}O$ deposited at 120 °C) were realized. In addition, also to probe the impact of buffer/i-layer band alignment on device performance and find the optimum i-layer for this particular buffer, a variation of i-layers were tested, namely: ZnO, Al:ZnMgO, and no i-layer at all. As usual, the Al:ZnO window layer was used with each of these combinations.

The corresponding device I-V characteristic curves are presented in Fig. 4.14a. Let us start by discussing the devices prepared with $Zn_{0.8}Sn_{0.2}O$ film deposited at 105 °C (shown by dotted lines in Fig 4.16). All the devices exhibit nice diode-like curves with no ‘S shape’ or rollover. Between the three i-layers, the device with Al:ZnMgO exhibits the highest FF and consequently a PCE of ~13.7 %, resulting from the lowest transport barrier in the device as already observed in section 4.2 (also see Fig. 4.17). The PCE is the highest among all $Cu(In,Ga)S_2$ devices prepared with $Zn_{0.8}Sn_{0.2}O$ buffer grown at 105 °C or 120 °C (see table 4.5). However, the device suffers from a high interface V_{OC} deficit of 52 mV, losing ~1 % absolute PCE (assuming all this deficit is converted into $V_{OC,ex}$). The device without any i-layer performs better in this aspect, as it loses just 29 mV in terms of interface V_{OC} deficit. However, due to a significant loss in FF compared to Al:ZnMgO and ZnO i-layer devices, the PCE of the device without i-layer is stuck at 11.8 %. While a loss in FF for ZnO i-layer device compared to Al:ZnMgO device is excepted as ZnO i-layer device has a higher barrier height (see Fig. 4.7), the loss in FF for Al:ZnO device is a bit surprising as the device should have the same barrier height as for Al:ZnMgO device (see Fig. 4.17 simulated band diagrams of different devices at equilibrium).

Therefore, to understand the origin of loss in FF the light I-V curves of the device were fitted with the one-diode model using I-V routine as explained in section 2.1.2 to extract the device R_s and R_{sh}. Indeed, the Al:ZnO device without i-layer has an R_{sh} of only 303 Ω-cm^2, significantly lower than the device with Al:ZnMgO (831 Ω-cm^2) or ZnO (730 Ω-cm^2) i-layer (see Fig. 4.18a).

Moreover, surprisingly the device also has an R_s value ~ 4.5 Ω-cm^2, slightly higher than the ZnO i-layer device ~ 3.3 Ω-cm^2. The high R_s is puzzling and can't be explained easily. On the other hand, the lower R_{sh} could result from sputter damage originating from sputtering of highly conductive Al:ZnO directly on top of buffers.[90, 181, 182] If the buffer does not provide complete coverage on the absorbers, or is easily damaged during the sputtering process, the highly conductive Al:ZnO window layer comes directly in contact with absorbers, or worse, with the back contact and can result in shunting pathways in the device. Therefore, it can be concluded that the $Zn_{0.8}Sn_{0.2}O$ buffer deposited at 105 °C does not provide adequate protection from sputter damage.

The ZnO i-layer device has the highest 91 mV interface V_{OC} deficit. This result is in accordance with our earlier observations (section 4.2.2). Thus, the loss in FF possibly due to a large cliff (compared to Al:ZnMgO i-layer) at the buffer/i-layer interface and large interface V_{OC} deficit is what limits the device efficiency to 12.6 %.

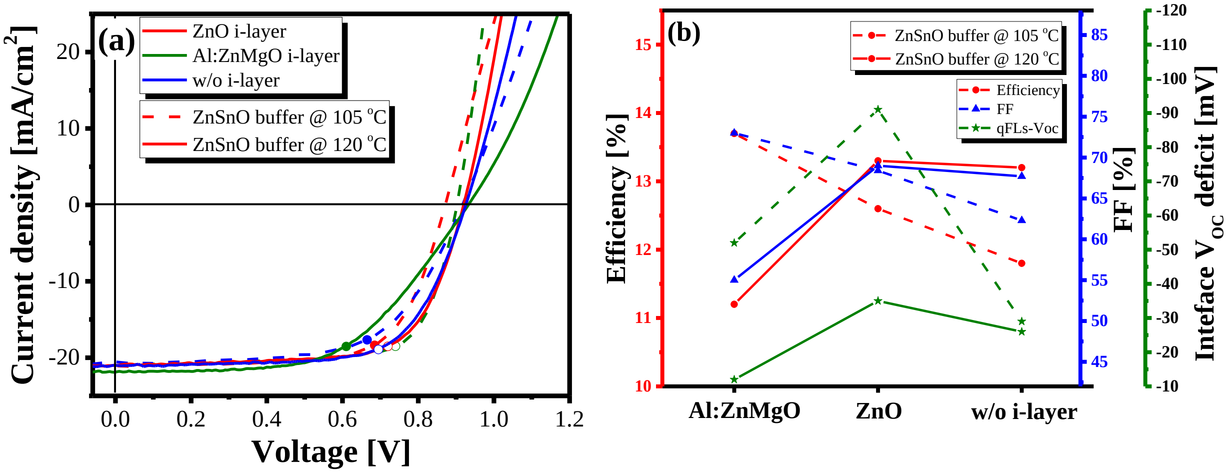


Figure 4.16: *(a) I-V curve of the $Cu(In,Ga)S_2$ devices prepared with ZnSnO buffer layer deposited at 105 °C (dashed lines), ZnSnO buffer layer deposited at 120 °C (solid lines). The red, olive and blue lines represent the devices prepared with ZnO, Al:ZnMgO and without buffer layer. (b) Scatter chart of device PCE (left axis), fill factor (right axis) and interface V_{OC} deficit (second right axis) vs different i-layers, i.e. ZnO or Al:ZnMgO or without i-layer. The dashed lines represent the device with ZnSnO buffer deposited at 105 °C layer, and the solid lines represent the device with ZnSnO buffer deposited at 120 °C buffer layer.*

Table 4.5: *I-V characteristic of best Cu(In,Ga)S_2 devices made of CdS and Zn(O,S) buffer. For Zn(O,S) buffer two different i-layer were used, for one device i-ZnO and for the other Al:ZnMgO. Since the $V_{OC,in}$ was measured only before buffer deposition, the $V_{OC,in}$ values reported here are reduced by 25 mV to account for $V_{OC,in}$ loss after annealing at 200 °C for 10 minutes.*

Buffer layer	**i-layer**	**PCE (%)**	**FF (%)**	**J_{SC} (mA/cm^2)**	**$V_{OC,ex}$ (mV)**	**$V_{OC,in}$ @1sun (mV)**	**$V_{OC,in}$ -$V_{OC,ex}$ (mV)**
ZnSnO 105 °C	ZnO	12.6	68.4	21.1	872	963	91
ZnSnO 105 °C	Al:ZnMgO	13.7	73	21.0	902	954	52
ZnSnO 105 °C	w/o	11.8	62.3	20.6	917	946	29
ZnSnO 120 °C	ZnO	13.3	69	21.0	920	955	35
ZnSnO 120 °C	Al:ZnMgO	11.2	55	21.9	932	944	12
ZnSnO 120 °C	w/o	13.2	67.7	21.0	926	952	26

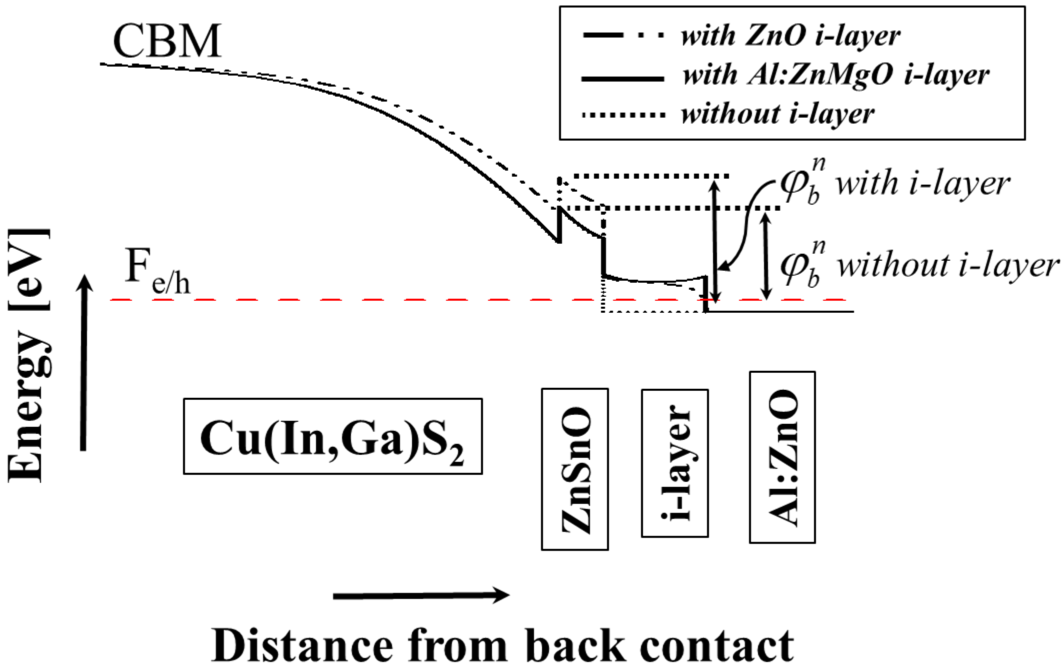


Figure 4.17: *Simulated band energy band diagram of Cu(In,Ga)S_2 device having a CBO of 0.2 eV at Cu(In,Ga)S_2/ZnSnO interface with Al:ZnMgO i-layer (solid), ZnO i-layer (dash-dotted lines) and only Al:ZnO (dotted) window layer. For simulating Al:ZnMgO device a CBO of -0.2 eV is introduced at both ZnMgO/Al:ZnMgO interface and Al:ZnMgO/Al:ZnO interface. For simulating i-ZnO device a CBO of -0.4 eV is introduced at ZnMgO/i-ZnO interface and without any CBO at i-ZnO/Al:ZnO interface and for simulating no i-layer device CBO of -0.4 eV is introduced at ZnMgO/Al:ZnO interface.*

The I-V curves of devices prepared with $Zn_{0.8}Sn_{0.2}O$ buffer grown at 120 °C is shown in Fig. 4.16. Remarkably all the devices exhibit a very low interface V_{OC} deficit compared to $Zn_{0.8}Sn_{0.2}O$ buffer grown at 105 °C. Particularly the device with Al:ZnMgO i-layer has an interface V_{OC} deficit of mere 12 mV. This value is lowest among all the other buffer layers studied so far, suggesting that this particular buffer deposition process leads to minimum absorber $V_{OC,in}$ deterioration.

Among the devices prepared with $Zn_{0.8}Sn_{0.2}O$ at 120 °C with the three i-layer combinations, the ZnO i-layer device unexpectedly outperforms all other devices. This improvement is a direct consequence of a low interface V_{OC} deficit in the device ~35 mV. Consequently, the device exhibits 50 mV higher $V_{OC,ex}$ (compared to ZnO device with $Zn_{0.8}Sn_{0.2}O$ buffer layer deposited at 105 °C), and therefore a PCE of 13.3 %, highest among this set of devices.

The device without any i-layer with a PCE of 13.2 % performs almost as well as the device with the i-ZnO layer and the same buffer layer. This device has an even lower interface V_{OC} deficit than ZnO i-layer device, something that was observed with $Zn_{0.8}Sn_{0.2}O$ buffer layer deposited at 105 °C as well (see table 4.5). Therefore, the device has a higher $V_{OC,ex}$ compared to ZnO device (see Fig. 4.16b). The only reason for the inferior PCE of this device is the slightly lower FF. Though, unlike the device with a $Zn_{0.8}Sn_{0.2}O$ buffer deposited at 105 °C with no i-layer, this device exhibits better FF owing to an improved R_{sh} of 1141 Ω-cm^2. However, the device has a higher R_s (3 Ω-cm^2) compared to ZnO (2 Ω-cm^2) device, and thus, a lower FF.

The extracted R_s and R_{sh} values from I-V fit method are also reported in Fig. 4.18a. The PCE of Al:ZnMgO i-layer device is the most surprising of all. Even though the device has a high J_{SC} (due to higher EQE see Fig. 4.18b), a very low interface V_{OC} deficit, and thus a high $V_{OC,ex}$, a highly deteriorated FF limits the device performance to a mere 11.2 %, which is ~2 % absolute lower than other two devices in this set. The high FF originates from a very high R_s (9.8 Ω-cm^2) observed for this device (also easily observable in the I-V curve), which is significantly higher than any other device (see Fig. 4.16a and table 4.5). Since Al:ZnMgO i-layer so far in this thesis has performed very well in all the devices except this one, it is only reasonable to believe something went wrong during the device fabrication, either in the ZnSnO deposition or the Al:ZnMgO deposition. And the device can be treated as an outlier. At the time of writing this thesis, further experiments are underway to prepare more devices with $Zn_{0.8}Sn_{0.2}O$ buffer deposited at 120 °C. The preliminary results (not shown here) display significantly higher FF, further confirming our claim to treat the device as an outlier.

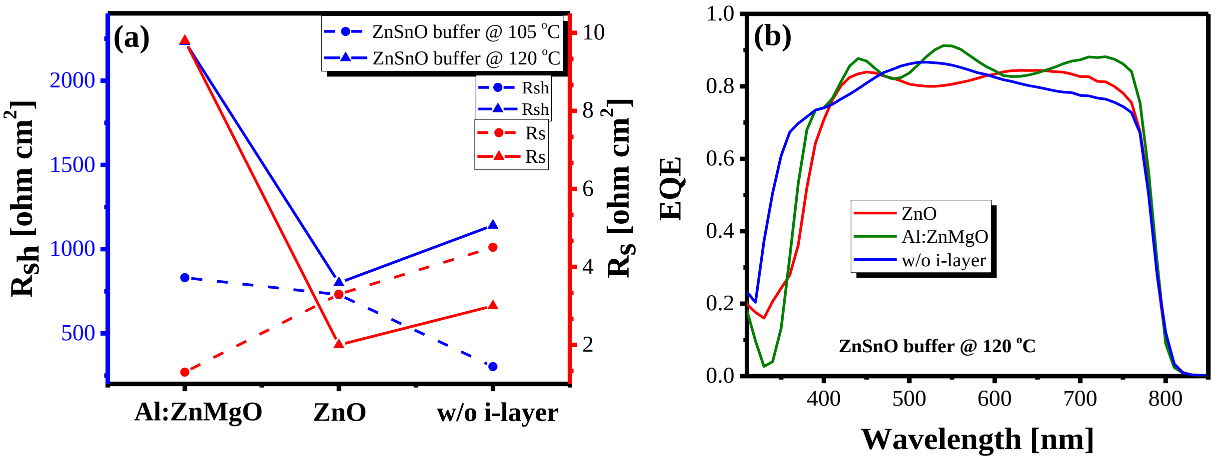


Figure 4.18: (a) *The shunt resistance R_{sh} (in blue) and series resistance R_s (in red) values extracted for the devices made with ZnSnO buffer layer deposited at 105 °C and 120 °C using I-V fit routine [as explained in section 2.1.2]. With each buffer layer, three devices are made with either ZnO or Al:ZnMgO or without i-layers. The dashed lines represent the device with ZnSnO buffer deposited at 105 °C layer and the solid lines represent the device with ZnSnO buffer deposited at 120 °C buffer layer. (b) EQE curve of the $Cu(In,Ga)S_2$ device prepared with ZnSnO buffer layer deposited at 120 °C. The red, olive and blue lines represent the devices prepared with ZnO, Al:ZnMgO and without buffer layer.*

Since the ZnSnO buffer deposited at 105 °C with Al:ZnMgO i-layer performed the best among all the devices prepared with ZnSnO buffer, the device was covered for even higher electrical performance further with MgF_2 ARC coating to decrease the optical losses. A 110 nm thick MgF_2 ARC layer was deposited on the device using e-beam evaporation. The thickness was calculated for minimizing reflections at 610 nm using equation 3.1 according to the procedure described in section 3.1.5. The device I-V and EQE spectrum before and after ARC coating is presented in Fig. 4.19.

Compared to the device without ARC coating, the J_{SC} increased by 1.2 mA/cm^2, FF by 0.5 %, and $V_{OC,ex}$ by 6 mV, all this led to a PCE of 14.8 %, the highest among all the devices prepared using ALD deposited buffer layers. The device was sent for certification to Fraunhofer Institute for Solar Energy Systems.

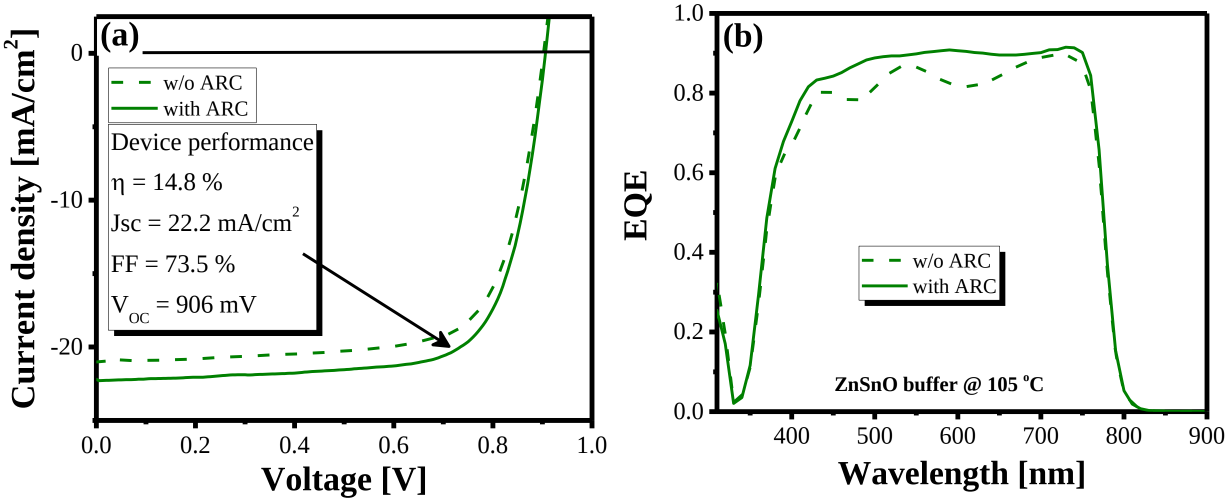


Figure 4.19: *(a) I-V curve and (b) EQE curve of the Cu(In,Ga)*S_2 *device having a PCE of 14.8 % prepared with* $Zn_{0.8}Sn_{0.2}O$ *buffer layer deposited at 105 °C with sputtered Al:ZnMgO i-layer with and without an anti-reflective coating of* MgF_2*.*

At Fraunhofer Institute, a slightly different procedure is used to measure solar cells' device efficiency that displays hysteresis in their I-V characteristics, as the one observed in our solar cells (described in section 4.1.2).). Hysteresis in I-V characteristics means I-V curve in the forward measurement direction, *i.e.* J_{SC} to $V_{OC,ex}$ is not the same as in reverse measurement direction, *i.e.* $V_{OC,ex}$ to J_{SC}. In such devices, to measure the PCE accurately, they use maximum power (P_{max}) point instead of FF to calculate the device efficiency. The PCE is calculated using equation PCE = P_{max}/P_{in} as described in section 2.1.2.

For this, first, the device I-V curve is measured from short-circuit current to open-circuit voltage, and then it is measured in the reverse direction. These are initial scans that help determine the voltage at maximum power point (V_{mpp}) and not the ones represented in Fig. 4.20. The device is then placed at this V_{mpp}, and the voltage is varied further until P_{max} point is obtained; this gives a stable V_{mpp}, I_{mpp} (current at maximum power point), and therefore P_{mpp}. The device is then kept at this voltage for 5 minutes. If no change in V_{mpp}, I_{mpp} is observed, then this point is taken as the maximum power point to compute the PCE of the device. Finally, the I-V curves are measured again, from short-circuit current to open-circuit voltage (red curve in Fig. 4.20), and then it is measured in the reverse direction (black curve in Fig. 4.20). This is repeated several times.

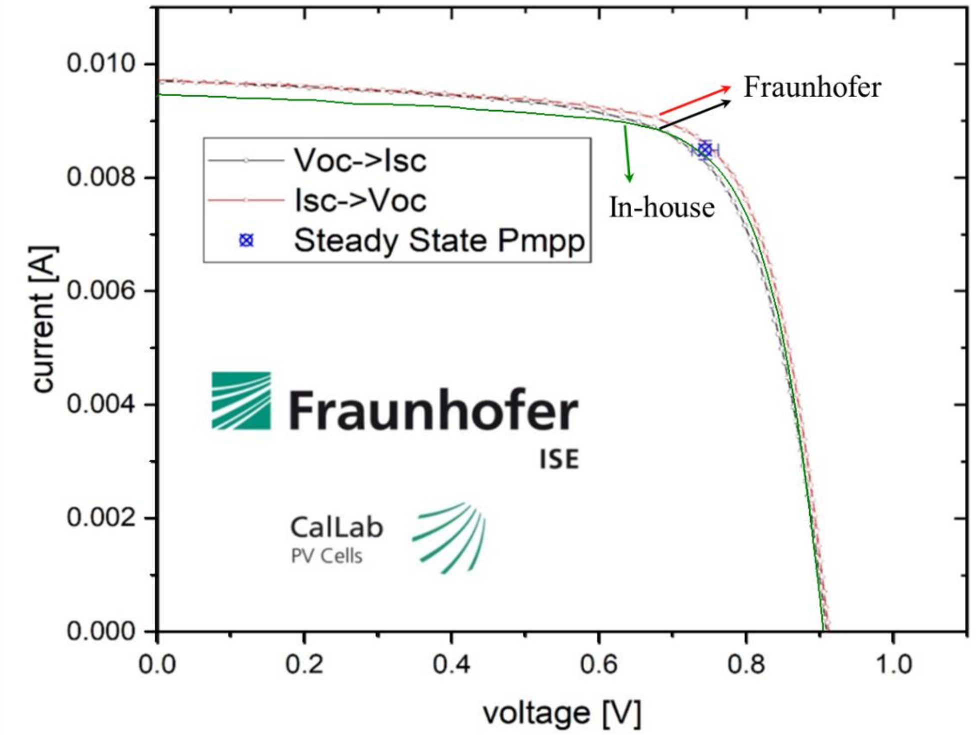


Figure 4.20: *Certified I-V curves of Cu(In,Ga)S_2/ZnSnO/Al:ZnMgO/Al:ZnO 14.0 % efficient device measured at the Fraunhofer Institute for Solar Energy Systems. The red curved is the measurement from short-circuit current to external open-circuit voltage, and the black curve is the measurement from external open-circuit voltage to short-circuit current. The olive curve is the in-house measurement. The blue square point shows the steady-state maximum power point of the device achieved by keeping the device at V_{mpp} for 5 minutes.*

For our Cu(In,Ga)S_2/ZnSnO/Al:ZnMgO/Al:ZnO device, the maximum power point tracking curves are shown in Fig. 4.21. Indeed the device shows a transient V_{mpp} behavior which almost stabilizes after 100 seconds along with the I_{mpp}. It is worth mentioning that the device prior to measurement was illuminated with ~600 W/m² for one h. The device was certified to have a PCE of 13.98 ± 0.39 % using the procedure described above. A $V_{OC,ex}$ of 911.8 ± 9.2 mV and 908.9 ± 9.1 mV and an I_{SC} of 9.71 ± 0.18 mA and 9.70 ± 0.18 mA is reported for the forward and reverse measurement directions, respectively. Similarly, the respective FF was 72.31 % and 69.93 % in forward and reverse measurement directions, respectively. Compared to in-house measurement, the certified device had a higher $V_{OC,ex}$, I_{SC} (see Fig. 4.20) but a lower FF. However, the device had a certified measured area of 0.4517 cm^2, which is 0.02517 cm^2 higher than the in-house measured area (0.425 cm^2). Thus, the certified device had J_{SC} ~21.49 mA/cm^2, which was 0.703 mA/cm^2 lower than the in-house measurement leading to an absolute 0.5 % lower efficiency. The lower J_{SC} is also evident in the EQE of the device (Fig. 4.22). Further, 0.3 % loss can be attributed to a loss in FF of the device, which might have originated from the metastable defects. Nonetheless, until writing this thesis, the Cu(In,Ga)S_2/ZnSnO/Al:ZnMgO/Al:ZnO device holds the record for the second-highest certified PCE for Cu(In,Ga)S_2 devices.

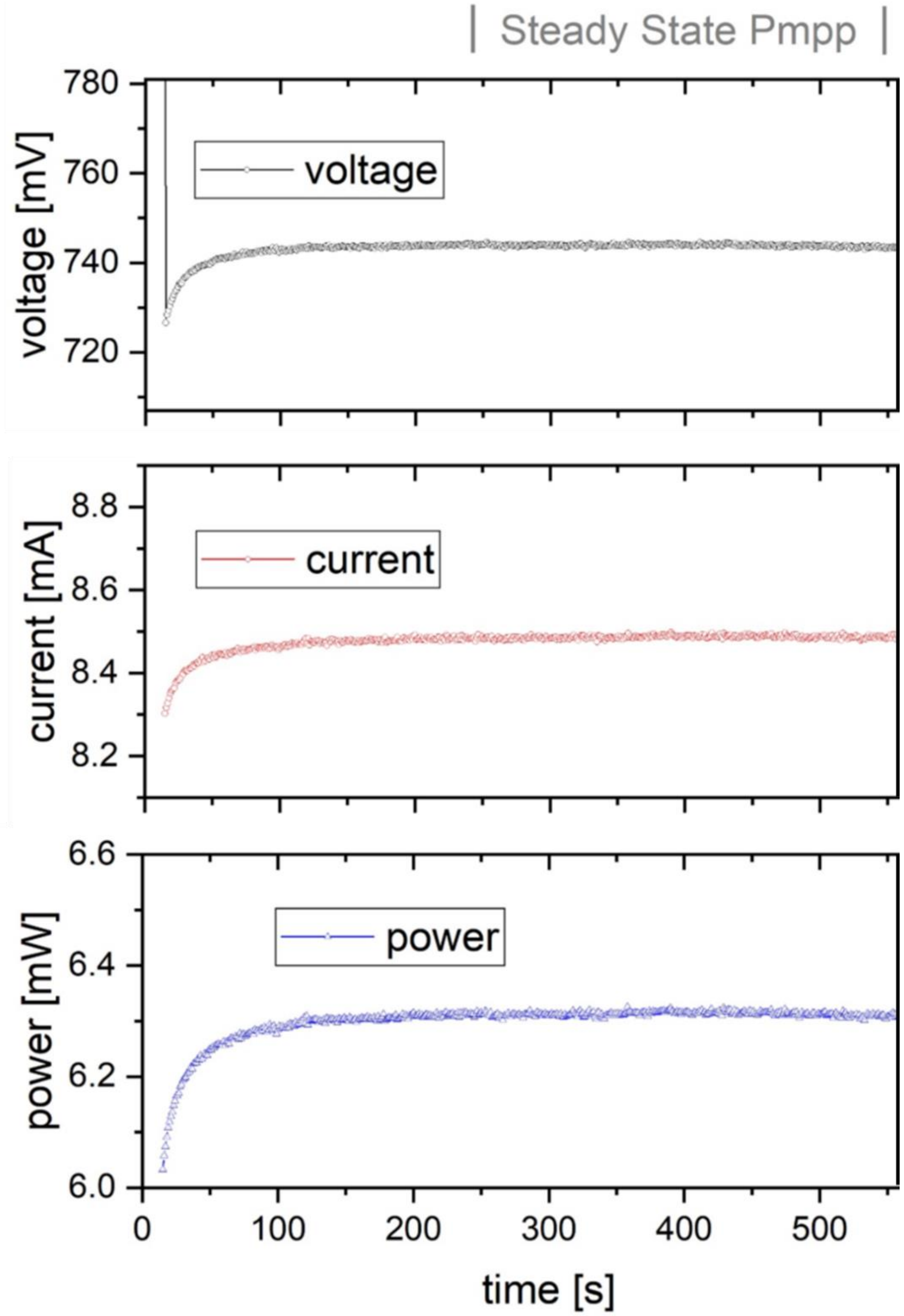


Figure 4.21: Transient curve of voltage (top), current (middle) and power (bottom) at maximum power point for the device under 100 mW/cm^2 illumination.

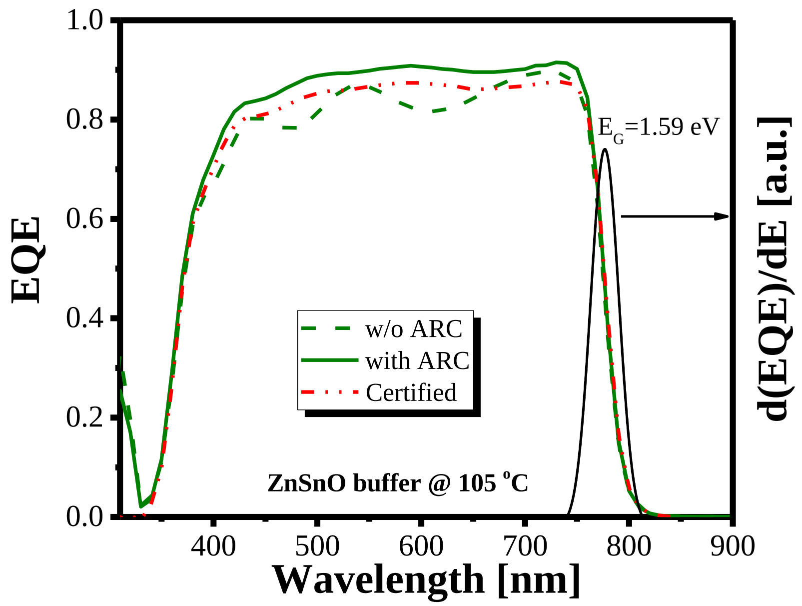


Figure 4.22: *EQE dashed-dot red line of 14 % efficient Cu(In,Ga)S_2/ZnSnO/Al:ZnMgO/Al;ZnO measured at Fraunhofer Institute for Solar Energy Systems. Along with it, the in-lab LPV measurements are also presented in olive, dashed lines represent device without ARC coating and solid lines represent device with ARC coating.*

We would like to report that the PCE of this device degraded over time, which was primarily due to a lower FF and $V_{OC,ex}$. Fig. 4.23a displays the device I-V curves measured after 9 months of storage in the dark in a desiccator under vacuum along with light-soaked curves and the in-house 14.8 % curve. As observed, the device PCE could only be partially recovered using light soaking (see Fig. 4.23a). Slight degradation in EQE was also observed. In fact, all the Cu(In,Ga)S_2 devices presented in this manuscript and even CuInS_2 devices, both Cu-rich or Cu-poor, showed either mild to strong degradations. The origin of these degradations was not investigated in this thesis. We believe the degradation depends on absorber quality as devices with CdS also display a light soaking effect (reported in Appendix Fig. 4.11).

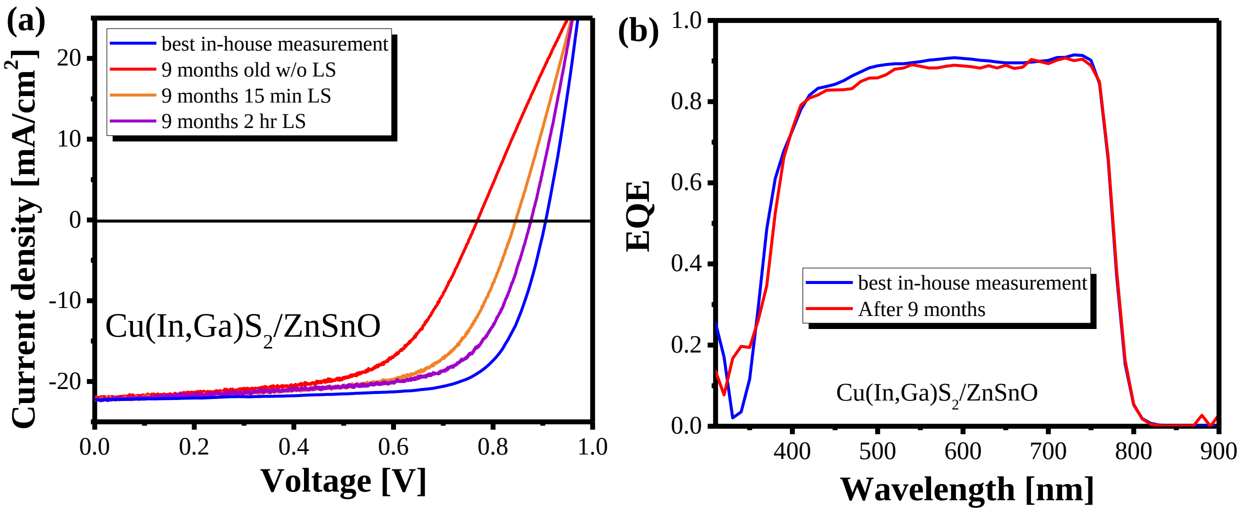


Figure 4.23: *(a) I-V curves of the 14 % certified Cu(In,Ga)S_2 device prepared with ZnSnO buffer layer measured immediately after making the device which gave in lab 14.8 % PCE device (in blue) and after one month with and without the different duration of LS (red, orange and magenta). (b) EQE of the device measured for the 14.8 % PCE device before and after 9 months of storage in a desiccator.*

To summarize this section, atomic layer deposited $Zn_{1-x}Sn_xO$ buffer layer paired with sputtered Al:$Zn_{1-x}Mg_xO$ i-layer delivers certified ~14 % Cu(In,Ga)S_2 devices with E_G ~ 1.59 eV, best among the three i-layer combinations. This is in line with results obtained for Zn(O,S) and ZnMgO buffer layers, where devices with Al:$Zn_{1-x}Mg_xO$ showed superior performance. A significantly low interface V_{OC} deficit is achieved with $Zn_{1-x}Sn_xO$ grown at 120 °C, almost equal to the fully optimized Cu(In,Ga)Se_2 high-efficiency devices.[172]

4.4 Summary of electrical characteristics of Cu(In,Ga)S_2 solar cells

The interface V_{OC} deficit for Cu-rich and Cu-poor Cu(In,Ga)S_2 devices has been found to originate primarily from interface recombinations in the device. For Cu-poor Cu(In,Ga)S_2 a negative CBO at the absorber/buffer interface and a high > -0.40 eV negative CBO at buffer/i-layer interface instigates interface V_{OC} deficit. However, for Cu-rich devices, it possibly originates from Fermi-level pinning.

Except for Cu-poor Cu(In,Ga)S_2/Zn(O,S) device, Cu-poor and Cu-rich Cu(In,Ga)S_2 devices fabricated with CdS and Zn(O,S) buffer layer possessed a very high interface V_{OC} deficit. The deficit originates from interface recombination in these devices, as revealed by an E_a less than the E_G. The significantly low interface V_{OC} deficit in Cu-poor Cu(In,Ga)S_2/Zn(O,S) device is instigated by suppressed interface recombinations as the devices have E_a equal to E_G. These results imply that in Cu-poor devices, interface V_{OC} deficit is linked to interface recombinations and can be mitigated by suppressing these recombinations in the device. In contrast, for Cu-rich devices, the interface recombination possibly originates from Fermi-level pinning at the $Cu(In,Ga)S_2$/buffer interface.

ZnMgO buffer layers with a high CBM also solve the cliff CBO problem in Cu-poor $Cu(In,Ga)S_2$ devices. However, increasing Mg content in the ALD deposited ZnMgO buffer devices above 27 % led to low FF and a high interface V_{OC} deficit in resulting devices, which was higher in ZnO i-layer devices than Al:ZnMgO i-layer devices. Numerical simulations reveal that this originates from a high electron injection barrier height due to a high negative CBO at the buffer/i-layer interface barrier, which is lower in the case of Al:ZnMgO due to its higher CBM. Similar observations are made for ALD deposited ZnSnO buffer devices.

A low positive CBO between $Cu(In,Ga)S_2$ and buffer layer, low negative CBO between buffer and i-layer has been found to yield high-efficiency devices successfully: 15.1 % PCE Zn(O,S) device and 14 % PCE ZnMgO device, in lab, and 14 % PCE ZnSnO device externally certified, by suppression of interface V_{OC} deficit.

Using above observations, the following design principles can be put forward to achieve high PCE devices with low interface V_{OC} deficit: (i) a positive CBO but as low as possible should be maintained between $Cu(In,Ga)S_2$ absorber and buffer, (ii) possibly a flat or a low negative (0 to -0.20 eV) CBO between buffer and i-layer and even i-layer and window layer should be maintained.

Chapter 5

$CuInS_2$ solar cell

In chapter 4, the presence of interface recombination in the Cu-poor and Cu-rich $Cu(In,Ga)S_2$ devices was recognized as the bottleneck for achieving low interface V_{OC} deficit and high efficiency in devices. While for Cu-poor $Cu(In,Ga)S_2$, the problem can be addressed through the use of alternate buffer layers that have optimum band alignment with the Cu-poor devices, the approach is not advantageous for Cu-rich $Cu(In,Ga)S_2$. The results suggest that interface recombinations are might not be caused by unfavorable band alignment at the interface and have alternate origins. This evokes the need to investigate the interface of Cu-rich $Cu(In,Ga)S_2$ solar cells to understand what causes interface V_{OC} deficit.

The omission of Ga from $Cu(In,Ga)S_2$ helps reduce the number of free variables and redundant complexity in understanding the source of interface V_{OC} deficit. In this chapter, the $CuInS_2$ – a simpler alloy system also suffers from interface V_{OC} deficit in Cu-rich devices is studied.[28] Using interface V_{OC} deficit as the figure of merit, the device performance of Cu-rich and Cu-poor $CuInS_2$ solar cells are discussed in section 5.1 to draw parallels with $Cu(In,Ga)S_2$ system. A relationship between the interface V_{OC} deficit and interface recombination *via* I-VT measurements for both Cu-rich and Cu-poor $CuInS_2$ devices is discussed. The interface of $CuInS_2$/Zn(O,S) device is probed with the help of photoelectron spectroscopy with the Zn(O,S) buffer recipe to investigate the band alignment and presence of Fermi-level pining. The results of band alignment facilitate in gaining further insights into the origin of interface recombination in Cu-rich devices. Finally, the surface treatments are explored as an alternate means to reduce interface recombination in Cu-rich $CuInS_2$ solar cells. The transient capacitance measurement uncovers the presence of metastable defects.

Most of the results presented here have been published by us in [183] or are under review [184].

5.1 Interface V_{OC} deficit in $CuInS_2$

In the introduction of this thesis section 1.3, the low mobility of Ga free Cu-poor $CuInS_2$ absorbers was described as the cause of their inferior device performance compared to the Cu-rich $CuInS_2$

counterparts. However, recent findings of A. Lomuscio have established a high concentration of deep defects in Cu-poor $CuInS_2$ absorbers as the fundamental cause of low $V_{OC,in}$ and efficiency in the solar cells.[28] In light of these new results, using interface V_{OC} deficit as the figure of merit, the device performance of Cu-rich and Cu-poor $CuInS_2$ solar cells has been revisited.

5.1.1 Cu-rich $CuInS_2$ vs Cu-poor $CuInS_2$

For Cu-poor $CuInS_2$ absorber deposition, 1-stage and 3-stage growth processes were used, and for Cu-rich $CuInS_2$ absorbers, 1-stage and 2-stage growth processes were used as explained in section 3.1.1. To fabricate working devices, a 10 % potassium cyanide (KCN) etching was performed on Cu-rich absorbers for 5 minutes to eliminate the highly conductive $Cu_{2-x}S$ secondary phase, and a 5 % KCN etching for 30 seconds on the Cu-poor films to ensure reproducible surface conditions.[26, 185] All the absorbers were then transformed into the device using the Zn(O,S) buffer layer together with the standard i-ZnO and Al:ZnO window layer. For Zn(O,S) BR2 recipe (see section 3.1.2) was used as it produces decent PCE solar cells without the need of additional annealing after buffer deposition. This is particularly important for the Cu-rich devices whose $V_{OC,ex}$ reduces significantly upon annealing (see Fig. A4.1c and Fig. A4.2).

Fig. 5.1a shows the I-V characteristics of the best devices prepared from above absorbers except for the 3-stage Cu-poor $CuInS_2$ absorber, which showed major shunting behavior and very poor $V_{OC,ex}$. All other devices exhibit standard diode-like I-V behavior, with the $V_{OC,ex}$, and PCE values comparable to reported high-efficiency $CuInS_2$ devices.[25, 141, 186, 187] The Cu-rich $CuInS_2$ device (2-stage) exhibits a high PCE (table 5.1), even higher than the Cu-poor $CuInS_2$ device. This is in contrast to the $Cu(In,Ga)S_2$ solar cells discussed in section 4.1.1 and even compared to the ternary $CuInSe_2$ solar cells[39], where the Cu-rich solar cells exhibit a lower PCE than the Cu-poor solar cells. This dissimilarity originates from the fact that the Cu-rich $CuInS_2$ absorbers possess a higher $V_{OC,in}$ in comparison to the Cu-poor $CuInS_2$ absorbers. This fact has not been observed for $Cu(In,Ga)S_2$ (see Fig. A5.1) and $CuInSe_2$ absorbers.[28, 83, 88]

Fig. 5.1b shows the bar chart of $V_{OC,in}$ and $V_{OC,ex}$ values of various devices, with the values of and the extracted I-V parameters reported in table 5.1. The 1-stage Cu-rich $CuInS_2$ device possesses the highest $V_{OC,in}$. However, the device fails to translate it into a high $V_{OC,ex}$, observed for the Cu-rich $Cu(In,Ga)S_2$ devices as well. The device thus has the highest interface V_{OC} deficit. The 1-

stage Cu-poor $CuInS_2$ device achieves the lowest interface deficit, signifying the highest interface quality among all the devices, similar to Cu-poor $Cu(In,Ga)S_2$ devices.

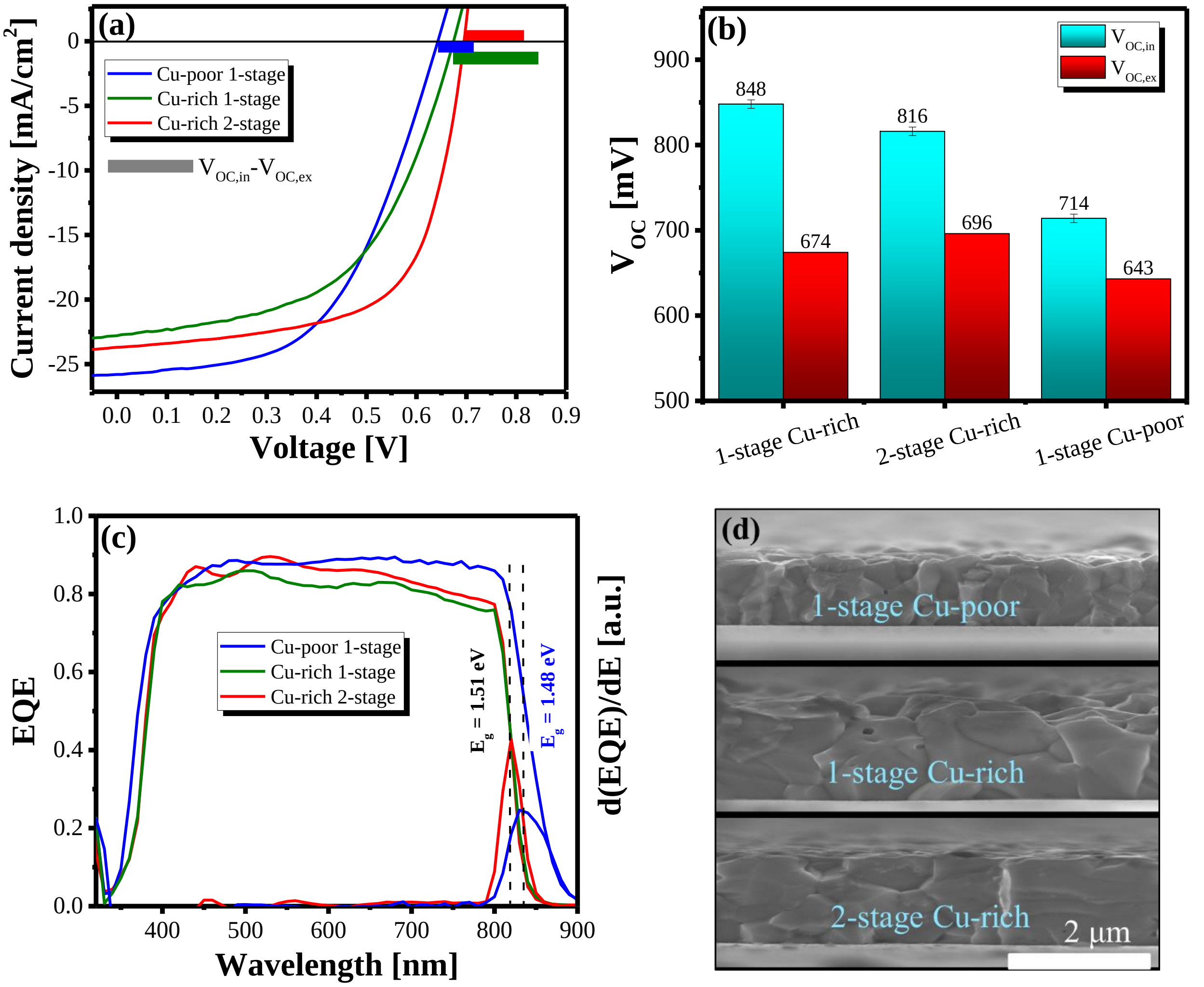


Figure 5.1: *(a) I-V curve (b) bar chart of $V_{OC,in}$ and $V_{OC,ex}$ and (c) Measured external quantum efficiencies of best $CuInS_2$ devices prepared with Cu-poor and Cu-rich as grown absorbers with the different growth process. (d) SEM cross-section images of the Cu-poor $CuInS_2$ absorbers prepared with 1-stage (top) co-evaporation process, Cu-rich $CuInS_2$ absorbers prepared with 1-stage (middle) and 2-stage (bottom) co-evaporation process.*

A smaller J_{SC} for Cu-rich devices is due to a higher bandgap ~1.51 eV possessed by the absorber than a lower bandgap ~1.48 eV possessed by Cu-poor absorbers (see Fig. 5.1c) and poor response in the longer wavelength region of the EQE. The Cu-rich device suffers from a small space charge region or diffusion length that causes a drop in EQE in the longer wavelength region, as explained in section 2.1.3. This fact is supported by the fact that the Cu-rich devices discussed here possess high apparent doping > $1x10^{17}$ cm^{-3}, consequently low SCR. Comparatively, the Cu-poor devices possess low apparent doping ~ $1x10^{16}$ cm^{-3} and hence higher SCR (see Fig. A5.1b).

Table 5.1: *Characteristic of best $CuInS_2$ devices prepared with Cu-poor and Cu-rich as grown absorbers with different growth processes.*

Growth process & [Cu]/[In]	PCE (%)	FF (%)	J_{SC} (mA/cm^2)	$V_{OC,ex}$ (mV)	$V_{OC,in}$ @1sun (mV)	$V_{OC,in} – V_{OC,ex}$ (mV)
1-stage (0.98)	8.8	53	25.8	643	714	71
3-stage (0.94)	–	–	–	–	772	-
1-stage (1.56)	8.1	53	22.8	674	848	174
2-stage (1.75)	10.7	65	23.7	696	816	120

Fig. 5.1d displays the SEM cross-section of the absorbers; the 2-stage Cu-rich absorber has smoother, void-free morphology compared to other absorbers. The presence of smoother surface results in a uniform deposition of Zn(O,S) buffer layer. Therefore, the shunting pathways are reduced in the final device, and consequently, a high FF and high PCE is obtained. Comparatively, the 1-stage Cu-rich absorber has a rough morphology with visible pinholes leading to poor shunt in the device and hence a low FF. The Cu-poor $CuInS_2$ is a different story. The poor FF in this device originates from the presence of a high φ_b^p, which is evident from the I-V measured at lower temperatures (Fig. A5.2c). The barrier results in an additional series resistance and hence reduces the FF of the device (as explained in section 2.2.2).

In summary, owing to a high FF and $V_{OC,in}$ and consequently higher $V_{OC,ex}$, the 2-stage Cu-rich device possesses a much higher PCE than Cu-poor device. However, the device has a higher interface V_{OC} deficit compared to the Cu-poor $CuInS_2$ device, much like the $Cu(In,Ga)S_2$ devices.

5.1.2 Activation energy and interface V_{OC} deficit in $CuInS_2$

The maximum potential of absorbers discussed in the previous section was limited by $V_{OC,ex}$, especially the Cu-rich $CuInS_2$ absorbers just like the $Cu(In,Ga)S_2$. To correlate the low $V_{OC,ex}$ in Cu-rich devices to interface recombinations, the I-VT measurements were performed to reveal the dominant charge carrier recombination mechanism. Fig. 5.2a displays the I-V derived $V_{OC,ex}$ values plotted as a function of temperature. Using linear extrapolation of the $V_{OC,ex}$ values to 0 K as explained in section 2.1.2, the activation energy of the dominating recombination current is extracted. For the 1-stage Cu-poor device, the $V_{OC,ex}$ measurements were performed at smaller steps to generate more points for $V_{OC,ex}$ extrapolation as at lower temperatures the I-V curves show significant distortion (Fig. A5.2c).

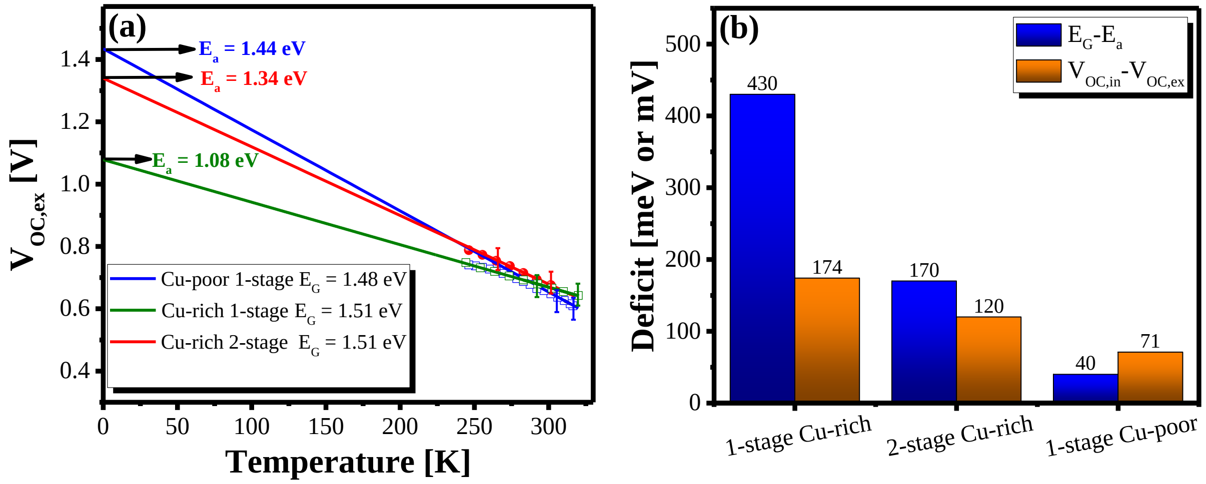


Figure 5.2: *(a) $V_{OC,ex}$ plotted as a function of temperature (b) bar chart showing interface V_{OC} deficit and the deficit between E_G and E_a of best $CuInS_2$ devices with prepared with Cu-poor and Cu-rich as grown absorbers with the different growth process. Arrow bars give the fitting range used to extract the activation energy of the dominant recombination path in the device.*

The three $CuInS_2$ devices: 1-stage Cu-poor, 1-stage Cu-rich and 2-stage Cu-rich exhibit activation energy (E_a) of 1.44 (± 0.05) eV, 1.07 (±0.02) eV and 1.34 (± 0.02) eV respectively for the dominant charge carrier recombination mechanism. The E_a value for both the Cu-rich $CuInS_2$ devices is significantly lower than the EQE-derived bulk bandgap (E_g) of 1.51 eV. This signifies the presence of interface recombination as the dominant charge carrier recombination pathway in these devices. The 1-stage Cu-poor device has an E_a less than E_G. However, the value is closer to the EQE-derived bulk bandgap (E_g) of 1.48 eV, implying the device to be less dominated by charge carrier recombination at the interface. This observation agrees with our earlier results in section 4.1.1, where the Cu-poor $Cu(In,Ga)S_2$ devices were found to be dominated by bulk recombinations. Moreover, Kim et al.[188] also found Cu-poor $Cu(In,Ga)S_2$ devices with a negligible Ga at the front surface are dominated by bulk recombinations. The E_a of the devices also seems to correlate with the deficit between the $V_{OC,in}$ and $V_{OC,ex}$, which can be observed in Fig. 5.2b. The bar chart displays the deficit between the $V_{OC,in}$ and $V_{OC,ex}$, along with the deficit between the E_G and the E_a of the device for absorbers. It appears that as the deficit between the two V_{OC}'s increases along with the deficit between E_G and E_a of the device. In chapter 6, similar observations are made using numerical simulations (see Fig. A6.5).

In summary, the interface V_{OC} deficit increases with the interface recombinations. Moreover, the Cu-rich $CuInS_2$ devices exhibit $E_a < E_G$ suggesting the device is dominated by interface recombinations similar to the Cu-rich $Cu(In,Ga)S_2$ devices.

5.2 Surface band alignment measurements $CuInS_2$/Zn(O,S) solar cells

For Cu-rich $CuInS_2$ solar cells, the $E_a < E_G$ is unexpected, as the BR2 Zn(O,S) recipe should yield a high 'S' concentration in the buffer (see section 3.1.2), and is expected to result in a spike at the $CuInS_2$/Zn(O,S) interface.[102, 143] Still, the E_a values is not shocking, as we have observed this in $Cu(In,Ga)S_2$ devices earlier in section 4.1.1, and have been reported in literature too.[33, 57] As discussed in section 2.1.2, there can be two possible explanations for the $E_a < E_G$, either the $E_{G,IF}$ is less than the E_G, or the Fermi-level is pinned at the interface. The only photoelectron study on $CuInS_2$/Zn(O,S) interface by M. Bar et al.[96] suggests a conduction band spike of 0.1 eV, as expected. However, with this study alone, a presence of conduction band cliff could not be entirely excluded, as the CBO was estimated using the VBO and the optical band gap energies of the $CuInS_2$ and Zn(O,S) bulk and not using the surface bandgap. Thus, there is a probability that the estimated CBO had some errors, as usually the surface bandgap and bulk bandgap are not the same. This was also observed in IPES measurements earlier [98]. Therefore, to conclusively settle the debate, whether the Cu-rich $CuInS_2$/Zn(O,S) devices are limited by interface recombination due to CB cliff at the $CuInS_2$/Zn(O,S) interface or not and also check for Fermi-level pinning, precise band measurements using a combination of photoelectron spectroscopic tools were performed. The relevant results and a comprehensive discussion of this study is presented in this section. The complete study is under review [184].

5.2.1 Photoelectron measurements on $CuInS_2$ device

The photoelectron measurements were performed on the $CuInS_2$ samples prepared by the 1-stage process for Cu-poor and the 2-stage process for Cu-rich absorbers. A specific procedure was followed to prepare samples for photoelectron spectroscopy: as before, first, a 10 % KCN etching was performed on Cu-rich absorbers for 5 minutes to eliminate $Cu_{2-x}S$ secondary phase and a 5 % KCN etching for 30 seconds on the Cu-poor films. Immediately after etching, the absorbers were rinsed and stored in DI water until buffer deposition to minimize air exposure. A thin film of DI water was maintained on the samples even during the transfer of films from DI water into the wet-chemical bath for depositing Zn(O,S) buffer layer BR2 recipe. A thickness series of Zn(O,S) was prepared using the chemical bath deposition (CBD) *via* halting the deposition after 0.5, 1, 2, 4, 10, and 20 minutes that also gives the information regarding the evolution of band bending and the chemical composition. Different deposition times were used to get the core binding energy with and without IIBB, as explained in section 3.3. At the end of each of these durations, the samples were rinsed in a 10 % NH_4OH aqueous solution to avoid uncontrollable precipitation of $Zn(OH)_2$ on the samples, followed by rinsing and storage in DI water until transfer into surface analysis system which was directly connected to a nitrogen-filled glove box.

To transfer the samples into the chamber with minimum air exposure, the samples were taken out of the DI water and with a water layer on top immediately placed into the load lock of the glovebox. The load lock was then pumped down, and the samples were freeze-dried. The transfer of the samples into the surface analysis system for photoelectron spectroscopy measurements took place inside the glovebox, where the samples were mounted onto the sample holders and then transferred into the system. Specific cleaning procedure using a low-energy (50 eV) Ar^+ treatment for 240 min and 40 min for uncovered absorbers and 20 min thick Zn(O,S) buffer covered absorber was applied respectively prior to the UPS and IPES characterization.[104] For HAXPES measurements, the samples were double bagged in the nitrogen atmosphere inside the glovebox, with the outer bag-containing desiccant. These samples were transferred to the SPring-8 system. During this transfer, there was an unavoidable 2-hour exposure of the samples to ambient conditions, accounting for mounting and introduction into the system.

5.2.2 Surface composition of $CuInS_2$ and Zn(O,S)

Let us start by discussing the near-surface composition of the samples, primarily because this affects the interface band alignment significantly. The XPS spectra of the samples are presented in Fig. 5.3, whereas the HAXPES spectra can be found in Fig. A5.3. Both sets of spectra contain elemental peaks corresponding to $CuInS_2$ in the bare and buffer coated absorbers, except for the XPS spectra of 20 minutes thick Zn(O,S) buffer, respectively. On the surface of both absorbers, carbon and oxygen signal is found with Cu-poor containing a higher concentration of oxygen. The origin of these signals might be the contamination of the sample during transfer to the analysis chamber. Fig. 5.4a shows the depth-dependent [Cu]/[In] derived by fitting respective core level peaks with Voigt profiles and linear background.[189] The depth-dependent profile was generated by combining the Cu 2p with the In 3d and the Cu 3p with the In 4d core levels, using their corresponding inelastic mean free path (IMFP) values. The IMFP is “the average distance that an electron with a given energy travels between successive inelastic collisions and is dependent on the attenuating material and the kinetic energy of the photoelectrons."[190] The pairs were chosen so, as they have almost similar IMFP determined using the QUASES IMFP TPP2M code.[191, 192]. The profile exhibits a Cu deficient surface region for both absorbers independent of their as-grown composition. Within error, the two absorbers have almost the same composition near the surface, with the exception of Cu-poor absorbers showing a higher Cu deficiency directly at the surface. A similar Cu-deficiency near the surface is also found for Cu-poor $CuInSe_2$ absorbers compared to Cu-rich absorbers.[193-195]

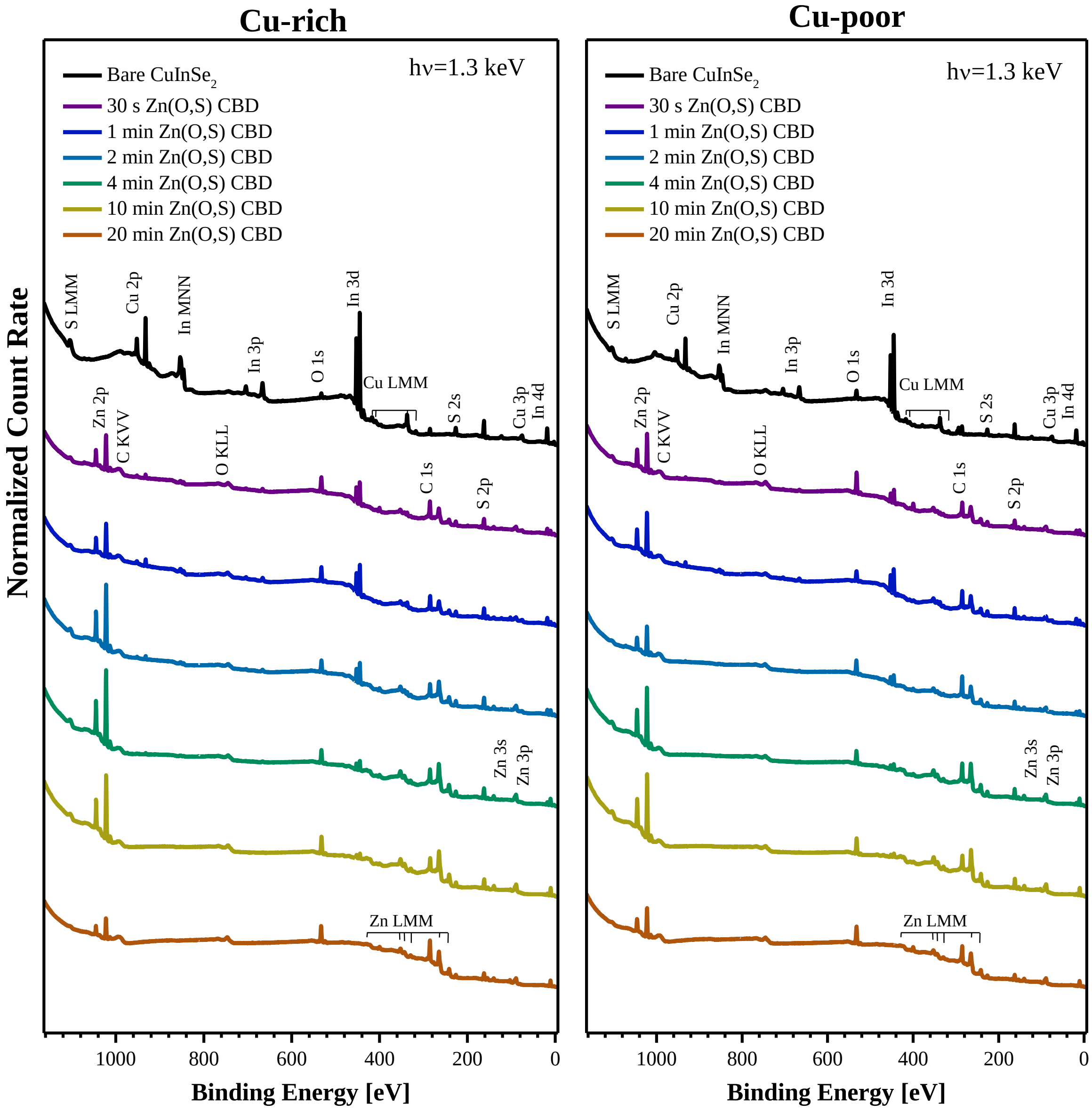


Figure 5.3: *XPS (1.3 keV, Mg K_α) survey spectra of Cu rich (left) and Cu poor (right) $CuInS_2$ absorbers with Zn(O,S) layers deposited using CBD for different durations (30 s to 20 min). Spectra are vertically offset for clarity.*

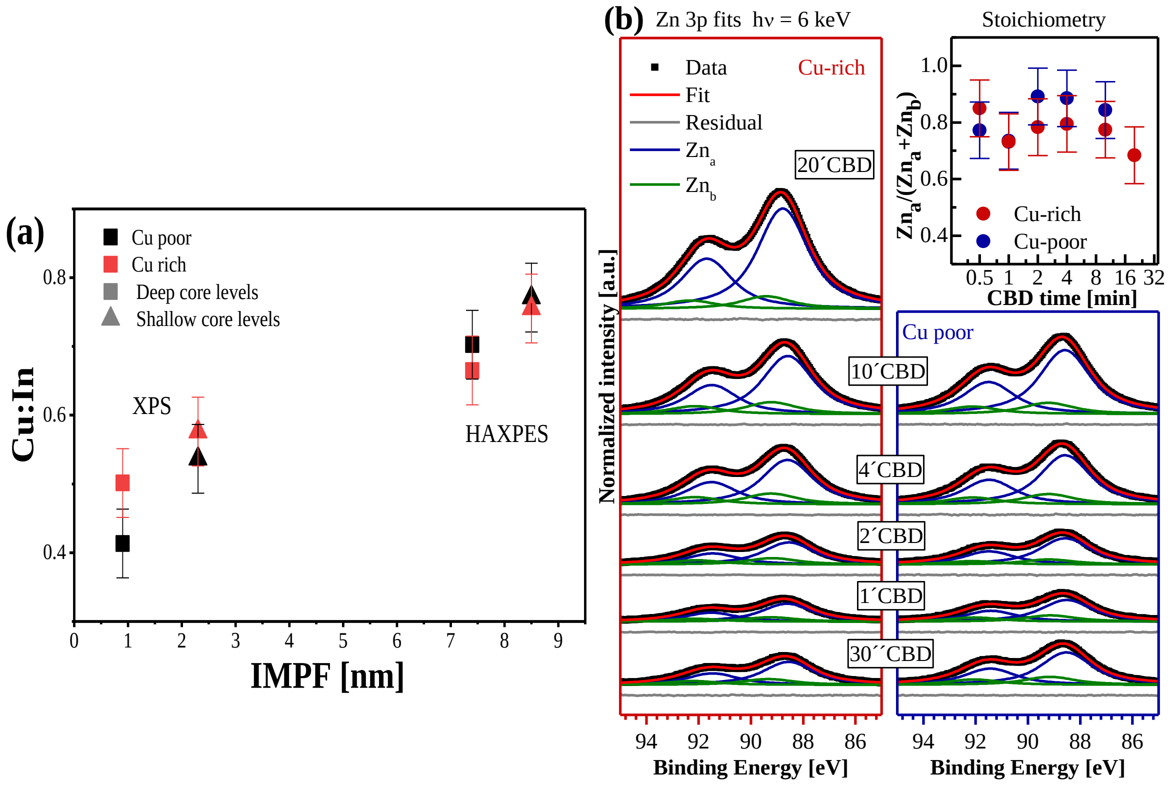


Figure 5.4: *(a) Cu/In ratio depth profile of the Cu rich and Cu poor $CuInS_2$ absorbers. Values are obtained by comparing deep core levels (Cu 2p and In 3d) and shallow core levels (Cu 3p and In 4d) obtained with more surface sensitive laboratory-based XPS measurements and less surface sensitive HAXPES measurements. (b) HAXPES (6 keV) spectra of the Zn 3p peak of Cu-rich (left) and Cu-poor (right) $CuInS_2$ samples with Zn(O,S) buffer layer deposited by different CBD duration (from 30 s to 20 min) as indicated. Data are shown with a linear background subtracted. Fits using pairs of Voigt profiles to represent the respective Zn 3p doublets are displayed along with the data as well as the respective residuals. The calculated $Zn_a/(Zn_a+Zn_b)$ ratio derived from the displayed fits is shown in the top right panel on a semi-log scale.*

Regarding the Zn(O,S) buffer layer, extracting the composition was more complex as Zn(O,S) is composed of ZnS and ZnO, and the binding energy of these species are close to each other. Therefore, HAXPES spectra is used as it offers better resolution compared to XPS. A reasonable fitting of Zn 3p doublet of HAXPES spectra required fitting with two different contributions (see Fig. 5.4b). To extract the value of ‘x’ in $ZnO_{1-x}S_x$, the two peaks were arbitrarily named Zn_a and Zn_b, where Zn_a was assumed to originate from the Zn-S bond contribution and Zn_b from the Zn-O bond contribution. The assumption is justified because it results in a Zn/S ratio of one, agreeing with the formation of the ZnS phase in the Zn(O,S) buffer layer (detailed information is provided in Appendix 5 Fig. A5.4 and Fig. A5.5). The value of ‘x’ was then calculated using the

$Zn_a/(Zn_a+Zn_b)$ ratio assuming 1:1 cation:anion ratio and is shown in the top right panel in Fig. 5.4b. The growth of $ZnO_{1-x}S_x$ seems to be similar on both absorbers with 'x' value between 0.7 at the surface of the buffer and 0.9 at the interface, which is in agreement with the literature report.[142, 144] Thus, a graded Zn(O,S) buffer with a nearly pure ZnS at the interface and increasing oxygen concentration towards the surface is grown on the absorbers.

5.2.3 Band alignment at the $CuInS_2$/Zn(O,S) interface

Fig. 5.5 presents the shift in core level energy, and the interface-induced band-bending (IIBB) extracted from the XPS data. The IIBB values were calculated using the energy shift observed in Cu 2p and In 3d core level relative to the bare $CuInS_2$ absorber giving the band-bending in the absorber. Similarly, the energy shifts in the Zn 2p core level relative to the 20 min CBD Zn(O,S) gave the buffer band-bending. The binding energies used for extracting the IIBB can be found in Table A5.1. The IIBB value was obtained by combining the absorber and buffer band-bending. An average 0.14 eV and 0.22 eV with a respective standard deviations of ±0.08 eV and ±0.02 eV is obtained for Cu-rich and Cu-poor $CuInS_2$ interface respectively.

A positive IIBB value is unexpected, as the formation of a p-n junction naturally would lead to a downward band bending in the upper region of the p-type $CuInS_2$ absorber towards the n part of the junction. The observed shift of the Cu 2p and In 3d photoemission lines with increasing buffer layer thickness to lower BE, displayed in Fig. 5.5, seems to be surprising. However, the shift to lower absorber core level BE can also be interpreted as a reduction of the pre-existing downward band bending at the $CuInS_2$ surface due to buffer deposition-induced passivation of charged defects at the surface. Furthermore, the observed shift, particularly on the Cu-rich sample, indicates that Fermi level pinning is not the problem of the interface with the Cu-rich $CuInS_2$ absorber.

The occupied and unoccupied density of states (DOS), *i.e.* VBM and CBM of the absorbers and the buffer measured with UPS and IPES is presented in Fig 5.6. The linear extrapolation of respective leading edges of Cu-rich and Cu-poor absorber data results in a VBM equal to -0.97 eV and -0.84 eV and a CBM 1.05 eV and 1.16 eV from Fermi level, respectively. Combining these values gives a $E_{G,surf}$ of 2.02 eV and 2.00 eV (± 0.14 eV) for the Cu-rich and Cu-poor absorbers, respectively. As discussed in the previous section, these values are roughly 0.5 eV higher than the bulk bandgap values derived from EQE measurements. Such a bandgap widening towards the surface is not surprising. It has been reported previously for $CuInS_2$ and even in $Cu(In,Ga)Se_2$

absorbers.[196, 197] A significant surface Cu depletion might cause $E_{G,surf}$ widening in chalcopyrite absorbers.[197]

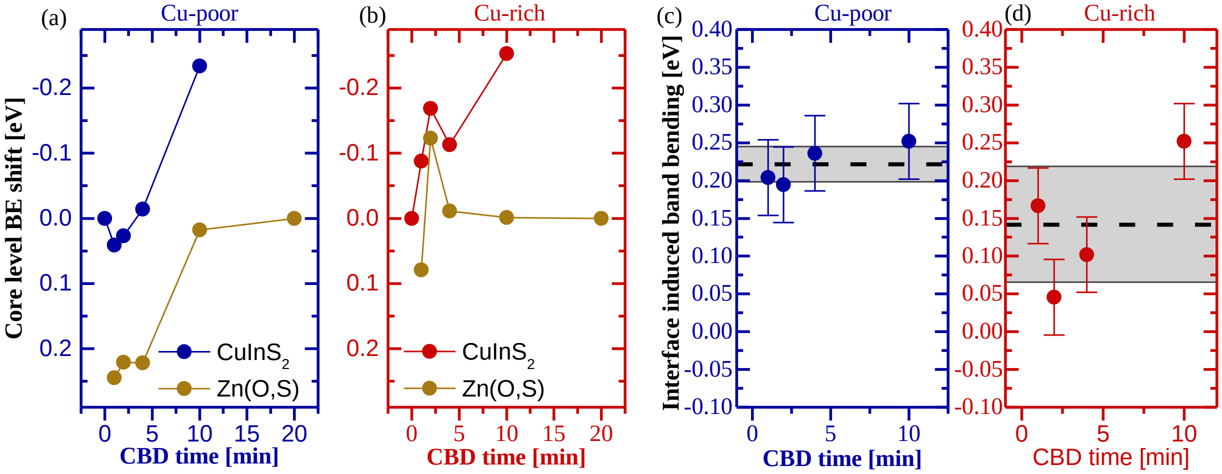


Figure 5.5: *(a) and (b): Binding energy (BE) shifts of absorber (average of Cu 2p and In 3d) and buffer (Zn p) related core levels of the different samples, relative to the bare* $CuInS_2$ *sample and the 20´ Zn(O,S) CBD sample, respectively (all used core level positions can be found in table 6.1). (c) and (d): Total interface induced band bending calculated from a) and b) (see text for explanation). The average of all samples relating to one absorber type (i.e. Cu-poor or Cu-rich) is given as the dashed black line, and the standard deviation of the average is indicated in grey.*

For Zn(O,S), the VBM was calculated to be -1.79 eV and -1.71 eV, whereas the CBM was 1.27 eV and 1.48 eV for Cu-rich and Cu-poor absorbers, respectively. The CBM of Zn(O,S), unlike all other VBM and CBM values, were extracted by a linear extrapolation of the low-intensity tail of the IPES spectrum. This is because the Zn(O,S) thin film is composed of respective ZnO and ZnS binaries, and calculations indicate that ZnO has largely reduced DOS compared to ZnS.[103, 196] Therefore, it implies that the ZnO has a subtle CBM onset compared to ZnS, which manifests itself as a low-intensity tail in IPES measurements. Moreover, the CBM of ZnS is predicted to be located further away from the Fermi level than ZnO.[103] Based on VBM and CBM values, the $E_{G,surf}$ of Zn(O,S) grown on Cu-rich and Cu-poor absorbers is thus found to be 3.06 eV and 3.19 eV (± 0.22 eV), respectively. This value is significantly lower than the bulk bandgap 3.7eV extracted using the Tauc plot (Fig. A5.6).

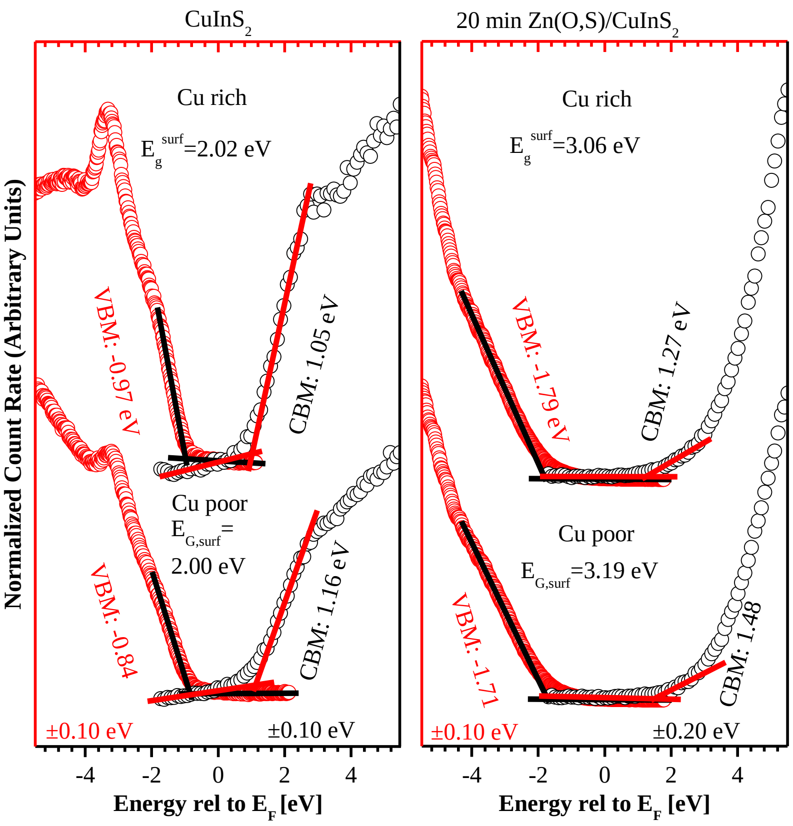


Figure 5.6: *UPS (red) and IPES (black) spectra of Cu- rich (top) and Cu- poor (bottom) bare CuInS2 absorbers without (a) and absorbers with after 20 min CBD Zn(O,S) buffer CBD) (b). All samples were treated with 50 eV Ar+ ions prior to measurements. IPES and UPS spectra are shown on a common energy axis relative to the Fermi level. Solid red (IPES) and black (UPS) lines display the linear extrapolation used for the determination of the valence band maximum (VBM) and conduction band minimum (CBM) energy w.r.t. Fermi level (E_F). The VBM and CBM values, as well as the derived electronic surface band gap ($E_{G,surf}$ = CBM-VBM), are indicated. The experimental uncertainty of the VBM and CBM values of the CuInS$_2$ absorbers and of the VBM value of the Zn(O,S)/CuInS$_2$ samples is ± 0.1 eV, whereas the uncertainty for CBM of Zn(O,S) is ± 0.2 eV.*

Now, having extracted the IIBB, the valence band and the conduction band edge values, the exact VBO and CBO can be calculated using the following formulae:[165]

$$VBO = VBM_b - VBM_a - IIBB \tag{5.1}$$

$$CBO = CBM_b - CBM_a - IIBB \tag{5.2}$$

Where the subscripts ‘a’ and ‘b’ stand for absorber and buffer, respectively. Inserting the IIBB, VBM and CBM values in above equations results in a VBO of -0.96 (±0.16) eV and -1.09 (±0.14) eV and a CBO of +0.08 (±0.24) eV and +0.10 (±0.22) eV for Cu-rich and Cu-poor CuInS$_2$/Zn(O,S) samples, respectively. Fig 5.7 displays the resulting band energy alignment at the

CuInS$_2$/Zn(O,S) interface for both types of absorbers. An ideal band alignment configuration [101, 198] (as discussed in section 2.2.1) with a large valence band cliff and a small conduction band spike at the CuInS$_2$/Zn(O,S) is present for both Cu-rich and Cu-poor samples. Moreover, the presence of IIBB excludes pinning of the Fermi level. Thus, the photoelectron spectroscopy measurements clearly exclude the presence of a cliff at the CuInS$_2$/Zn(O,S) interface and along with the Fermi-level pinning at the interface.

The results conclude that the $E_a < E_G$ in Fig. 5.2 obtained for Cu-rich CuInS$_2$ devices originates neither from unfavorable band alignment at the CuInS$_2$/Zn(O,S) interface nor from the presence of Fermi-level pinning. There must be another origin of interface recombination-dominated devices. Thus, the band alignment measurements necessitate the need to evoke an alternate mechanism for interface recombination.

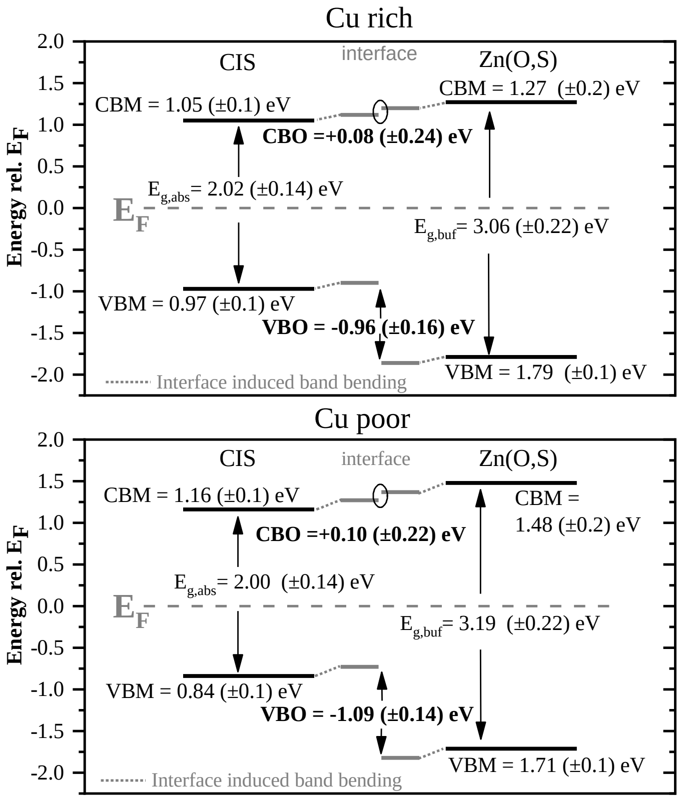


Figure 5.7: *Illustration of the energy level alignment at the Zn(O,S)/CuInS$_2$ interface when using Cu-rich (top) and Cu-poor (bottom) absorbers. The VBM and CBM values are displayed on the left (CuInS$_2$) and right (Zn(O,S)) side. The VB and CB band offsets considering IIBB are displayed in the center.*

5.3 Surface treatments and metastability in $CuInS_2$ solar cell

To comprehend alternate possible cause interface V_{OC} deficit in the Cu-rich $CuInS_2$ devices and reduce it, we performed sulfur-based post-deposition treatments at 80 °C on KCN etched absorbers. The treatment was motivated by the gain in $V_{OC,ex}$ observed with increased thiourea concentration (sulfur source) in chemical bath used for buffer deposition by A. Lomuscio.[26] Since an improvement in the $V_{OC,ex}$ must originate from the passivation of defects, with the help of admittance spectroscopy, it must be possible to investigate the defect responsible for the interface V_{OC} deficit. In the following, S-PDT's effect on the device performance is investigated with the help of I-V, PL, and capacitance measurements. The results of these S-PDTs are published in our work [183].

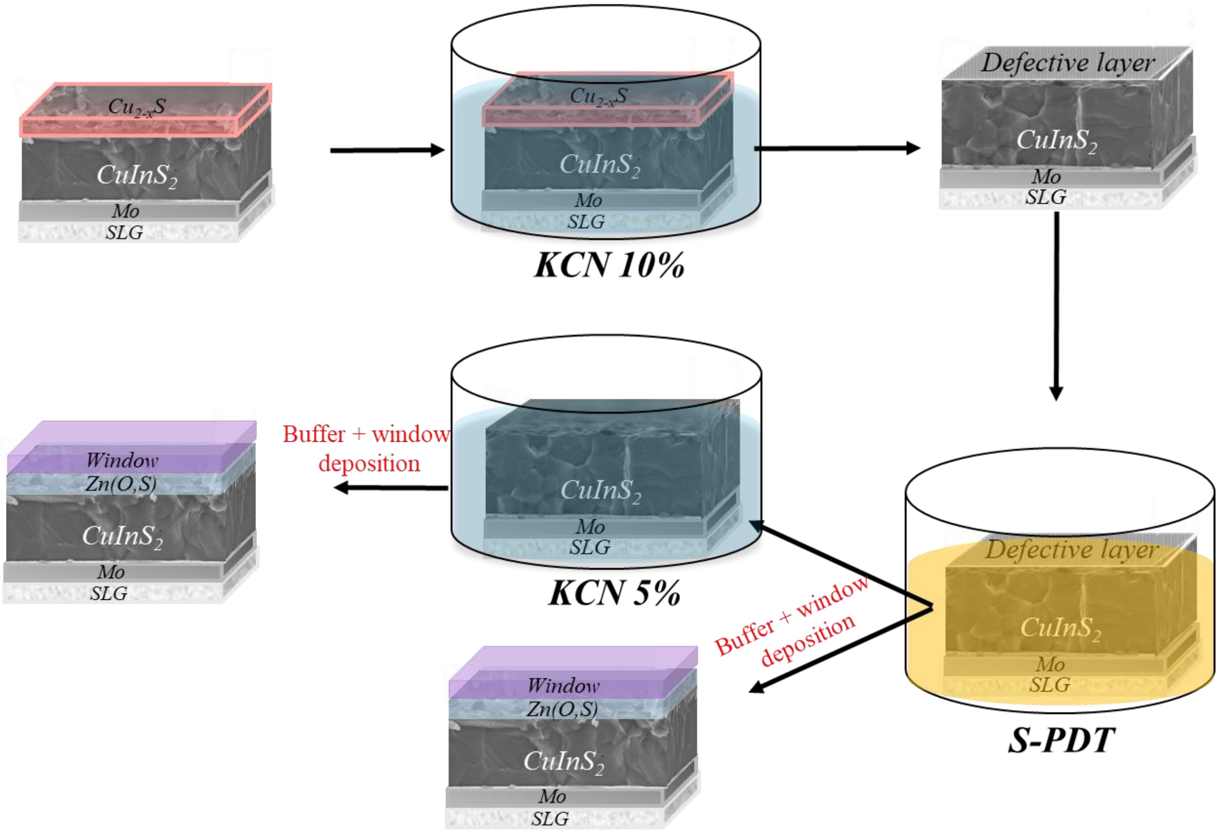


Figure 5.8: *The complete schematic diagram of the procedure used for S-PDT on as grown Cu-rich absorber with $Cu_{2-x}S$ layer on top.*

5.3.1 Influence of S-PDT on $CuInS_2$ device characteristics

For the study, three solutions, namely: aqueous solution ammonium sulfide (AS), sodium sulfide (NaS) and aqueous thiourea (TU) were utilized. The choice of solutions was based on their proven ability of surface passivation treatments on sulfide and selenide absorbers in the past,[26, 199-201] and also because they contain sulfur species. The AS and NaS solutions are known to contain both S^{2-} ions to HS^- ions, and the exact proportion of the two depend upon pH of the solution.[202] On the other hand, the TU solution has an S atom covalently bound to a carbon atom.

The experiments were performed on Cu-rich absorbers grown using the 2-stage deposition process as discussed in section 2.2.1, having elemental composition [Cu]/[In] ~1.7 measured by EDX. A total of seven absorbers grown in the same run were used for these experiments. The complete experimental schematic is presented in Fig. 5.8. A 10 % KCN etching was performed for 5 minutes on absorbers to remove the $Cu_{2-x}S$ phase, as discussed before in section 5.1. Subsequently, the absorbers were subjected to the S-PDT. The exact description of treatment solutions is as follows: DI water (18.2 M-ohm resistivity) aqueous solution of 1. $(NH_4)_2S$ (0.4M), 2. Na_2S (0.4M) in NH_4OH (2M) and 3. CH_4N_2S (0.4M) in NH_4OH (2M), respectively. Each solution was freshly prepared and heated to 80 °C on a hot plate just before the treatment. The six freshly etched absorbers were immersed in these PDT solutions (two in each solution) for a duration of 10 minutes. Afterward, the absorbers were rinsed with DI water, and one absorber from each S-treatment was again subjected to 5 % KCN etching for 30 seconds with the aim to nullify any passivation that might have resulted from the S-PDT. Finally, the seven absorbers were processed into a solar cell with SLG/Mo/$CuInS_2$/Zn(O,S)/i-ZnO/Al:ZnO architecture using the processes described in sections 3.1.2 and 3.1.4. Concerning the calibrated PL measurements, small pieces of absorber from the same run were S-treated separately using the same procedure as described above and were measured before and after Zn(O,S) buffer layer coating.

Let's start by discussing $V_{OC,in}$ measurements. Fig 5.9a gives the bar chart of $V_{OC,in}$ for the absorbers with S-PDT and the untreated absorbers with and without buffer layer. The $V_{OC,in}$ after buffer deposition, is essential to study, as contact is necessary to make the absorber into a solar cell. Regardless of the treatment, the samples display a reduction in $V_{OC,in}$ after buffer layer deposition compared to the $V_{OC,in}$ of the untreated sample. This suggests increased carrier recombination after buffer deposition, in contrast to the observed surface passivation for selenide absorbers.[83, 173] Both NaS-PDT and TU-PDT lead to increased non-radiative recombination in bare absorbers as the $V_{OC,in}$ decreases by 43 mV and 15 mV, respectively, after the treatment. In contrast, AS-PDT leads to no change in recombination activity in the absorber. The higher drop in $V_{OC,in}$ observed after NaS-PDT can be attributed to mechanical degradation of the absorber because during the treatment, the absorber was partially delaminated and flaked off from the molybdenum. Although TU-PDT leads to a reduction in $V_{OC,in}$ before buffer treatment, it proves to be a safeguard against the degradation caused by or during buffer deposition, as the $V_{OC,in}$ does not drop during the buffer deposition after these treatments. Thus, from optical measurements, TU-PDT stands out to be the best among all the treatments.

To better understand whether the difference in recombination activity originated from an improved interface or an improved grain boundary after PDT, cathodoluminescence measurements were performed on untreated and TU-PDT samples by Aleksandra Nikolaeva and Dr. D. Abou-Ras at Helmholtz-Zentrum Berlin für Materialien und Energie, GmbH. The results of these measurements on the TU-PDT absorber did not show observable changes (see Appendix Fig A5.7) in grain boundary recombination compared to the untreated absorber. Thus, it is reasonable to assume that the main effect of the S-PDT is the passivation of defects at or near the buffer/absorber interface and not at the grain boundary. To confirm the improvement at the interface, electrical characteristics are discussed in the following.

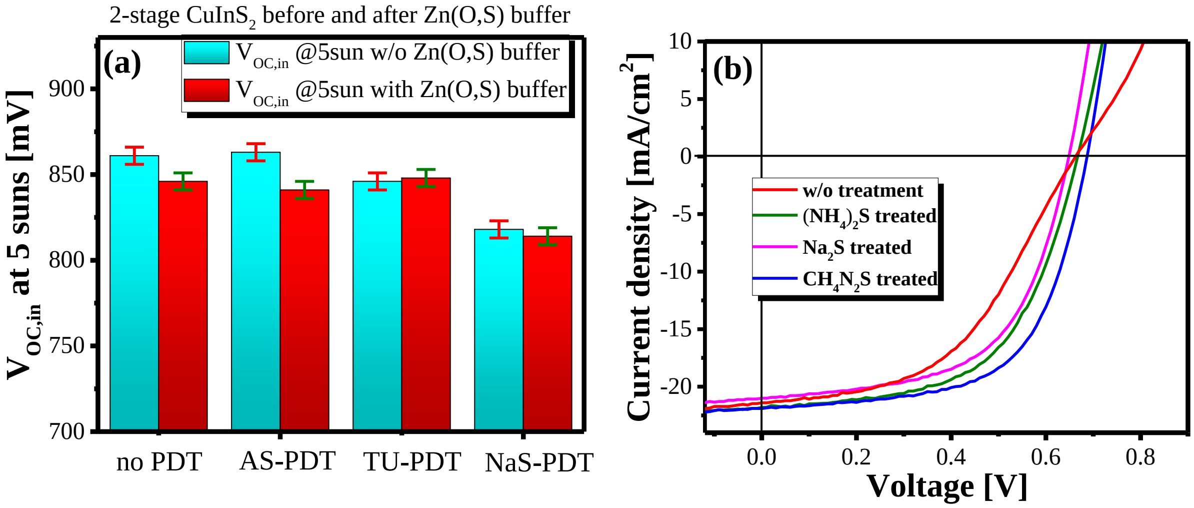


Figure 5.9: *Influence of AS-PDT, NaS-PDT and TU-PDT treatment on (a) $V_{OC,in}$ values of absorbers with and without buffer under 5 sun illumination (b) I-V characteristics of Cu-rich CuInS$_2$ device.*

Table 5.2: *I-V characteristics of best Cu-rich $CuInS_2$ device (scaled to J_{SC} obtained from EQE as explained in section 2.1.3) treated with different S-PDT and untreated devices, along with it are the R_{sh} and $V_{OC,in}$ values. The $V_{OC,in}$ values reported here, were measured for five suns and then corrected to get one sun value as explained in Appendix 4.*

	Efficiency (%)	FF (%)	J_{SC} (mA/cm^2)	$V_{OC,ex}$ (mV)	$V_{OC,in}$ @1sun (mV)	$V_{OC,in} – V_{OC,ex}$ (mV)	R_{sh} (ohm-cm^2)
w/o treatment	6.8	48	21.4	662	806	144	354
AS-PDT	8.3	57	21.8	667	801	134	518
NaS-PDT	8.2	60	21.0	651	771	120	373
TU-PDT	9.2	61	21.9	687	808	121	456

Fig 5.9b shows the I-V characteristics of the untreated and as-treated devices without the second etching step. The extracted device I-V characteristic parameters and the $V_{OC,in}$ values at one sun are reported in table 5.2. The $V_{OC,in}$ value at one sun, was determined from the five sun $V_{OC,in}$ values (explained in Appendix 5) measured on absorbers with Zn(O,S) buffer layer. The shunt resistance reported in the table was determined from the slope of the illuminated I-V curve in the -0.2V to 0.0V range in reverse bias.

It is clear from the device I-V characteristics that the S-PDT devices have superior performance compared to the untreated device, majorly because of its low FF. Moreover, the I-V curve of the untreated device stands out because of its uncharacteristic ‘S shape’, which is why the device exhibits a low fill factor (FF) and consequently the lowest PCE. The origin of this ‘S shape’ is characteristic of a carrier transport barrier in the device (as discussed in section 4.2.4) and can be caused by a large band offset at the absorber/buffer or buffer window interface or due to the presence of a ‘p^+ layer’, and can even a combination of both.[45, 99, 170, 173, 203, 204] However, the ‘S shape’ is nonexistent in the S PDT devices. Thus, the band offset alone can be ruled out as the root of the ‘S shape’ in I-V curves as all the devices were prepared in the same buffer and window run. However, a combination band offset with a process that leads to a reduction in electron Fermi-level, for example, the presence of acceptor defects (p^+ layer), could lead to a large φ_b^p and hence ‘S shape’ in I-V curve. Moreover, the photoelectron study confirms a small conduction band spike of 0.1 eV at the $CuInS_2$/Zn(O,S) interface (see section 5.2), with such a low conduction band spike alone, an ‘S shape’ is not feasible (see section 4.2.4). The I-V results thus suggest the presence of a ‘p^+ layer’ in the absorber that is passivated by S-PDT.

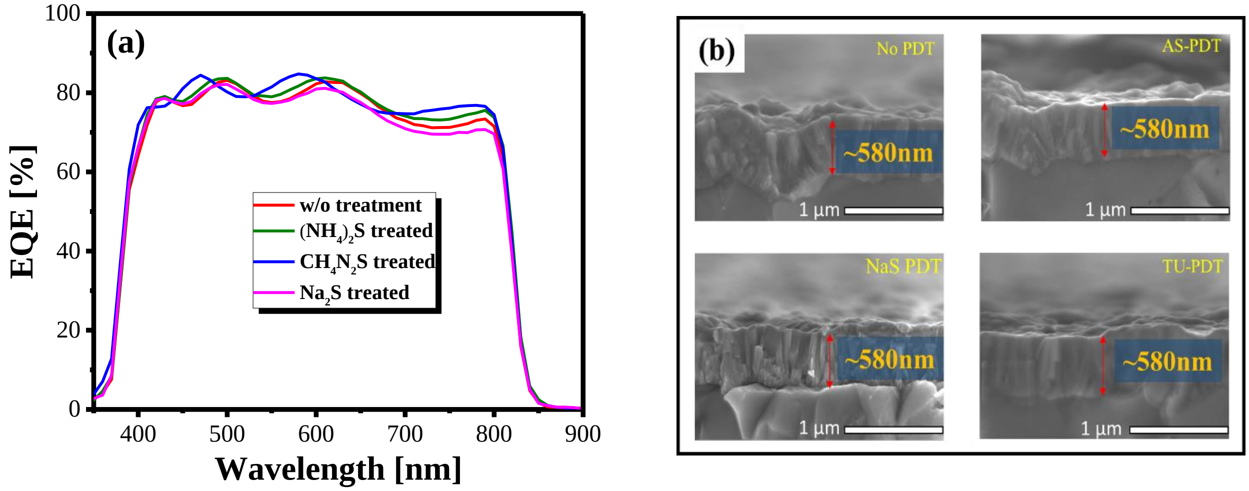


Figure 5.10: *(a) Measured external quantum efficiencies (b) SEM cross-section images of the $CuInS_2$ devices without any treatment and with AS-PDT, NaS-PDT and TU-PDT.*

The S-PDT also increases the J_{SC} in the treated devices except for the NaS-PDT device. This improvement is a consequence of increased EQE in the long-wavelength region. However, the J_{SC} of all devices still remained below 80 % of the Shockley-Queisser limit.[177] This could be understood with the EQE measurements. Fig. 5.10 shows the EQE of the four devices, which on average remains lower than 80 % for each device. A major reason for the low EQE is that the devices possess a very smooth surface, as seen in the SEM cross-section in Fig. 5.10b. This leads to strong light reflection and even to an interference pattern in the EQE, which originates from the interference of waves reflected from multiple interfaces in the device structure. This causes an overall EQE loss by optical reflection (mechanism three as explained in section 2.1.3). Moreover, for all the devices, the EQE is relatively lower in the long-wavelength region compared to the short- wavelength region. A low diffusion or SCR can be the root of this. All the devices discussed here possess a high doping > 1e17 cm^{-3} and consequently low SCR (see Appendix Fig. A5.8). Thus, a low EQE of devices at high wavelengths indicates that the devices suffer from low carrier diffusion length. In fact, these Cu-rich devices were found to possess a very low lifetime, less than even one nanosecond,[205] which probably leads to the low carrier diffusion length.[49]

Compared to the rest of the devices, the TU-PDT devices exhibit a shift in interference patterns visible in EQE. The shift could have resulted from a thinner Zn(O,S)/TCO stack thickness or a change in the optical properties of the absorber surface. However, the SEM cross-section of the devices Fig. 5.10b shows an average thickness of 580 nm for the Zn(O,S)/TCO stack for all the devices independent of the PDT. This eliminates the changes in Zn(O,S)/TCO stack properties as the possible cause of EQE variations in the devices. Therefore, the optical properties of the absorber surface may have been modified either by the surface chemistry or by deposition of an additional layer. The surface analysis by XPS measurements of absorber with TU-PDT displays the presence of a second S compound other than one corresponding to $CuInS_2$, confirming the presence of a layer on top of the absorber surface (see Appendix Chapter 5 and Fig. A5.9). Not only does this layer explain the shift in EQE peaks, it might also be the reason why the $V_{OC,in}$ does not degrade in the TU-PDT absorber after the buffer deposition.

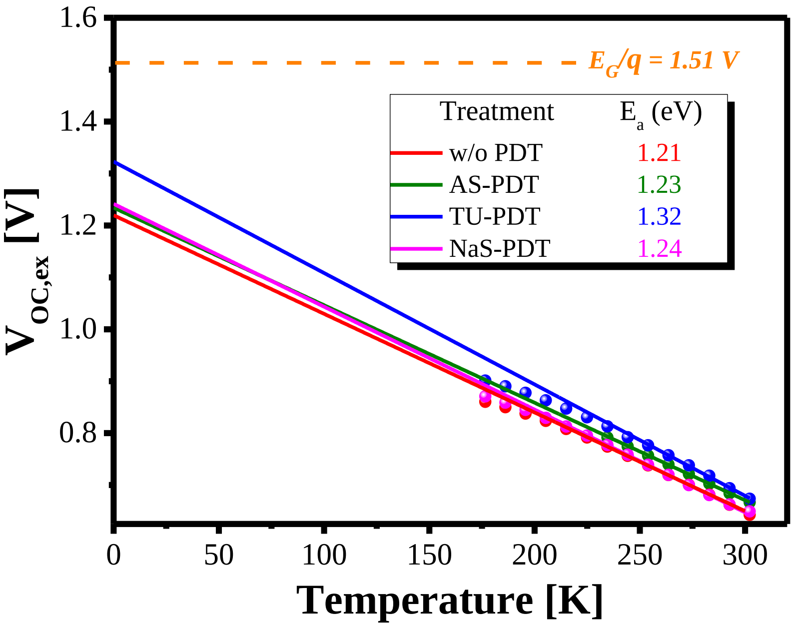


Figure 5.11: *The $V_{OC,ex}$ plotted as a function of temperature for the $CuInS_2$ devices without any treatment and with AS-PDT, NaS-PDT and TU-PDT.*

5.3.2 Cause of improvement in interface V_{OC} deficit

Among all S-PDT devices, only TU treated devices displayed an improvement in the $V_{OC,ex}$. For the AS treated device, the $V_{OC,ex}$ remains on par, and for NaS treated, even lower as compared to untreated device. Prima-facie, it seems that only TU-PDT reduces the interface recombination. However, a comparison of the interface V_{OC} deficit of the devices shows an improvement in interface recombination with all PDTs. The AS-PDT shows the highest interface V_{OC} deficit after the untreated device. In contrast, both NaS and TU-PDT show slightly lower interface V_{OC} deficit (see table 5.2). This suggests that these treatments lead to passivation of defects states at or near the interface, TU-PDT leading to highest passivation followed by NaS-PDT and AS-PDT.

This trend is further supported by the temperature-dependent $V_{OC,ex}$ measurements. Fig. 5.11 shows the $V_{OC,ex}$ extracted from I-V measurements performed at different temperatures for the untreated and S-PDT devices. For all the devices, the E_a of the dominant recombination path remains lower than the E_G of the absorber, indicating dominating recombinations at the absorber/buffer interface. The E_a does increase with the S-PDT, particularly for TU-PDT, suggesting a reduction of non-radiative recombinations at the interface (as observed with numerical simulations in section 6.3). Thus signifying that TU-PDT leads to a reduction in defects at or near the interface the most.

Above analysis explains why we observe an improvement in interface V_{OC} deficit. However, it is unclear how these PDTs work. Even though the three S-PDTs have equal sulfur concentration, each S-PDT has shown a different impact on the device properties. The TU-PDT stands out for being the most effective of the three S-PDTs. The key to understanding why this is the case lies in three parameters: 1. the exact sulfur species in the solution, 2. the solution pH and 3. the cations present in the solution. These parameters are listed out in table 5.3 for each solution. The AS and NaS-PDT solutions have the same sulfur source (S^{2-} anion), whilst TU-PDT has S atom covalently bound to a carbon atom. Concerning the AS and NaS-PDT that contain the same sulfur source, NaS-PDT has a higher proportion of S^{2-} ions to HS^- ions because of its higher basicity compared to the AS PDT.[202] Moreover, the Na_2S solution also contains very mobile Na^+ cations which can aggregate at the grain boundaries or Cu sites.[206] Both; higher S^{2-} anion concentration and Na^+ cation concentration could be the potential reason for the surface passivation and consequently a lower interface V_{OC} deficit in the NaS-PDT device.

Table 5.3: *Summary of sulfur-post deposition treatment conditions and chemical species present in each solution*

PDT	**Sulfur source**	**Cations**	**Anions**	**PDT pH**
AS	0.4M S^{2-}, HS^-	0.8M NH_4^+	-	9.1
NaS	0.4M S^{2-}, HS^-	2M NH_4^+, 0.8M Na^+	2M OH^-	13.2
TU	0.4 M $S=C(NH_2)_2$	2M NH_4^+	2M OH^-	11.6

Understanding how TU-PDT leads to surface passivation is a bit more complex, as TU dissociation in the solution has been controversial. In earlier studies, the release of sulfur ions in basic solution was thought to be *via* HS^- dissociating into S^{2-} anion.[207, 208] However, recent studies suggest that TU dissociation only takes place after forming a complex with a metal cation.[209] This means that the TU (CH_4N_2S) molecule first diffuses to the absorber surface and then physisorbs or reacts at the surface. In fact, the XPS analysis of the TU treated absorber shows the presence of additional peaks in the S 2p spectra, other than the peaks corresponding to $CuInS_2$.[183] These additional peaks were found to be compatible with an organic sulfur species (likely relating to TU), and was absent in the untreated and the AS treated absorber, further supporting the claim of TU physisorption on the absorber surface. Thus, the TU-PDT seems to form a protective barrier layer at the absorber surface, preventing the $V_{OC,in}$ degradation during Zn(O,S) deposition. Additionally, the layer also passivates the surface defects, thereby reducing interface V_{OC} deficit and improving the FF in the device.

It is now clear that the S-PDT passivates defects at or near the interface and improves the interface V_{OC} deficit and FF. Moreover, the 'p^+ layer' (also called as a defective layer here) has been evoked as the cause of the 'S shape' in the I-V curve of the untreated device. But, what causes the interface V_{OC} deficit and the 'S shape'?

As discussed in section 2.2.3, for $Cu(In,Ga)Se_2$, the defective layer has been explained as a highly doped (at least one order magnitude higher than bulk) thin layer (few nm) near the absorber surface.[210, 211] The existence of the double vacancy defect (V_{Cu} and V_{Se}) has been evoked as the cause of the existence of this layer.[212] The studies by Elanzeery and Colombara et al. confirm the presence Se related vacancy defect near the surface of Cu-rich $CuInSe_2$ caused by KCN etching.[213, 214] Moreover, Elanzeery also showed that the defect could be created in Cu-poor devices by strong 10 % KCN etching.[46] In literature, mitigation of the defects in the defective layer has been reported by light soaking the device under open-circuit conditions.[9, 103, 114, 136, 210, 215-219] Such a light soaking (LS) treatment was also applied to the untreated device, and indeed LS removed the 'S shape' (Fig. 5.12a). However, when placed in the dark for several hours, the device was brought back to the initial state, *i.e.* with the 'S shape'. This indicates that the involved defects show 'metastable' behavior. Hence, it is safe to assume that an S-related vacancy defect might also be present in the $CuInS_2$ system resulting in 'S shaped' I-V curves and is caused by KCN etching.

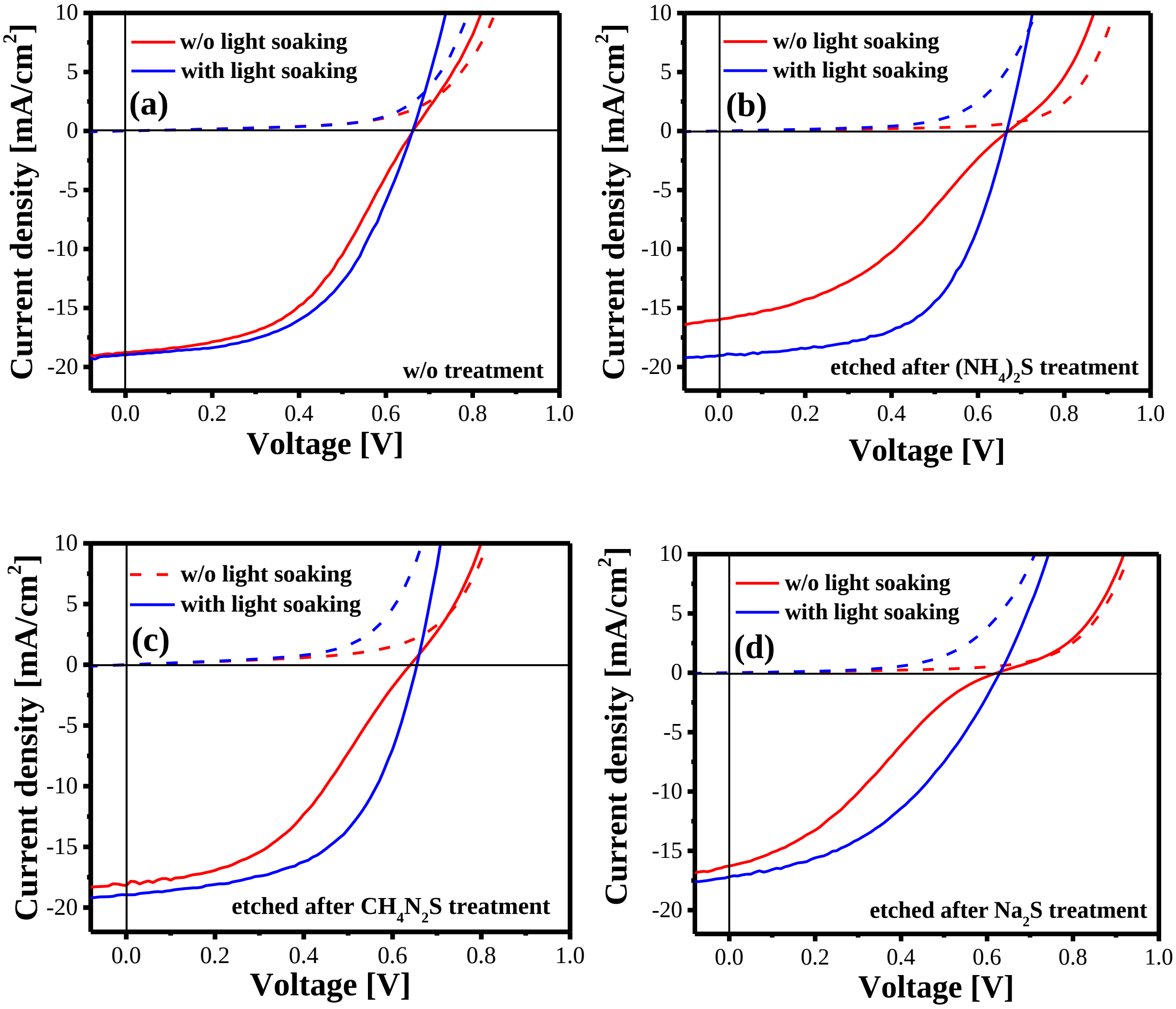


Figure 5.12: *I-V curves of (a) untreated (b) AS-PDT (c) NaS-PDT and (d) TU-PDT Cu-rich* $CuInS_2$ *device prepared with the second KCN etching step. The 'S shape' visible in all the devices disappears after light soaking (LS).*

So far, it seems that the S-PDT leads to passivation of KCN etching induced near-interface defects, albeit partially (as even the S-PDT devices show a slight improvement in FF after light soaking, see appendix Fig. A5.10). If this is true, the passivation could be reversed by performing a second KCN etching step. And indeed, the I-V curve of all the post S-PDT KCN etched devices exhibit the 'S shape' as can be seen in Fig 5.12. Like the untreated device, the 'S shape' disappears after 30 minutes of LS under open-circuit conditions. This observation suggests that the Cu-rich $CuInS_2$ devices also suffer from metastable defects that seem to originate from KCN etching, much like the Cu-rich $CuInSe_2$ device.[74] It must be noted that in our case, even a soft KCN etching 5 % for 30 seconds is enough to reverse the effects of passivation. This might be attributed to the weak passivation by S-PDTs. Nonetheless, the passivation of near interface defects *via* S-PDT confirm the defect to be related to S-vacancy.

5.3.3 Capacitance transient in $CuInS_2$ solar cells

Having established the presence of the defect near the interface, it is imperative to shed light on the characteristics of this defect. A direct method of probing the defects in SCR is admittance spectroscopy; however, the 2-stage Cu-rich $CuInS_2$ device exhibit no clear signature of a deep or semi-deep defect in the admittance spectra and neither a change in activation energy of the admittance step (see appendix Fig. A5.11). This despite the fact that PL measurements were done by Lomuscio et al. display the presence of deep defect signature ~0.9 eV (see appendix Fig. A5.11 and [28]). Therefore, the time-evolution of SCR width of untreated device and TU-PDT device was measured and analyzed as an indirect method to probe the impact S-PDT particularly TU-PDT on the defects. The inverse of measured capacitance was used to transform it into apparent SCR width by rewriting equation 2.24 as:

$$x_{app}(t) = \frac{\varepsilon_r \varepsilon_0}{C_{SCR,app}(t)}$$

where, $C_{SCR,app}(t)$ and $x_{app}(t)$ are the transient capacitance and apparent SCR width, respectively. The device transients are measured by first illuminating the sample with a certain light intensity for 300 seconds and subsequently keeping it under dark for 300 seconds. The entire measurement method is explained in detail in the Appendix A5. The $C_{SCR,app}(t)$ includes the contribution from SCR of absorber, buffer and front contact. However, only slow metastable changes in capacitance is discussed. Therefore this fact will be overlooked here.

Fig. 5.13a and b display the SCR transients of the two devices. Under illumination near t=0 seconds for all the devices, constant x_{app} is obtained, suggesting saturation of trap states (by trapping of charge carriers), independent of the illumination intensity. After switching off the illumination, an increase in x_{app} is observed (due to de-trapping of charge carriers), reaching a constant value after 300 seconds. At this point, the device is in a new certain quasi-steady state. The difference between the x_{app} at t=0 seconds and t=300 seconds increases with the increasing illumination intensity for both devices. Immediately after switching off the illumination, the x_{app} increases abruptly [Fig. 5.13a], as the excess of light generated carriers recombines. This fast increase in SCR width in this device decreases with the increase in illumination intensity. This is a consequence of the trapping of excess charge carriers in the deep recombination centers, which release these charge carriers slowly (in the order of 10s of seconds), as can be seen in the slow tail of the capacitance transient. The magnitude of this slow tail increases with increasing illumination intensity as more and more photogenerated charge carriers are trapped in these ‘slow’ defects.

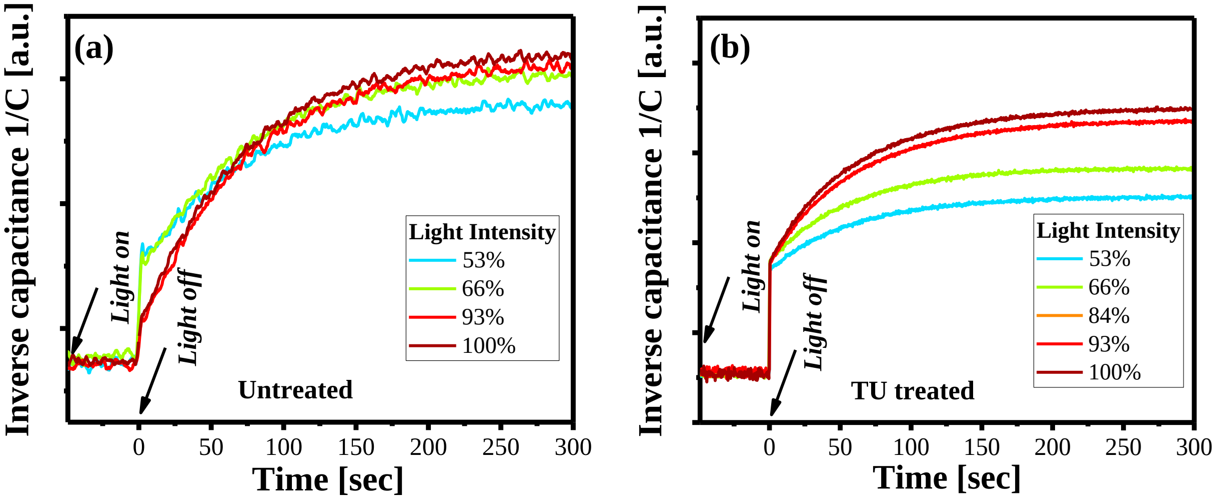


Figure 5.13: *Time evolution of inverse of capacitance (apparent SCR width) for different illumination levels for the untreated device and TU treated device (a) and (b), respectively. The respective transient curves are shifted to an equal transient capacitance value at t = 0 seconds. The transients are measured at different illumination levels under short circuit conditions, with 100 % light intensity corresponding to 1 sun intensity. The device transient was measured by keeping it under illumination for 300 seconds and subsequently in the dark for 300 seconds.*

Concerning the TU-PDT device, the abrupt change in x_{app} at t=0 seconds is equal for each illumination intensity (Fig. 5.13b). It is a direct consequence of the passivation of the slow defects. The entire process can be understood as follows: In the untreated device, the ‘slow’ defects trap charge carriers more so with increasing illumination intensity. At t=0 seconds in the dark, the jump in x_{app} can be attributed almost entirely to the free carriers, and the transient back to the dark state to the slow defects. On the contrary, the passivation of these slow defects in TU treated device results in much lower carrier trapping. However, the slow transient after t=0 seconds and an equal x_{app} jump independent of illumination intensity suggests partial trapping of photogenerated carriers in the device. Moreover, an increase in the magnitude of this slow response with increasing intensity indicates that carriers are still trapped in these slow metastable defects, showing that the slow defects remain even after the TU-PDT.

To confirm KCN etching as the origin of near-surface defects in the device, the transient capacitance measurements were also performed on post TU-PDT KCN etched device. The capacitance transients of this device are similar to the untreated device (see appendix Fig. A5.12).[183] This confirms that the KCN etching is the origin of slow metastable defects in $CuInS_2$ solar cells and can even remove the beneficial passivation effects of S-PDT.

To summarize, the S-PDT, particularly TU-PDT, improves the interface VOC deficit and FF, thereby improving device performance. The improvement was linked to the passivation of defects at or near the interface, which was indicated by an increase in E_a of the charge carrier dominant recombination path. The light soaking and capacitance transient measurements suggest the presence of metastable defects in the devices originating from KCN etching. The results establish the KCN etching leading to S-related vacancy defect as the root of interface V_{OC} deficit and poor FF in the device.

5.4 Summary of electrical characteristics of $CuInS_2$ solar cells

Similar to the Cu-rich $Cu(In,Ga)S_2$, the Cu-rich $CuInS_2$ devices suffer from interface V_{OC} deficit linked to interface recombinations due to the presence of defects at or near the interface. The investigation of electrical device performance combined with $V_{OC,in}$ measurements of $CuInS_2$ devices suffering has been presented.

The comparison of electrical characteristics of Cu-rich and Cu-poor $CuInS_2$ solar cells with a Zn(O,S) buffer has shown that the Cu-rich $CuInS_2$ solar cell suffers from significantly higher interface V_{OC} deficit even though the devices deliver superior device performance. As observed previously,[32] the temperature-dependent $V_{OC,ex}$ measurements reveal that interface recombinations limit the Cu-rich devices. The E_a of the dominant recombination path was found to have a correlation with the interface V_{OC} deficit. The Cu-poor $CuInS_2$ devices had the highest E_a and consequently the lowest interface V_{OC} deficit, whereas, for Cu-rich $CuInS_2$, the deficit increased with decreasing E_a of the device.

A combination of photoelectron spectroscopic measurements performed on $CuInS_2$/Zn(O,S) devices demonstrated a positive conduction band offset of 0.1 eV at the $CuInS_2$/Zn(O,S) interface independent of the absorber composition. Furthermore, the significant change observed in band-bending during junction formation eliminates Fermi level pinning at the interface. The results thus eliminate an unfavorable energy level alignment and Fermi-level pinning at the

$CuInS_2$/Zn(O,S) interface as the source of interface recombination in the case of Cu-rich devices. Therefore, the results necessitate the need for an alternate mechanism that can explain interface V_{OC} deficit and result in device characteristics similar to interface-dominated devices.

The optoelectrical analysis of the Cu-rich $CuInS_2$ before and after the sulfur-based post-deposition treatments, particularly the TU-PDT, displayed an improvement in interface V_{OC} deficit and also the ability of the thiourea treatment to prevent the known $V_{OC,in}$ degradation [26] of the sample after buffer deposition. This improvement was associated to the passivation of defects near the interface, which was indicated by an increase in E_a of the charge carrier dominant recombination path. The transient capacitance measurements revealed the presence of slow metastable defects in the untreated and their partial passivation in the treated solar cells. The results suggest the presence of defects at or near the interface caused by KCN etching, as in the case of $CuInSe_2$ solar cells as the cause of interface V_{OC} deficit.

Building a model to understand the interface V_{OC} deficit based on the near interface defects requires better knowledge of the defect responsible. However, in admittance spectroscopy, a defect signature that can be linked to interface V_{OC} deficit is absent. The next chapter will probe $CuInSe_2$, a closely related alloy system that suffers from interface V_{OC} deficit, which is well documented to the “200 meV” defect signature in admittance spectroscopy.

Chapter 6

Experimental evidence and modeling of defective layer

In the preceding two chapters, the performance limiting factors for the $CuInS_2$ and $Cu(In,Ga)S_2$ solar cells were explored through electrical measurements. While Cu-poor $Cu(In,Ga)S_2$ displayed an impressive translation of $V_{OC,in}$ into $V_{OC,ex}$, the Cu-rich $CuInS_2$, and $Cu(In,Ga)S_2$ device were found to suffer from large interface V_{OC} deficit caused by dominating interface recombinations in the device, as revealed by the I-V measurements. Moreover, in chapter 5, the S-PDT and the second KCN etching step establish the near-surface nature of performance-limiting defects. These defects are generated as a consequence of the KCN etching of the Cu-rich $CuInS_2$ absorbers. However, these are not the first devices to display these features in their electrical characteristics. As described briefly in section 2.2, the Cu-rich $Cu(In,Ga)Se_2$ solar cells also suffer from similar performance-limiting interface recombinations.[74]

When comparing the Cu-rich $CuInSe_2$ system to the $CuInS_2$ system, the former has a certain advantage over the other. The $CuInS_2$ devices do not show any signs of the near-surface deep defect in their admittance spectroscopy, even though PL measurements clearly establish their presence (Fig. A5.11 and [28]). In contrast, the 200±20 meV near-interface defect signature observable in the admittance spectroscopy of $CuInSe_2$ devices has already been established as the cause of interface V_{OC} deficit in these devices. The defect originates from the necessary KCN etching step required to remove the secondary $Cu_{2-x}Se$ phase, resulting in a high concentration $>10^{16}$ cm^{-3} of deep defects (~200 meV) in Cu-rich $CuInSe_2$ absorbers.[46, 170] The defects are termed as near-interface defects because admittance spectroscopy performed at different DC applied voltages does not yield a voltage-dependent defect activation energy nor a defect that disappears with bias (see Fig. A6.3a and b), which would be typical for interface defects.[220, 221] Here, near-interface defects are defects spread in a thin region (few tens of nm) near the interface towards the absorber. In contrast, interface defects are the defects present just at the 2-D interface between absorber and buffer.

The “200 meV” defect originates from the necessary KCN etching and can be passivated with the help of Se-related treatments (for more details, see section 2.2).[46, 74] Thus, a lot of information regarding the origin and nature of the near-surface defects can be extracted by studying the 200±20 meV defect. Additionally, although KCN etching has been identified as the root cause of the 200±20 meV defect, it is not clear whether any etching would lead to the formation of the 200±20 meV defect or only the KCN etching. These open questions make a compelling argument for exploring the electrical properties of Cu-rich $CuInSe_2$, particularly studying and investigating the cause of the interface V_{OC} deficit in thin-film solar cells. Therefore, this chapter will focus on Cu-rich $CuInSe_2$ to build a comprehensive model to understand how the near interface defects cause of interface V_{OC} deficit in these devices.

The chapter is divided into three sections. Almost all the sections are taken verbatim or with minor modifications from our manuscript [174]. In the first section 6.1, the electrical performance of the Cu-rich and Cu-poor $CuInSe_2$ solar cells has been revisited, with emphasis on the $V_{OC,in}$ and $V_{OC,ex}$ of devices, which is used to extract the interface V_{OC} deficit. Parallels are drawn between the $CuInSe_2$ and $CuInS_2$ solar cells in terms of interface V_{OC} deficit and temperature-dependent I-V measurements. The presented I-V measurements are already reported in the thesis of Dr. Elanzeery,[74] and have been revisited in the context of this thesis. These results also form an essential background for understanding the present work better.

Based on our knowledge from section 5.3, where we observed an impact of PDT on the defects in the $CuInS_2$ devices. The second section 6.2 is dedicated solely to the PDT performed on Cu-rich $CuInSe_2$ to gain more insights into the origin and nature of the defect. The as-grown Cu-rich absorbers are etched with KCN and aqueous bromine solution, and the devices are probed with admittance spectroscopy. Further, for KCN etched device, with the help of deep-level transient spectroscopy (DLTS), the defect's character (acceptor or donor) is examined. In an attempt to vary the interface defect density, the KCN etched Cu-rich absorbers are treated with three different solution treatments, namely aqueous zinc ($Zn_{aq.}$), sulfur (S) and cadmium (Cd) solution, as well as by depositing a Zn(O,S) buffer. With the help of admittance spectroscopy, the impact of these treatments on defect signal is probed to understand the species responsible for the defect. The results can be partly explained with the divacancy complex model[124] as the origin of the 200 meV defect signal in admittance spectroscopy.

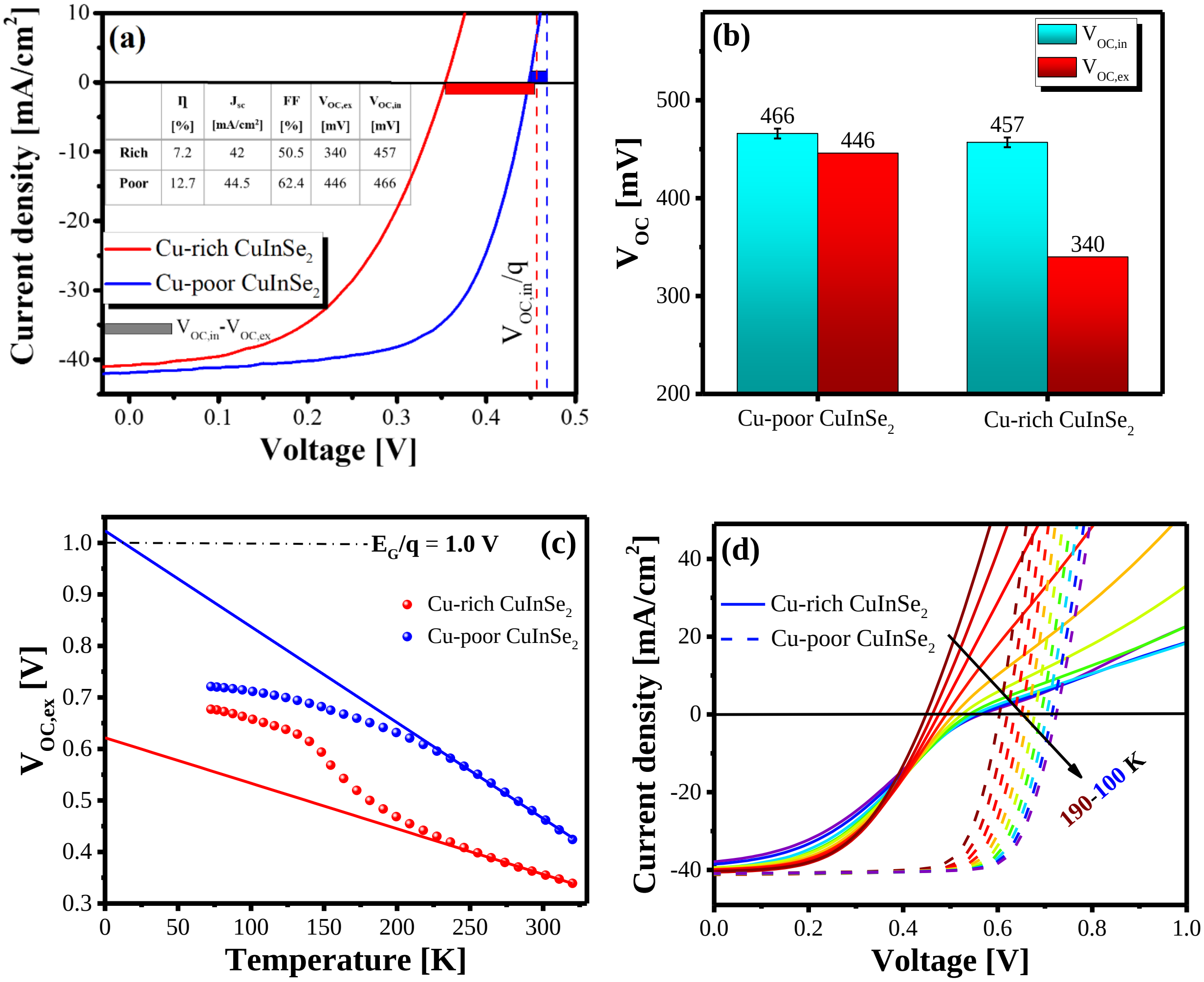
With the information gained in sections 6.1 and 6.2, finally, in section 6.3, the I-V, admittance, and DLTS data is used to construct a model for understanding the interface V_{OC} deficit. This is done by probing the effect of near-surface defects on $V_{OC,in}$ and $V_{OC,ex}$ of the $CuInSe_2$ and $CuInS_2$ device using drift-diffusion simulations. Using numerical modeling through SCAPS-1D, a model based on strong sub-surface defects is established, which demonstrates an interface V_{OC} deficit and $E_a < E_G$ in a device with favorable band alignment and no Fermi level pinning at the interface. The model is also compared with the device having pinned Fermi level through interface defects, which is the only possible explanation for $E_a < E_G$ in devices with a spike at the absorber/buffer interface.

Section 6.1 to section 6.3 is taken directly from our published work [174] with minor modifications. The part that has been taken verbatim has been highlighted with a different text format.

6.1 Cu-rich vs Cu-poor $CuInSe_2$

We start by comprehending how the $V_{OC,in}$ and $V_{OC,ex}$ of $CuInSe_2$ solar cells fare compared to $CuInS_2$ solar cells. In particular, we are interested in the interface V_{OC} deficit in these devices. For this, the performance of devices prepared with the Cu-rich and Cu-poor as grown absorbers is summarized here. The absorbers are prepared as explained in section 2.2.1 and then processed into solar cells, both similarly, *i.e.* with the same buffer (CdS), i-layer (i-ZnO) and window layer (Al:ZnO), deposited with identical process parameters using the process explained in chapter 3. The $V_{OC,in}$ measurements, were done on absorbers samples covered with CdS buffer layer on top exactly as described in section 3.2.1.

Unlike $CuInS_2$ absorbers, where the Cu-rich $CuInS_2$ absorbers exhibit superior $V_{OC,in}$ compared to the Cu-poor absorbers (see chapter 5),[28] both Cu-rich and Cu-poor $CuInSe_2$ absorbers possess similar $V_{OC,in}$ (see table inset Fig. 6.1a), signifying a similar $V_{OC,in}$. Fig. 6.1a shows the typical I-V characteristics of the Cu-rich and Cu-poor devices. The Cu-rich device exhibits a lower $V_{OC,ex}$ than the Cu-poor device, even though absorbers have almost the same $V_{OC,in}$ [see table inset Fig. 6.1a and Fig. 6.1b].



	η [%]	J_{sc} [mA/cm²]	FF [%]	$V_{OC,ex}$ [mV]	$V_{OC,in}$ [mV]
Rich	7.2	42	50.5	340	457
Poor	12.7	44.5	62.4	446	466

Figure 6.1: *Comparison of Cu-rich vs Cu-poor CuInSe₂ device (a) I-V curve characteristics, and (b) the comparison of $V_{OC,ex}$ (in red) and $V_{OC,in}$ (in cyan), which shows a high interface V_{OC} deficit for Cu-rich devices. The blue and the red bar shows the interface V_{OC} deficit for Cu-rich and Cu-poor devices. (c) $V_{OC,ex}$ as a function of temperature, extrapolation to 0 K gives activation energy of saturation current density (d) I-V as a function of temperature, a rollover is observed at lower temperatures in Cu-rich devices.*

The lower $V_{OC,ex}$ originates from the high interface V_{OC} deficit (~130 mV) observed in Cu-rich CuInSe₂ devices, similar to CuInS₂ devices (see section 5.1). The high interface V_{OC} deficit has also been observed in the Cu-rich Cu(In,Ga)Se₂ devices,[83] much like the Cu(In,Ga)S₂ devices (see section 5.1). This is significantly higher than the Cu-poor device (~20 mV) discussed here or in fully optimized devices (~10 mV).[172] Similar to the Cu-rich CuInS₂ devices (see section 5.1), this interface V_{OC} deficit is also associated to interface recombination being the dominant recombination path in the device, as revealed from the $V_{OC,ex}$ measurements at different temperatures [Fig 6.1c] The activation energy (E_a) of the saturation current density is obtained from the extrapolation of $V_{OC,ex}$ to 0 K (as explained in section 2.1.2).

Not just for the devices presented here, historically too, Cu-rich $CuInSe_2$ devices have always displayed an E_a lower than the E_G[32, 86, 222], which has been recently associated with the presence of deep interface defects.[46, 74] In contrast, the Cu-poor devices display an E_a equal to the E_G, and hence, interface recombination does not limit $V_{OC,ex}$. Furthermore, a rollover in the first quadrant is observed at lower temperatures in the Cu-rich device, which is not present in the Cu-poor device [Fig. 6.1d]. This roll-over in the first quadrant indicates a barrier for the forward current, and a number of causes were discussed in section 4.2.4.[223]

In summary: the Cu-rich $CuInSe_2$ solar cells show the typical signatures of interface recombination: an extrapolation of $q \cdot V_{OC,ex}$ to 0K that is smaller than the band gap energy, and a strong interface V_{OC} deficit similar to $CuInS_2$ solar cells. However, the bandgap of the Cu-rich and of the Cu-poor material is essentially the same (as observed from the EQE curves of the devices Fig. 4.1c and Fig. A6.1b). The two textbook causes for interface recombinations as discussed in section 2.1.2 are negative CBO at the absorber/buffer interface and Fermi-level pinning. However, it has been shown that CdS forms a favorable band alignment with $CuInSe_2$[224] and Zn(O,S) with $CuInS_2$ (in section 5.2), and the photoelectron studies show no sign of Fermi-level pinning in the Cu-rich $CuInSe_2$ or $CuInS_2$ device (see, e.g. [225] and section 5.2). Moreover, if Fermi level pinning was the dominant mechanism, a diode factor near 1 would be expected.[55] In contrast, in general, diode factors ~ 2 for Cu-rich $Cu(In,Ga)Se_2$[226] and $CuInS_2$ is observed (Fig. A6.2). Thus, an alternative model is needed to explain the observed behavior, which will be discussed in section 6.3. However, to build a reliable model, first, the characteristics of the deep defect that has been correlated to be the cause of all these issues in Cu-rich $CuInSe_2$[46] has to be probed. The following section will focus on gaining more insights into the defect.

6.2 $CuInSe_2$ "200 meV" defect origin, nature, and characteristics

6.2.1 Impact of etching solution on deep defect in $CuInSe_2$

It is unknown whether the "200 meV" defect originates specifically from the KCN etching or the etching process of the secondary phase independent of the etchant used. To investigate this, Cu-rich $CuInSe_2$ solar cells are prepared using two different etching solutions: 10 (wt. %) aqueous KCN solution (for reference) and 0.16 % mM aqueous Br solution. The impact of etching on the defect structure is investigated by measuring admittance spectroscopy.

Fig. 6.2a shows exemplary admittance spectroscopy measurements for KCN etched Cu-rich $CuInSe_2$ solar cell. The spectra exhibit a capacitance step in the temperature range 190-100 K. The corresponding frequency derivatives of the admittance spectra demonstrate broad asymmetric peaks (Fig. 6.2b). These broad peaks are a peculiar feature always present in the admittance spectra corresponding to the ~200 meV defect.[46] The admittance spectra of aqueous Br etched Cu-rich $CuInSe_2$ solar cell exhibits a similar capacitance step (dotted lines in Fig. 6.2a and 6.2b). More importantly, the inflection frequencies of admittance spectra of this device plotted together with that of the KCN etched device in an Arrhenius plot lie very close to each other, with activation energies around 200 meV. This indicates the presence of a similar capacitance response in both devices.

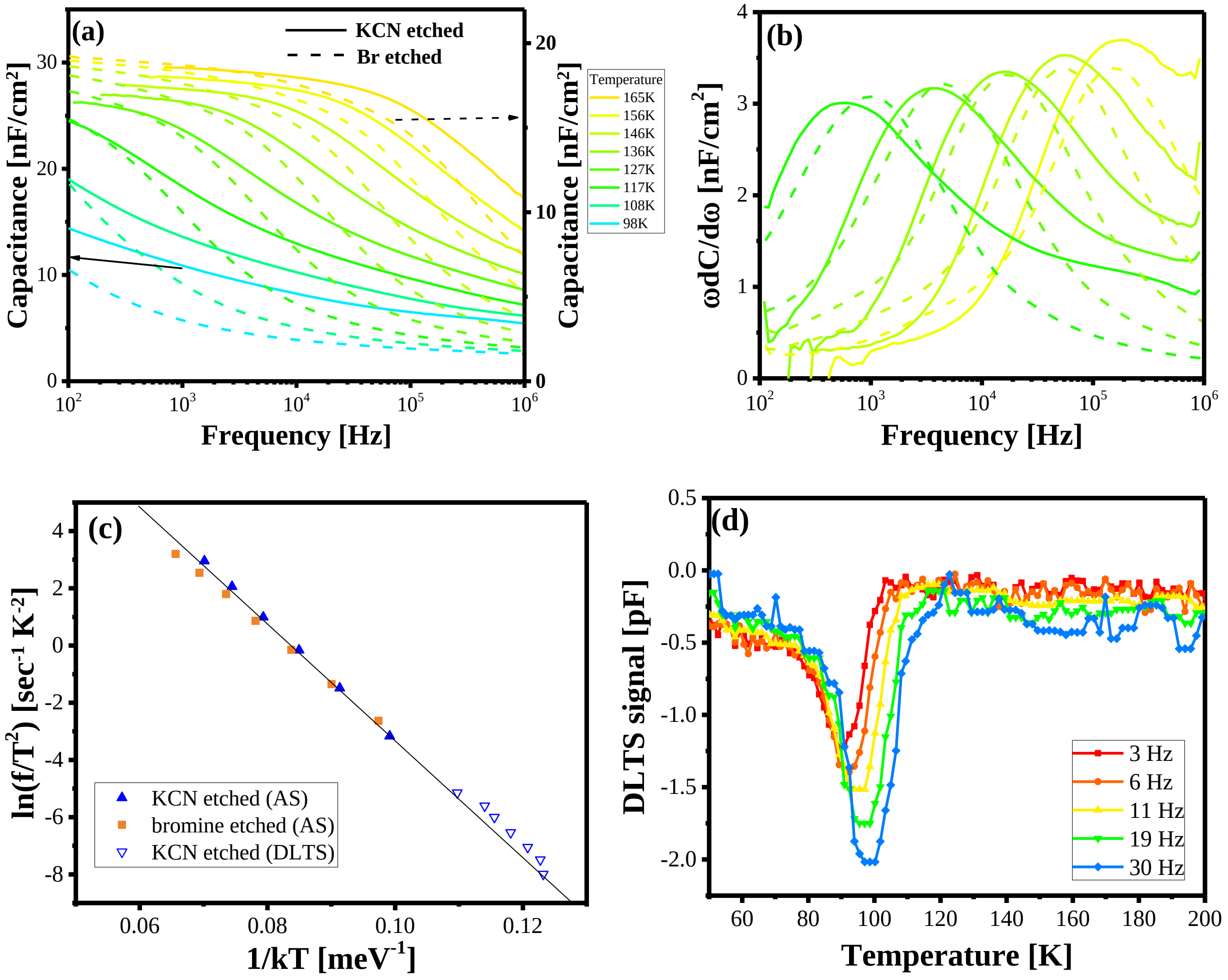


Figure 6.2: *(a) Admittance spectra of Cu-rich $CuInSe_2$ solar cell prepared from absorbers etched with KCN and bromine solution. Please note different y-axis for the KCN etched (right y-axis) and Br etched (left y-axis) devices. (b) ωdC/dω plot of corresponding admittance spectra, the peaks are broad and asymmetric. (c) The Arrhenius plot of measured admittance (closed symbols) and DLTS (open symbols) measurements of CuInSe2 Schottky junction devices were prepared with KCN etched and bromine etched absorbers. (d) DLTS signals of the KCN etched $CuInSe_2$ Schottky junction device.*

In supplement to these results, a device prepared from a Br etched absorber also has the same E_a of the saturation current density as the KCN etched device, significantly lower than E_G (Fig. 6.3a), identifying the presence of prevailing interface recombination. Thus, both results, the presence of a similar capacitance step with almost equal activation energies and the presence of interface recombination, confirm the existence of the deep defect independent of the etchant used to remove the $Cu_{2-x}Se$ phase. This suggests that the ~200 meV defect is an intrinsic defect originating from the removal of the secondary phase from Cu-rich $CuInSe_2$ films, as suggested in the literature.[214]

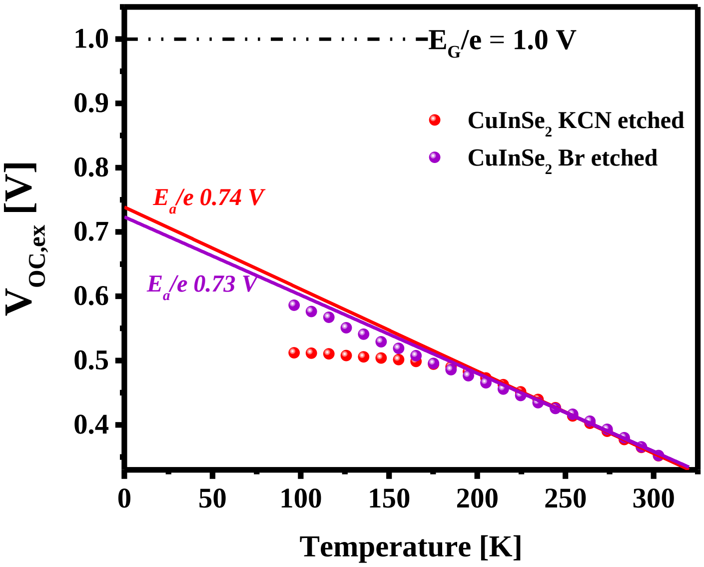


Figure 6.3: *$V_{OC,ex}$ measurements of 10 % KCN and 0.01M Br solution etched $CuInSe_2$ solar cells.*

6.2.2 Probing the nature of the deep defect using DLTS

Although admittance spectroscopy provides the defect activation energy, it does not yield the defect nature. Therefore, to investigate whether the defect is acceptor or donor in nature, DLTS (Fig. 6.2c) is measured on KCN etched $CuInSe_2$ Schottky devices (*i.e.* Mo/$CuInSe_2$/Al). Schottky devices were used to probe a passivated absorber as the buffer deposition can lead to (partial) passivation of defects.[46] For DLTS measurement, $CuInSe_2$ Schottky devices were kept at -1V bias followed by a +1V voltage pulse and the capacitance transient was measured.

Fig. 6.2d shows the DLTS results for a chosen rate window alongside with the corresponding Arrhenius plot in Fig. 6.2c. The peak in the DLTS spectrum is negative, which is a fingerprint of emission of majority carriers from a trap. Further, the activation energy of the corresponding signal is similar to the one observed in admittance spectroscopy. Moreover, the DLTS data points in the Arrhenius plot continue the admittance data, suggesting that it is the same signal as the one observed in admittance spectroscopy. These results thus confirm that the ~200 meV defect observed in admittance spectroscopy of Cu-rich $CuInSe_2$ devices is an acceptor defect.

6.2.3 Post deposition treatments on $CuInSe_2$ devices

In section 5.3 we have observed that S-PDT can lead to passivation of defects causing interface V_{OC} defcit in $CuInS_2$ solar cells. Earlier work on $CuInSe_2$ also establishes the presence of deep defects in $CuInSe_2$ solar cells,[46] that can be passivated with mild surface chalcogen treatments and buffer layers with a high sulfur concentration in the deposition process.[46, 85, 86] It is fascinating that in addition to high temperature (>300°C) chalcogen treatments, discussed in section 2.2, even chemical bath deposited buffer layers, *i.e.* CdS and Zn(O,S) at low temperatures (<85°C) were found to passivate deep defects.[46] This suggests that the defect is present at or near the surface within few tens of nanometers. It is not likely that the buffer layer deposition, which are done at low temperatures, passivates a defect in the bulk. To explore this possibility and rule out the buffer layer as a viable cause for the disappearance of defect signature in admittance spectroscopy, three post-deposition treatments (PDT) are performed. For the PDTs, KCN etched Cu-rich $CuInSe_2$ absorbers were immersed into three different solutions: ammonia solution of $ZnSO_4$ (Zn-PDT), ammonia solution of $CdSO_4$ (Cd-PDT), ammonia solution of CH_4N_2S (S-PDT), each at 80 ˚C for 10 minutes. Since buffer chemical bath contains multiple ionic species, to exclude the impact of these the absorbers were made into Schottky device and then admittance spectroscopy was performed.

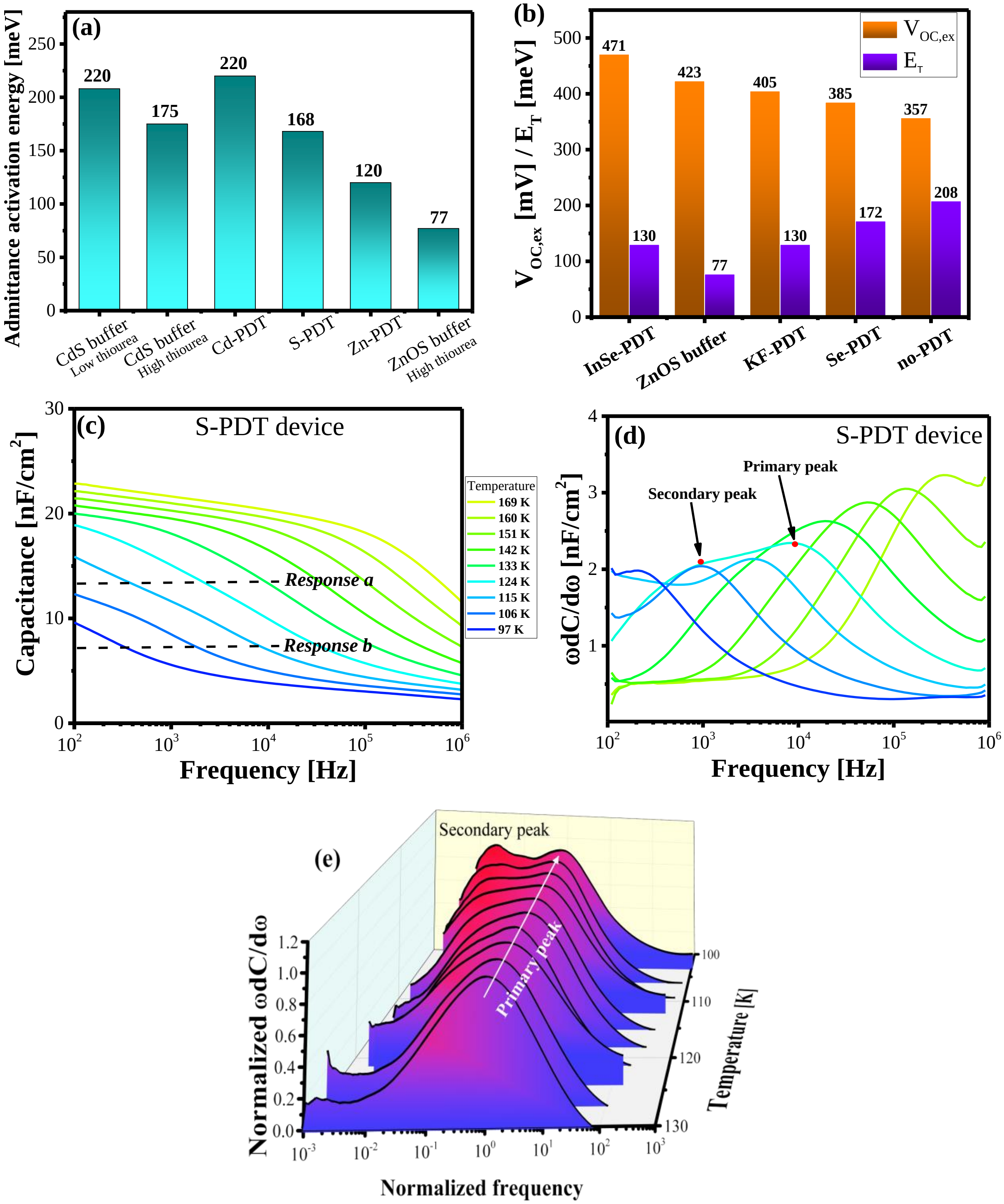


Figure 6.4: *(a) Summary of activation energies obtained from Arrhenius plot of the main capacitance step for different PDTs and buffer layers. The bar chart shows the activation energy of the main capacitance step obtained for devices prepared after performing various PDT on the 10 % KCN etched absorbers. (b) Summary of* $V_{OC,ex}$ *values and defect energy (*E_T*) obtained from admittance spectroscopy of post-KCN treated devices and the untreated device. (c) Admittance spectra of S-PDT* $CuInSe_2$ *absorber in a Schottky device (d) corresponding* $\omega dC/d\omega$ *plot, which at*

124 K shows double-peak structure the high-frequency peak is arbitrarily named primary peak and the low-frequency peak as the secondary peak. (e) The plot of normalized frequency vs normalized $\omega dC/d\omega$ w.r.t. frequency. The curve shows the appearance of a secondary peak, particularly at low temperatures.

Fig. 6.4a gives the summary of the defect energies obtained after the three PDTs (Schottky-device) along with the values obtained after CdS and Zn(O,S) buffer deposition (on solar cells). For the PDT samples, a reduction in the defect activation energy is used as an indirect indicator for the passivation of the deep defect. This is because the samples that displayed a reduction in defect energy after different PDTs also demonstrate an improvement in $V_{OC,ex}$ (see Fig. 6.4b) and consequently in the interface V_{OC} deficit, which signifies passivation of deep defects. Among the three PDTs, Zn-PDT leads to complete passivation of the defect, confirmed by the significant reduction in the activation energy of the capacitance step (see Fig. 6.4a). The respective energies of 77 meV and 120 meV obtained after the Zn(O,S) buffer and Zn-PDT can be attributed to the A2 (60meV) and A3 (135 meV) acceptor in $CuInSe_2$, respectively.[88, 227] However, the S-PDT only results in partial passivation, as it still exhibits the signature of a deep defect in the admittance spectra (Fig. 6.4c) with activation energy ~170 meV.

It has been speculated that the broadness of the 200 meV peak originates from the contribution of two defects 200 ± 20 meV defect and 130 ± 10 meV defect.[46] And passivation of the 200 meV defect in the device leads to a decrease in activation energy of capacitance step in admittance spectroscopy. In the case of complete passivation, the capacitance step with activation energy 130 meV remains.[46] However, in the case of partial passivation, the capacitance step with activation energy between 130 meV and 200 meV is obtained. In particular, for the S-PDT device, the frequency derivative of admittance spectra (Fig. 6.4d) displays broad peaks, a feature similar to the un-passivated samples. Also, the main capacitance step in admittance spectra starts to bifurcate into two steps (response 'a' and 'b' in Fig. 6.4b) at low temperatures (<130 K), which might be due to the presence of two different defect signatures. For better visualization, the high-frequency peak of the curve at 124 K is arbitrarily assigned as the primary peak and the other as the secondary peak in Fig. 6.4d.

Fig. 6.4e shows the normalized amplitude of the primary peak plotted vs. normalized inflection point (*i.e.* the frequency at peak maxima) of the corresponding frequency derivative with the temperature as a parameter. Here, the admittance spectrum was measured in smaller temperature steps (~3 K) to resolve the two peaks better. A careful observation of the plot reveals the evolution of the second peak highlighted in red at low temperatures. This establishes the presence of two different defects, which constitute the main step in the admittance spectra of Cu-rich $CuInSe_2$ devices.

For the untreated absorbers, the presence of similar broad peaks in the $\omega dC/d\omega$ spectra (Fig 6.2b) indicates that the capacitance step might be originating from contributions of two defects, one more prominent than the other. Lastly, the admittance spectra of the Cd-PDT device do not show any reduction of the activation energy of the capacitance step (Fig. 6.4a), confirming that neither Cd^{2+}, $(SO_4)^{2-}$ or OH^- results in passivation as they are contained in Cd-PDT solution. To summarize, Zn treatment leads to complete passivation of the defects, the S treatment leads to partial passivation, and Cd treatment alone leads to no passivation of the defect.

To get an estimate of defect density, capacitance steps consisting of overlapping defect contributions (see, for instance, Fig. 6.4d) were fitted by Dr. Thomas Weiss as described in [228]. In particular, the defect response from a discrete defect level is extended to Gaussian defect distributions. Here, two Gaussian distributions are used and are fitted simultaneously to the complete temperature and frequency range. A fit describing the two overlapping capacitance steps of the spectra shown in Fig. 6.4d is shown Fig. A6.3c. For the untreated sample, a defect density ~2×10^{16} cm^{-3} for both peaks together, and for S-PDT sample a defect density of ~4×10^{15} cm^{-3} was obtained.

Since low-temperature PDT does not lead to changes in the bulk, it can be concluded that the 200 meV defect is actually a defect at or near the surface. The defect is most probably related to the Cu-Se divacancy defect complex[124] as it is passivated by Zn PDT and S/Se PDT (see Fig. 6.4a). The passivation occurs because Zn cation can easily passivate the Cu vacancy due to their similar ionic radii, whereas the S/Se anion can directly passivate the Se vacancy. Besides this, admittance spectroscopy results suggest that the defect capacitance signal consists of two constituents, one of which (probably the Cu-Se divacancy defect signal) can be passivated with proper surface treatment.

To summarize, the experimental findings: the 200 meV defect is an acceptor defect, has a defect density of around ~10^{16-17} cm^{-3},[46] and is present at or near the surface, *i.e.* a near-surface defect. However, it is unclear how this defect can lead to large interface V_{OC} loss and a saturation current activation energy lower than the bandgap. In the next section, a numerical model is realized by introducing defects in $CuInSe_2$ based on above-discussed defect properties to describe the experimental observations.

6.3 Modelling the interface V_{OC} deficit in $CuInS(e)_2$ solar cells

So far, we have seen that all Cu-rich chalcopyrite devices are characterized by a saturation current strongly dominated by interface recombination. This is indicated by E_a obtained from extrapolation of $V_{OC,ex}$ *to 0K* always being lower than the E_G as shown throughout this thesis in section 4.1, section 5.1, and section 6.1 and also historically.[32, 45] Two possible explanations for the activation energy of the saturation current E_a lower than the bandgap are established in the literature: a cliff at the absorber buffer interface, *i.e.* negative CBO at $CuInSe_2$/CdS interface and $Cu(In,Ga)S_2$/Zn(O,S) interface, or Fermi level pinning at this interface (as mentioned in section 2.1.2).[45, 229]

A straightforward origin of interface recombination could be a negative CBO, *i.e.* a cliff at the interface. However, in section 5.2 we found a +0.1 eV CBO between the conduction band minimum of $CuInS_2$ and Zn(O,S) in the photoelectron measurements. Similarly, the photoelectron study by Morkel *et. al.* reports a conduction band minimum of CdS aligned with Cu-poor $CuInSe_2$.[230] As there is no indication that the band edges of Cu-rich $CuInSe_2$ are different from those of Cu-poor material, these observations eliminate negative CBO as the cause of interface recombination in these devices.

The other possible scenario could be the presence of a high concentration of defects (N_{IF}) at the $CuInSe_2$/CdS ($CuInS_2$/Zn(O,S)) interface, which pins the electron Fermi level at the interface. To have a working solar cell like in Fig. 5.1a and Fig. 6.1a, the pinning position must be above the middle of E_G to obtain a decent $V_{OC,ex}$. Thereby the electron concentration at the interface remains significantly higher than the hole concentration. Thus, the interface recombination depends on the interface hole concentration (p_{IF}) and the hole surface recombination velocity (S_p), *i.e.* $R \approx p_{IF}*S_p$.[45] The reverse saturation current density (J_0) is given by:[45]

$$J_0 = qN_{v,a}S_p \exp\left\{-\frac{E_b^h}{kT}\right\} \qquad (6.1)$$

Where $N_{v,a}$ is the effective valence band density of states in the absorber and q is the elementary charge, E_b^h is the equilibrium hole barrier at the interface and is equal to the energy difference between the position of electron Fermi level (F_e) and the valence band edge (E_v) under equilibrium, *i.e.* $E_b^h = F_e - E_v$. Equation 6.1 is true if the recombination current is dominated by interface recombination, *i.e.* in the case of a significant S_p. This is more likely for a negatively charged interface, *i.e.* with a high density of acceptor states. However, it is not necessarily the case that the pinning defect and the recombination defect are the same, although we assume this in our simulation. From equation 6.1, it is evident that in the case of Fermi level pinning, the E_a of the saturation current should be E_b^h, which is lower than E_G. Consequently, the external open-circuit voltage is given by equation 2.21 with $J_{00} = qN_{v,a}S_p$ following [45, 229]

$$V_{OC,ex} = \frac{E_b^h}{q} - \frac{kT}{q} \ln\left(\frac{qN_{v,a}S_p}{J_{ph}}\right) \tag{6.2}$$

Thus, $V_{OC,ex}$ is dominated by E_b^h. One should note that for a good device which is not dominated by interface recombination, the $V_{OC,ex}$ at 0K is equal to the bandgap of the absorber (see section 2.1.2). It should be cautioned that extrapolation of $V_{OC,ex}$ to the bandgap, does not exclude interface recombination.[231] Thus, in the case of Cu-rich Cu(In,Ga)Se_2 or Cu(In,Ga)Se_2 device with spike-type band alignment, Fermi level pinning could explain an E_a value smaller than E_G, namely E_b^h obtained from $V_{OC,ex}$ *vs* temperature plot (assuming S_p and J_{ph} are not or only weakly temperature dependent).

6.3.1 Numerical simulations for interface V_{OC} deficit in $CuInSe_2$

The results obtained in section 6.2 indicate the near-surface and acceptor nature of the defect, *i.e.* an acceptor defect present close to or at the absorber/buffer interface. Therefore, the defect could represent either a defective layer within the absorber, just below the surface, or a defective interface between the absorber and the buffer. In this section, using numerical modeling, the impact of both: a defective layer and a defective interface on the $V_{OC,in}$ and $V_{OC,ex}$ of the device will be investigated. We will first assess the models to reproduce the experimentally observed characteristics of Cu-rich $CuInSe_2$ devices as observed in Fig. 6.1 and 6.2 and discuss: (i) >100 meV interface V_{OC} deficit, (ii) a 200 meV defect signature in the admittance spectroscopy, (iii) an E_a of the saturation current density lower than the E_G of $CuInSe_2$ and (iv) a ‘S shape’ in only the first quadrant at lower temperatures in the I-V curves. The most successful model will then be applied to $CuInS_2$ to check if the model can also explain this system's experimental observation.

A device model is designed in SCAPS-1D (see section 3.4) emulating the Cu-rich $CuInSe_2$ devices (back contact/$CuInSe_2$/CdS/ZnO/Al:ZnO/front contact). Table A6.1 records the electrical and optical parameters used in the simulations, which were set constant, taking values from previous measurements.[232-234] Further, no conduction band offset at the absorber/buffer interface and flat band conditions at the absorber back contact were assumed to keep the model as simple as possible to avoid convergence problems in SCAPS.

Three models were developed. All the models involve deep acceptor defects since the characteristic "200 meV" defect in the Cu-rich $CuInSe_2$ is a deep acceptor state. The first model named as 'DL_CB' comprises a defective layer (often called p^+ layer in the literature [211, 235]), *i.e.* a thin layer with a high concentration of 220 meV deep acceptor defects away from CB. The second model named 'DL_VB' is just a variation of the first model with the 220 meV deep acceptor states away from VB. There are no deep defects at the interface in both the models (Fig. 6.6a).[170] We believe both models are possible; DL_CB model as defect is observable in reverse bias admittance measurements, which a majority carrier trap would not be if it is close to the valence band.[236] DL_VB model because CV measurements before and after defect passivation result in a reduction in apparent doping.[46] The defects and their capture cross-section in bulk and in the defective layer in a manner such that the model results in a $V_{OC,in}$ and $V_{OC,ex}$ similar to the experimental value.

The third model, named 'IFD' comprises a defective interface, with a significant amount of deep interface acceptor defects above mid-gap at the A/B interface and large electron capture cross-section, to ensure Fermi level pinning (Fig. 6.6b). The defect level is placed 650 meV above the valence band in this model. The defect energy value was chosen to allow for simulating activation energy for recombination current as close as possible to the experimental values. This was done because activation energy is equal to the Fermi-level is pinning position in this case (see equation 6.2). The distance of F_e and F_h from the conduction and valence band gives a measure of density of thermal or photo-generated free carriers in the respective bands. The high defect density (N_d) along with a large electron capture cross-section (reported in table A6.1) in both models results in strong reduction of electron quasi-Fermi level (F_e) and thus, a reduction of the $V_{OC,in}$ near the surface due to Shockley-Read-Hall (SRH) recombination (see Fig. 6.6b). Consequently, the $V_{OC,ex}$ of the device is reduced.

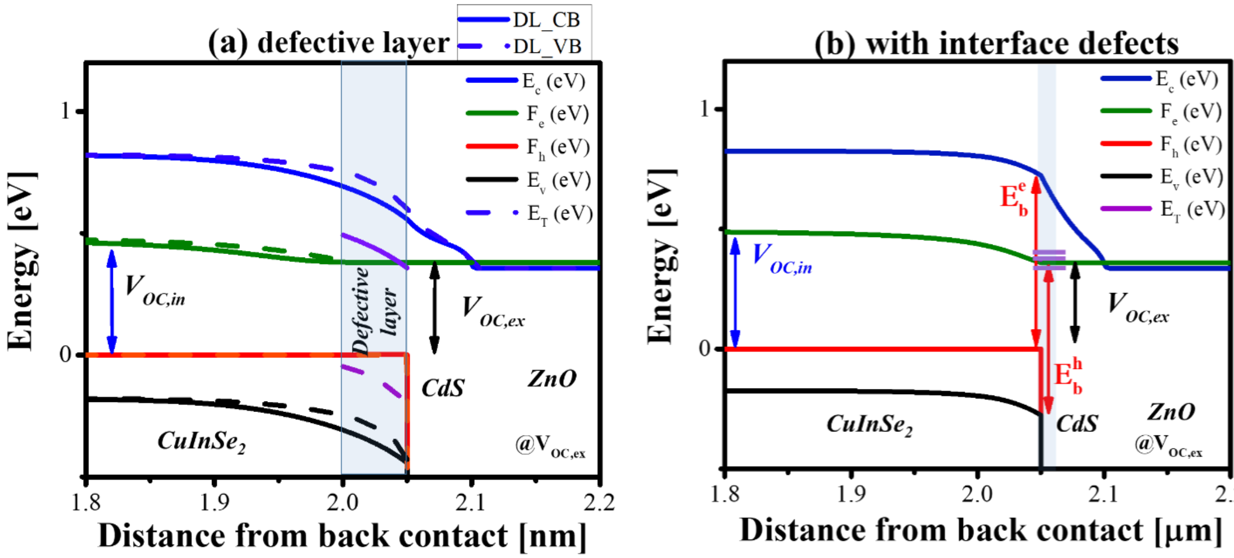


Figure 6.6: *Simulated band diagram of the device at open-circuit ($V_{OC,ex}$) voltage with (a) in solid lines DL_CB and in dashed lines DL_VB and (b) interface defects. The maximum quasi-Fermi level splitting in the device is labelled as $V_{OC,in}$. In contrast, the $V_{OC,ex}$ values are represented as the difference between the hole quasi-Fermi level at the back contact and electron Fermi level at front contact. The purple line shows the defect levels with high concentration in the device structure and E_b^h is the hole barrier and E_b^e is the electron barrier at the interface. The equilibrium band diagram is shown in Fig. A6.4.*

Moreover, in both models the $V_{OC,in}$ is reduced only in a very small region near the A/B interface: ~100 nm for the ~50 nm thick defective layer and ~50 nm for the defective interface, but is otherwise uniform throughout the absorber. This quasi-Fermi level gradient near the surface is observed independent of the carrier mobility. Even in high mobility limit (electron mobility values ~100 cm^2/V-s), the $V_{OC,in}$ is reduced near the surface in the CuInSe$_2$ device. A $V_{OC,in}$ measurement by photoluminescence (PL) reflects the (nearly uniform) maximum $V_{OC,in}$ in the bulk of the absorber, as the PL intensity increases exponentially with the $V_{OC,in}$.

The $V_{OC,ex}$ is the difference between the majority quasi-Fermi levels on either side. Since there is only a negligible gradient in the hole quasi-Fermi level, the $V_{OC,ex}$ is given by the $V_{OC,in}$ at the absorber buffer interface. Hence, it is established that all models result in deficit between the measured $V_{OC,in}$ and the $V_{OC,ex}$, as depicted in Fig. 6.6.

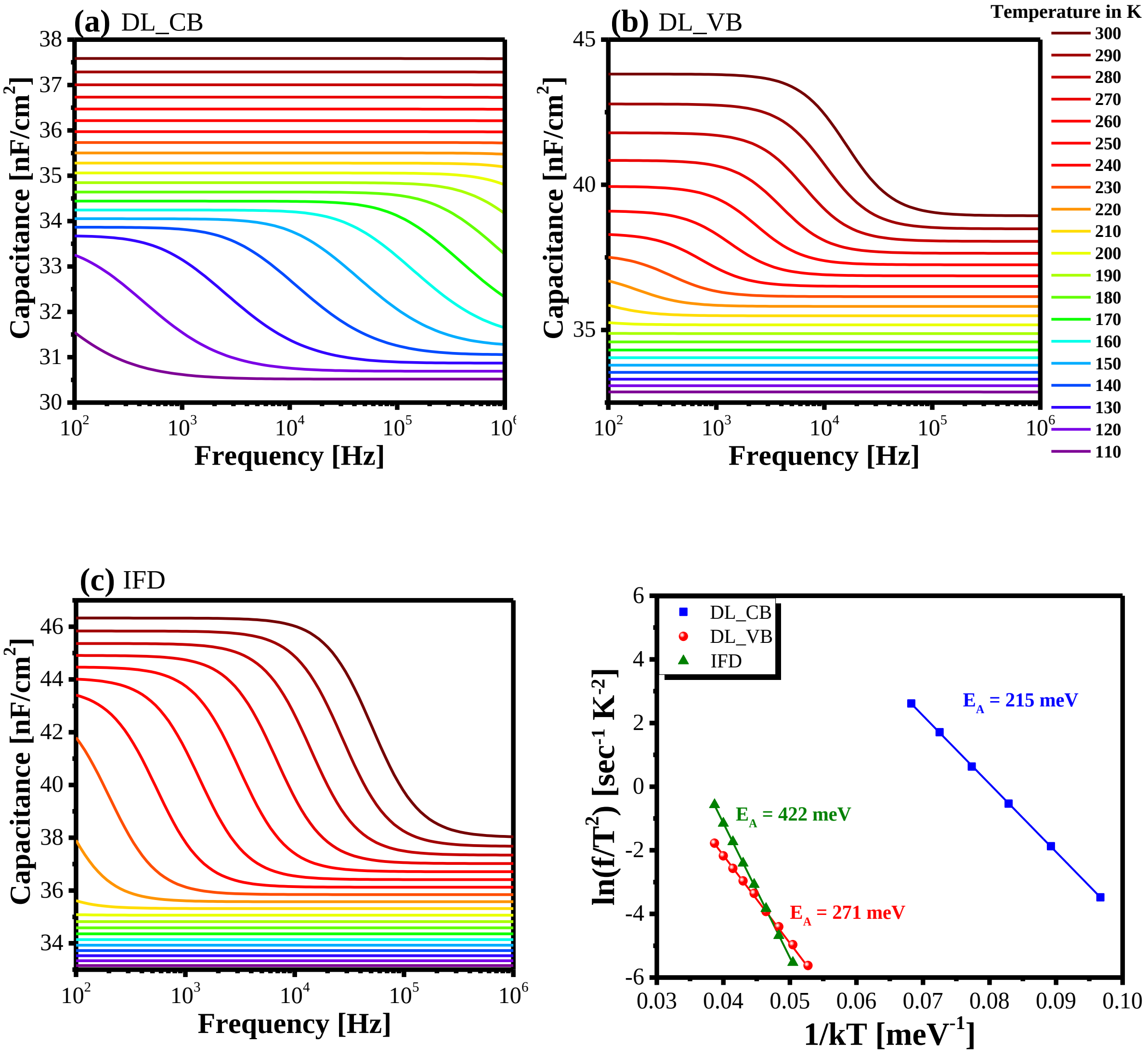


Figure 6.7: *Simulated admittance spectra of $CuInSe_2$ solar cell (a) DL_CB model (b) DL_VB model and (c) IFD model (d) Arrhenius plot of corresponding admittance spectra.*

The validation of either model as the appropriate description for Cu-rich $CuInSe_2$ devices also requires the fulfillment of criteria (ii), (iii) and (iv). Therefore, to check which of the models fulfill the criterion (ii), admittance spectra was simulated for the three devices. Fig. 6.7 shows the simulated admittance spectra and the corresponding Arrhenius plots of the devices. Out of the three admittance spectra, only the DL_CB model reproduces a capacitance step in a temperature range (110-160 K) similar to Fig. 6.2a, along with the proper defect activation energy (see Fig. 6.7d). The other two devices have no capacitance step in that temperature range. Also the activation energy corresponding to the capacitance step in the two cases are not close to 220 meV, but rather 271 meV and 422 meV (360 meV if the defect is 780 meV away from $CuInSe_2$ VBM). Thus, it can be concluded that the defective layer model with acceptor defects close to CBM closely resembles the Cu-rich $CuInSe_2$ device.

Let us now focus on criterion (iii). Even though the DL_VB model IFD model could not reproduce the admittance signal, the models will be considered further to have a comparison between them.

Fig. 6.8a shows the simulated $V_{OC,ex}$ values at different temperatures obtained from the two models with defects at or near the interface and for a reference model without any near interface defects. The simulations go down to 250 K, at lower temperatures, the numerical calculations under illumination would no longer converge. Remarkably, the IFD model with electron Fermi level pinning and also DL_CB and DL_VB models leads to an E_a of the saturation current less than the absorber E_G. It should be noted that the main recombination in the device with a defective layer occurs in that defective layer and not at the interface [Fig. A6.4a]. The E_a values obtained with this model are slightly higher than the experimental values. Even a considerable increase in defect concentration does not result in an E_a value below 0.78 eV in the DL_CB model and 0.81 eV in the DL_VB model [Fig. A6.5].

Thus, all the models can introduce a recombination pathway with an E_a lower than the E_G. Another critical observation comes from the hole barrier simulation at different temperatures (Fig. 6.8b and Fig. A6.6a). Neither model results in a temperature-independent hole barrier (E_b^h). However, E_b^h exhibits only a weak temperature dependence in the device with interface defect, and the extrapolation of E_b^h to 0 K equals the E_a obtained from $V_{OC,ex}$ measurements. This indicates that the simple model of Fermi level pinning in eq. 1 is only an approximation, and E_a should be identified as E_b^h at 0 K, as E_b^h itself is weakly temperature dependent. It is noteworthy that the N_{IF} used here was 10^{12} cm^{-2}, and even N_{IF} of 10^{14} cm^{-2} results in a weakly temperature-dependent E_b^h. Even in the latter case E_a is not equal to E_b^h at 300 K. It should be noted that the Fermi level is pinned in the model by a high concentration of acceptor defects. It is possible that a perfect pinning is obtained by a combination of acceptor and donor defects. Contrarily, in the device with the defective layer E_b^h and E_C-F_h or E_b^e are strongly temperature dependent, *i.e.* they show no Fermi-level pinning (Fig. 6.8b and Fig. A6.6a).

Fig. 6.8c shows simulated E_a and E_b^h at 0 K (obtained by extrapolating simulated hole barrier values to 0 K) for IFD as a function of interface defect density ($N_{d,IF}$). It is clear that in a certain range by varying the defect density one can have E_a anywhere between the E_G and the defect position in the interface E_G. Further, there is a one-to-one correlation between E_a and E_b^h at 0 K for IFD model.

Thus, it appears that in the case of a defective layer, the E_a of the recombination current is not determined by the hole barrier. This can be understood by considering that the recombination occurs mainly within the defective layer, *i.e.* away from the absorber-buffer interface, where the electron density decreases and electrons become the minorities. In summary, a strongly defective layer can also lead to activation energies lower than E_G, without Fermi level pinning and a cliff in the conduction band alignment.

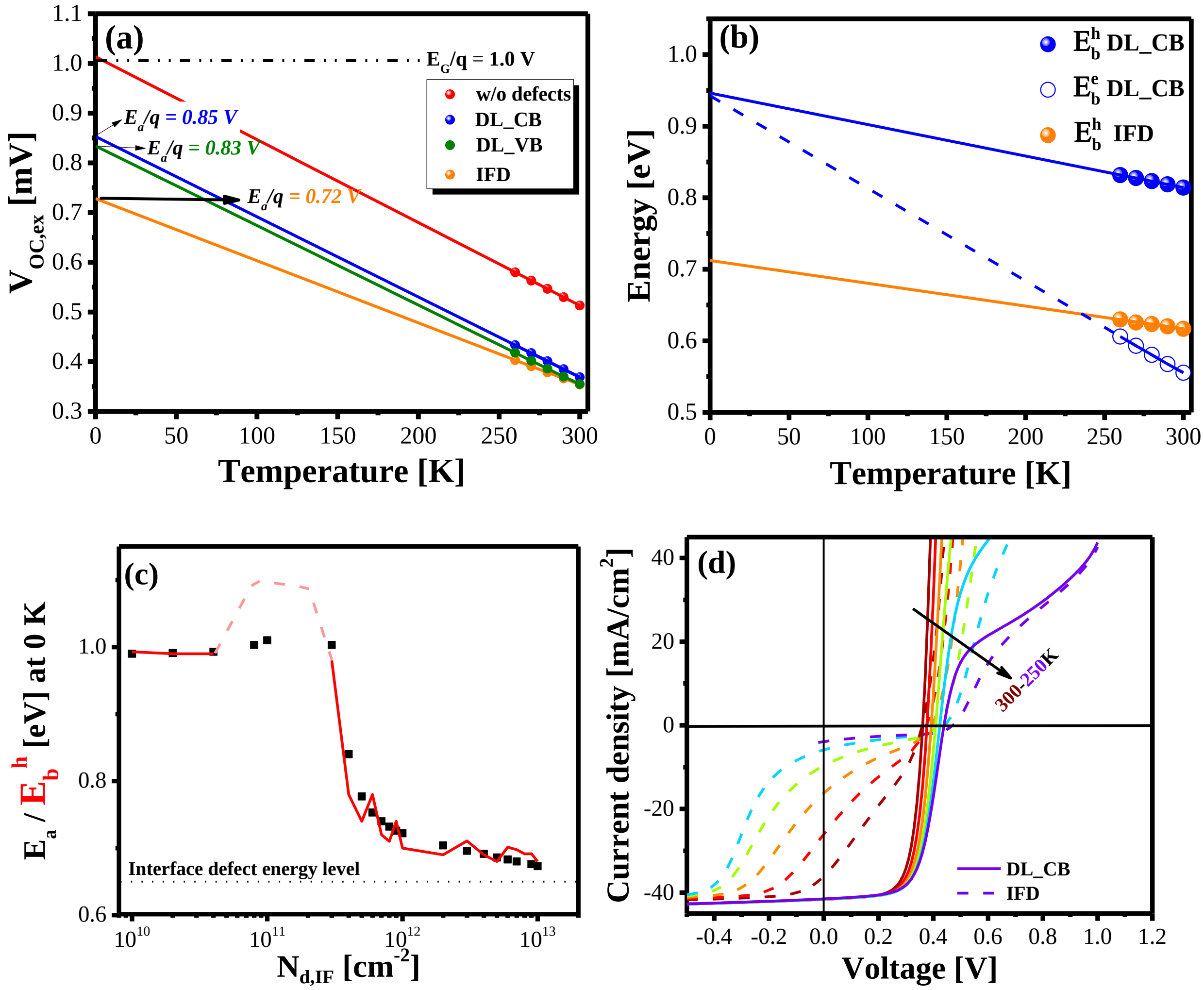


Figure 6.8: *(a) Simulated open-circuit voltage ($V_{OC,ex}$) values of the device with defective layer (DL_CB and DL_VB) and of the device with interface defects (IFD). (b) The electron and hole barrier as the function of temperature and its extrapolation to 0 K. (c) Activation energy (E_a) and the E_b^h at 0 K for the device with interface defects as a function of interface defect density. The E_a is obtained from V_{OC} vs. temperature curve and E_b^h is obtained from extrapolation of hole barrier to 0 K. The graph clearly shows a direct correlation of the activation energy with hole barrier height. Both quantities approach the energy of the defect at high defect concentrations. The two points with E_b larger than E_G are numerical artifacts. (d) Simulated I-V curve at different temperatures of devices with defective layer and with a defective interface. The former results in 'S shape' in the first quadrant (solid lines), whereas later results in 'S shape' in the third and fourth quadrant (dashed lines).*

Finally, the model was tested on criterion (iv), *i.e.* the 'S shape' in the first quadrant exhibited by Cu-rich $CuInSe_2$ devices at lower temperatures. It has already been established in section 5.2.4 that the ‘S shape’ in the first quadrant of the I-V curve originates from a cliff at buffer/i-layer (CdS/ZnO) interface.[45] Therefore, in contrast to the above models where only flat band conditions were assumed at the different interfaces, for the simulations in Fig. 6.8d, a small spike of 0.1 eV was introduced at the $CuInSe_2$/CdS interface (which gives a more realistic scenario as flat band conditions might not always be true in a device structure) and a 0.4 eV cliff at the CdS/ZnO interface. The particularly high cliff offset value was used to simulate the rollover in the first quadrant at higher temperatures, as SCAPS fails to converge at lower temperatures.

Fig. 6.8d shows the I-V curves at low temperatures simulated for a device with a DL_CB and a device with a defective interface, the I-V curves for the device with DL_VB can be found in Fig. A6.6b. It must be noted for all devices at a sufficiently high forward bias (>0.8 V) the ‘S shape’ in the first quadrant is present even in the device without any defective layer or interface defects (see Fig. A6.4d). Moreover, for the DL_CB and DL_VB models, the ‘S shape’ in I-V at low temperatures in only the first quadrant is observed. On the contrary, Fermi level pinning at the interface leads to an ‘S shape’ in the first and fourth quadrant. The ‘S shape’ in the first quadrant in all the models is due to the presence of a cliff at the CdS/ZnO interface (see Fig. 6.9a). Consequently, the electron density in the CdS layer is very low, which requires a significant gradient in the electron quasi-Fermi level to drive the diode current.

In contrast, in the case without cliff-like band alignment and thus higher electron concentration in the CdS layer, that drop of the electron quasi-Fermi level ΔE_{Fn}^{CdS} in the CdS buffer layer would otherwise contribute to the quasi Fermi level splitting in the $CuInSe_2$ absorber and therefore yield a higher diode current, *i.e.* no S shape in the 1st quadrant. Therefore, it can be concluded that it is the cliff at the CdS/ZnO interface together with the defective layer or defective interface that leads to an ‘S shape’ in the first quadrant of I-V curve.

As for the ‘S shape’ in the fourth quadrant, the acceptor type interface defects introduce a negative charge at the interface, which significantly reduces the band bending inside the absorber (see Fig. 6.9b). Consequently, at the $CuInSe_2$/CdS interface, the electron Fermi-level is further away from the CBM, and therefore, the device has a high φ_b^p. Comparatively, in the defective interface model, the defects near the interface contribute to the total charge of the absorber, leading to a steeper band bending inside the absorber. Thus, the φ_b^p for this device is lower.

According to equation 2.39, the device with interface defects has a lower J_{TE} compared to the device with the defective layer. This is exactly what is observed in the simulated I-V curves of the device. The J_{ph} of the device with interface defects is limited by the J_{TE} across the interface. The J_{TE} and hence the J_{ph} across the interface decreases further as forward bias is applied because the drop in Fermi-level is reduced (as discussed in section 4.2.4), thus leading to an 'S shape' in the first quadrant. In contrast, for the device with the defective interface, the J_{TE} is high enough and does not limit the J_{ph}. Hence no 'S shape' in the I-V curve. Thus, the model with a defective layer best describes the experimental I-VT behavior of the Cu-rich $CuInSe_2$ device.

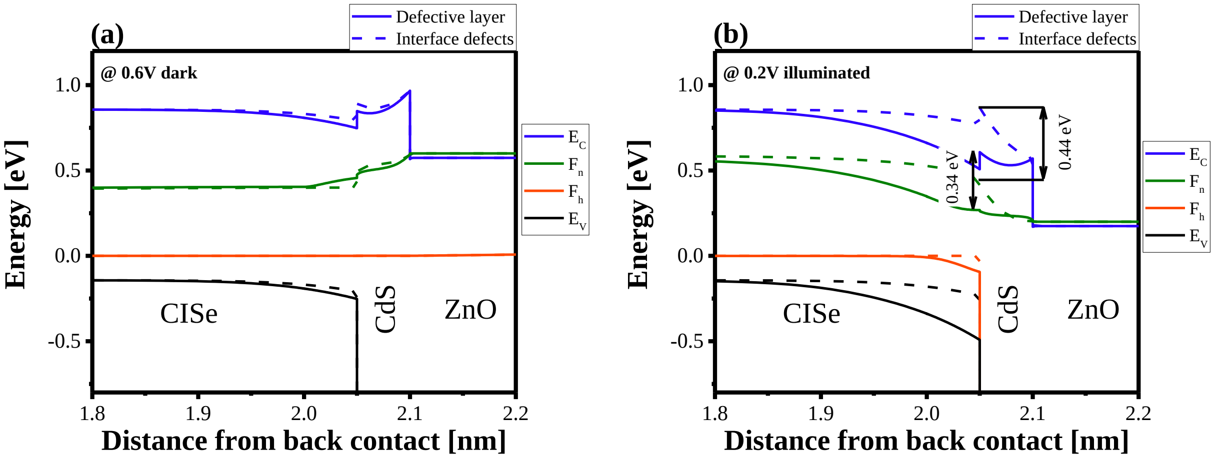


Figure 6.9: *Simulated band diagram of $CuInSe_2$ device with defective layer and interface defects (a) in the dark at 0.6 V at temperature 250K (b) under illumination at 0.2V at 250K.*

It is worth mentioning that although in the above situation, the defective interface does not lead to 'S shape' in the I-V curve, however, this does not hold true in general. In fact, the defects near the interface do lead to a reduction of the electrons near the interface, and therefore $E_{n,a}$ (in equation 2.39), leading to an increase in φ_b^p (as compared to the device without interface defects). Therefore, a situation can be envisioned either with high defect concentration or a high absorber/buffer CBO spike that results in large φ_b^p. Such a scenario, where the density in the defective layer and CBO at the absorber/buffer interface is varied was simulated and the corresponding I-V curves are shown in Fig. 6.10a and b and the I-V curves without defective layer is shown in Fig. A6.6c. In both cases, either with a high defect density for a particular CBO at the absorber/buffer interface or with high CBO for a particular defect density in the defective layer an 'S shape' in the I-V curve is observed. Thus, when present in high concentration, a defective layer can also lead to 'S shape' in the I-V curve. Therefore, the defective layer can explain even the I-V curves of the un-treated Cu-rich $CuInS_2$ solar cells, which exhibit 'S shape' in the fourth quadrant (see section 4.4).

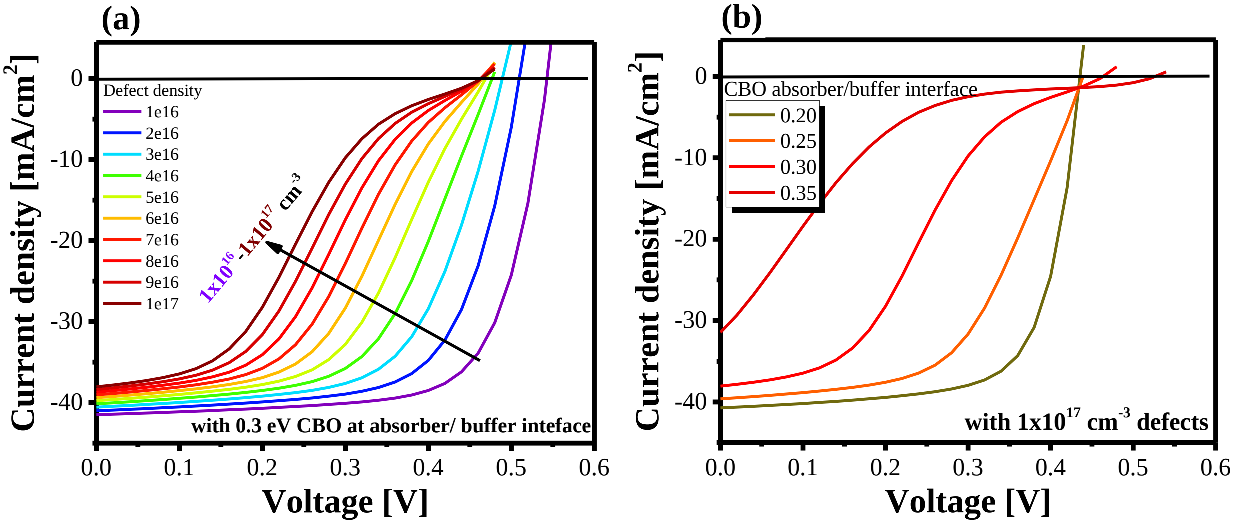


Figure 6.10: *Simulated I-V curves of $CuInSe_2$ device with DL_CB, (a) shows the impact of defect density, with a CBO of 0.3 eV at the absorber/buffer interface (b) shows the impact of CBO at the absorber/buffer interface with $1\text{x}10^{17}$ cm^{-3} defects in the defective layer.*

6.3.2 Numerical simulations for interface V_{OC} deficit in $CuInS_2$ devices

Having established that the DL_CB model can explain the experimental observations of $CuInSe_2$ solar cell (to a reasonable extent), we try to simulate a $CuInS_2$ device with the DL_CB model. However, this requires information regarding the defect responsible for the interface V_{OC} deficit. For this purpose, DLTS measurements were performed on $CuInS_2$ solar cell and $CuInS_2$ Schottky devices. Fig. 6.11a and b show the DLTS spectrum of the two samples and the activation energy of the traps corresponding to the peaks observed in the spectrum. In the devices, three majority carrier traps: '(1)', '(2)' and '(3)' were obtained, having activation energy of 298 meV, 484 meV, and 571 meV. In the Schottky device, two majority carrier traps: '(1)' and '(2)' were observed, whereas in solar cell, majority carrier trap '(1)' and '(3)' were observed. Both the devices contain the signature of trap (1). Therefore it might be that this trap causes interface V_{OC} deficit. We do not claim that this is indeed the defect that causes the interface V_{OC} deficit in these devices. Because confirming this requires further experiments and analysis, which were not performed in this work due to time constraints.

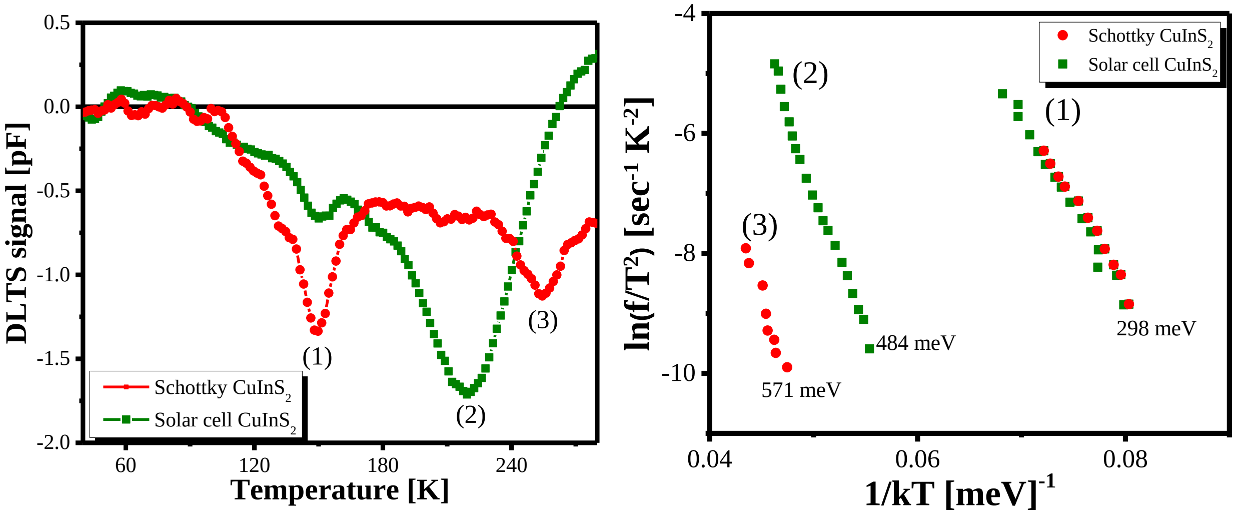


Figure 6.11: *(a) DLTS signals of the KCN etched $CuInS_2$ schottky junction device (red) and solar cell (olive) and (b) the corresponding Arrhenius plot.*

Based on the results of DLTS measurements, we model the $CuInS_2$ device. The parameters used for this simulation are reported in table A6.2. For ease of simulation, we replaced the bandgap of $CuInSe_2$ with $CuInS_2$ and of CdS with Zn(O,S), keeping all other material parameters the same. As for the defects, the $V_{OC,ex}$ limiting 200 meV defect, was replaced by 300 meV defect. Other than the 300 meV defect, to obtain an $V_{OC,in}$ comparable to the experimentally measured value (table 5.1), a deep defect around 0.7 eV is also introduced in the $CuInS_2$ layer.

Fig. 6.12a shows the simulated $V_{OC,ex}$ on the left axis and interface V_{OC} deficit on the right axis, both plotted as a function of defects density. The interface V_{OC} deficit and consequently a drop in $V_{OC,ex}$ increases as the defect density increases. Moreover, the model also produces an $E_a < E_G$, which decreases with the increase in defect density Fig. 6.12b. These results agree with the I-V measurements on the S-PDT devices discussed in section 5.3. Thus, confirming that the DL_CB model applies to even $CuInS_2$ solar cells as well.

It is established that the model with a DL_CB model explains, to a good extent, the experimentally observed Cu-rich $CuInSe_2$ and $CuInS_2$ device characteristics, including the 'S shape' in the first quadrant of the I-V curves. At this point, it is worth summarizing a few points regarding the models. All the models lead to a significant interface V_{OC} deficit in the device and an $E_a < E_G$. The exact value of both V_{OC} deficit and E_a depends on the defect properties such as defect energy, density, and capture cross-section. However, the exact mechanism in the two cases is different: in the defective layer model, the main recombination is in the SCR close to the surface. On the contrary, the absorber/buffer interface is the location of the main recombination channel in the defective interface model, and leads to a weak electron Fermi level pinning as evident from Fig. 6.8b where E_b changes only weakly with temperature. The E_a is given by the value of E_b^h at 0 K.

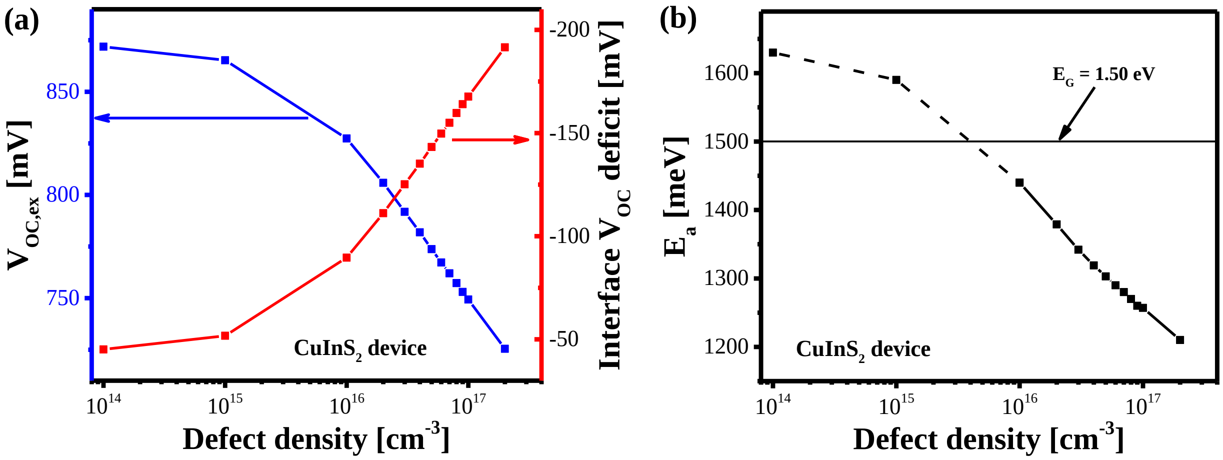


Figure 6.12: *(a) Simulated $V_{OC,ex}$ on left axis and interface V_{OC} deficit on right axis as a function of defect density in the defective layer in $CuInS_2$ solar cells. (b) The E_a obtained from extrapolation of simulated $V_{OC,ex}$ to zero K as a function of defect density in $CuInS_2$ solar cell. The points above the E_G might be a numerical artifact.*

The models presented here might not be entirely accurate, as they do not include many factors such as surface E_G widening or band offsets between absorber and buffer. Still, the models do a decent job of reproducing the main experimental characteristics of Cu-rich $CuInSe_2$ and $CuInS_2$ devices that indicate a problematic interface and provide a suitable explanation. Among the models presented, the DL_CB model explains better the observed admittance spectra of Cu-rich $CuInSe_2$. Furthermore, it was shown that the most critical parameters indicating interface recombination, *i.e.* a significant difference between $V_{OC,in}$ and $V_{OC,ex}$, and an E_a of saturation current lower than E_G can be reproduced by a model that contains neither a reduced interface bandgap nor Fermi level pinning.

6.4 Summary

This chapter explored the origin and characteristics of near-surface defects in Cu-rich $CuInSe_2$ solar cells and how they lead to interface recombination in $CuInSe_2$ and $CuInS_2$ devices. It was established that the presence of near surface acceptor defects is caused by etching the secondary $Cu_{2-x}Se$ phase in Cu-rich $CuInSe_2$ and probably in $CuInS_2$ devices the same phenomena occurs. The admittance measurements on the Cu-rich $CuInSe_2$ absorbers etched with aqueous KCN, and aqueous Bromine solutions reveal the presence of the 200 meV defect signature in both devices, independent of the etchant used for removal of $Cu_{2-x}Se$ phase. The results establish the 200 meV defect to be an intrinsic part of Cu-rich devices originating from the etching of secondary phases. Moreover, it was observed that the defect signature is usually in the form of broad peaks in admittance defect signature. The DLTS measurements made on KCN etched Cu-rich $CuInSe_2$ device exhibit a negative capacitance change peak, thus confirming the defect to be an acceptor defect, as speculated by Dr. Elanzeery[74]. In addition, admittance spectra of the devices prepared with several PDT $CuInSe_2$ absorbers demonstrate that the usual broad admittance defect signature is produced by the response from two defect levels close to each other, as shown in the S-PDT device. Also that the 200 meV defect signature can be a divacancy defect, as the defect can be (partially) passivated *via* the Zn and S-PDT.

Numerical simulations demonstrated that both a near interface defect model and the interface defect model can reproduce the electrical characteristics of Cu-rich $CuInSe_2$ devices, in particular reduced $V_{OC,ex}$ compared to $V_{OC,in}$. The reduction emanates due to deep traps at or near the surface, which lead to strong non-radiative recombinations in the region near the surface and dominate the $V_{OC,in}$ near the surface. Consequently, the $V_{OC,in}$ decreases rather abruptly near the surface resulting in a reduced $V_{OC,ex}$, thus resulting in an interface V_{OC} deficit in the device. The reduction in electron concentration near the interface leads to a high barrier for both injected and photogenerated electrons. Thus depending upon the CBO at the absorber/buffer interface and at the buffer/i-layer interface it is possible to have 'S shape' in fourth quadrant and rollover in first quadrant, which would not be observable in devices without near interface defects.

Moreover, it was demonstrated that the presence of both a defective surface and a defective interface lead an E_a of the saturation current density obtained by temperature-dependent $V_{OC,ex}$ measurements lower than the bulk E_G of the absorber. Both the devices can lead to 'S shape' in I-V curves of the device. The 'S shape' in the first quadrant was linked to the drop of the electron quasi-Fermi level ΔE_{Fn}^{buffer} in the buffer due presence of a cliff at the buffer/i-layer interface. In contrast, the 'S shape' in the fourth quadrant was linked to a high φ_b^p, which originates from either a weak band bending in the absorber and drop in Fermi-level near the interface (in case of interface defects model), or a substantial drop in Fermi-level near the interface (in case of defective layer model). Thus, the near interface defect model successfully explains the interface V_{OC} deficit and an activation energy E_a less than the E_G for the Cu-rich $CuInSe_2$ and $CuInS_2$ devices. Additionally, it can also explain the presence of barriers in the form of 'S shape' in the I-V curves in the device.

Chapter 7

Conclusion

In this work, we achieved two significant milestones for $Cu(In,Ga)S_2$ solar cells by addressing the interface V_{OC} deficit. (1) We minimized interface V_{OC} deficit and obtained high $V_{OC,ex}$ values using Cu-poor $Cu(In,Ga)S_2$ absorbers through optimization of buffer and i-layer. (2) We devised a near interface model, which revealed that it is the near interface defects that limit the $V_{OC,ex}$ of the Cu-rich chalcopyrite solar cells.

In this thesis, by comparing Cu-rich and Cu-poor $Cu(In,Ga)S_2$ prepared with different buffers and numerical simulations, we get the following results: For Cu-poor $Cu(In,Ga)S_2$ devices, we established an interface V_{OC} deficit which originates from: (i) a conduction band cliff at the absorber/buffer interface, (ii) a conduction band cliff at buffer/i-layer interface in devices with a conduction band spike at the absorber/buffer interface and (iii) a loss in $V_{OC,in}$ during heating of Cu-poor $Cu(In,Ga)S_2$ during and after buffer deposition leading to an overall interface deficit.

We mitigated these issues using different strategies:

(i) Alternative buffer layer: We showed in chapter 4 (section 4.1) that CdS has an $E_a < E_G$ for the dominant recombination path, which is given by the $E_{G,IF}$. Using Zn(O,S) buffer layer, the interface recombinations were suppressed by introducing a spike-type conduction band alignment. The device had an $E_a = E_G$ for the dominating recombination path as the $E_{G,IF} = E_G$.

(ii) Alternative i-layer: We observed in chapter 4 (section 4.2) that a cliff at $Zn_{1-x}Mg_xO$/ZnO (buffer/i-layer) interface, particularly with 'x' ≥ 0.3, led to a high interface V_{OC} and low FF in the devices. Although the devices have a conduction band spike at the $Cu(In,Ga)S_2/Zn_{1-x}Mg_xO$ (absorber/buffer) interface and consequently $E_a = E_G$. By utilizing Al:ZnMgO as an i-layer, we improved not only the FF but also the interface V_{OC} deficit in the resulting devices. We have also revealed, using numerical simulations, that a high barrier for electrons in the device causes a drop in electron Fermi-level near the interface in $Zn_{1-x}Mg_xO$/ZnO devices leading to interface V_{OC} deficit.

(iii) Low-temperature buffer deposition: A drop in $V_{OC,in}$ was observed for absorbers covered with Zn(O,S) buffer layer after annealing on a hot plate at 200 °C and deposition of ZnMgO at 150 °C, in chapter 4 (section 4.3). We have successfully shown that using ZnSnO buffer layer deposited at temperatures ≤ 120 °C, the drop in $V_{OC,in}$, and therefore, the global interface V_{OC} deficit can be reduced.

Using this new knowledge, we accomplished 14.0 % PCE in an externally certified ZnSnO device, which is the second-highest certified device, until writing this thesis. We also achieved an in-lab 15.1 % PCE Zn(O,S) device and 14.0 % PCE ZnMgO device showing that it is possible to make highly efficient solar cells using Cu-poor $Cu(In,Ga)S_2$ absorbers.

Now the question remains why does Cu-rich $Cu(In,Ga)S_2$ show a high interface V_{OC} deficit? We establish that it is neither due to unfavorable CBO at the absorber/buffer interface nor due to Fermi-level pinning. Instead, we demonstrate that near-surface defects causing interface recombinations are the source of interface V_{OC} deficit.

- It is not due to unfavorable CBO at the absorber/buffer interface: We showed with different buffer layers and band energetic measurements in chapter 4 (section 4.1) and 5 (section 5.2) that the Cu-rich devices suffer from interface V_{OC} deficit due to recombination at the interface independent of the CBO at the absorber/buffer. Both devices made with Zn(O,S) buffer layer and ZnMgO buffer layer had a high interface V_{OC} deficit and an $E_a < E_G$, suggesting possibly Fermi-level pinning in the device.
- Fermi-level pinning is not the cause of interface recombination: Using photoelectron spectroscopy in chapter 5 (section 5.2), it was revealed that the Fermi-level of the devices changes its position as we deposit Zn(O,S) buffer layer on Cu-rich $CuInS_2$ absorbers. The IIBB values changed throughout the deposition of Zn(O,S) buffer on top of Cu-rich $CuInS_2$ absorbers eliminating Fermi-level pinning at the interface as the cause of interface recombination.
- Near-surface defects are the source of interface recombinations: In chapter 5 (section 5.3) We observed a reduction in interface V_{OC} deficit and an improvement in the E_a of the recombination path with TU-PDT. In the untreated device, we observed 'S shape' in the first I-V quadrant and slow capacitance transients suggesting the presence of metastable deep defects. However, in the facile TU-PDT device, both 'S shape' and the slow capacitance transients were reduced significantly, implying that the metastable defects are passivated. Since the PDT are performed

at a low temperature ~80 °C, it is reasonable to assume that it passivated defects at or near the absorber surface, exposing that the defects causing interface recombination are at or near the interface.

We have offered a near interface defect model in chapter 6, which displayed all the signatures of interface recombination in numerical simulations. Our simulations showed that highly recombinative defects dispersed throughout a layer near the interface anywhere in the bandgap lead to a local drop-in $V_{OC,in}$ leading to a $V_{OC,ex}$ lower than the highest $V_{OC,in}$ of the absorber. The device in this situation results in an $E_a < E_G$, which is the signature of interface recombinations even though the dominating recombinations are occurring near the interface and not at the interface. Because of the model presented in this thesis, it is finally possible to answer the perplexing question, “Why Cu-rich chalcopyrite solar cells are limited in their $V_{OC,ex}$ and show interface recombination signature?”

Our model has extensive implications as it now provides a third new mechanism that gives all the signatures of interface recombination and can be applied to any device with highly recombinative defects near the interface.

Outlook

Having identified the cause of interface recombination in this thesis, the onus is to passivate near interface defects using techniques similar to proven In-Se treatment for $CuInSe_2$.

Depending upon the stoichiometry and whether the annealing takes place after buffer deposition or after complete device fabrication, annealing had a different impact on the $Cu(In,Ga)S_2$ solar cell's device performance, particularly on FF. This suggests that the barrier height is modified differently in each case, although the reason remains unknown. Therefore it makes for an interesting study to probe the effect of annealing on band alignment and Fermi-level position in the device structure using photoelectron spectroscopy.

Also, annealing Cu-poor device after Zn(O,S) buffer deposition showed promising results, a drop in $V_{OC,in}$ was observed. The heating of the absorber during ALD buffer deposition showed a similar drop. To clarify the reason for the drop in the absorber $V_{OC,in}$ have to be probed before and after buffer deposition and annealing. One possible origin of this drop could be the migration of Zn into the $Cu(In,Ga)S_2$ absorber, which might lead to lower absorber doping by passivating Cu vacancies. This can be explored with the help of C-V measurements on samples before and after the buffer deposition process. Another possibility would be measuring lifetime and $V_{OC,in}$ and combing them to extract the doping.[205]

Most of the devices, including even the best devices presented in this thesis, showed hysteresis and presence of metastabilities, including the degradation of device performance with time. However, the root cause of these metastabilities was not explored in this thesis. The most commonly evoked model for metastability in $CuInSe_2$ is the Cu-Se divacancy defect model. It might be that a similar phenomenon causes metastabilities in $Cu(In,Ga)S_2$ devices too. Growth of $Cu(In,Ga)S_2$ under different sulfur partial pressure and the investigation of devices with one particular buffer layer under different voltage and light bias conditions might help explore the metastabilities in these solar cells.

Numerical simulations show that the barrier height can be reduced by omitting the i-layer and consequently, a higher FF can be achieved. However, the results of ZnSnO buffer devices without an i-layer showed that this requires a buffer layer that can provide better protection against sputter damage during Al:ZnO deposition. In the future, deposition of Al:ZnO using soft methods such as ALD or metal-organic chemical vapor deposition can be pursued.

The DLTS measurements on Cu-rich $CuInS_2$ showed the presence of three majority carrier traps. However, due to limited setup availability and time constraints, the influence of S-PDT on these majority carrier traps was not studied. In the future, DLTS measurements can be done on devices that are post-deposition treated to see its influence on majority carrier traps. This can help identify the defect causing of interface V_{OC} deficit which can be linked to other PL measurements too.

Appendix Chapter 4

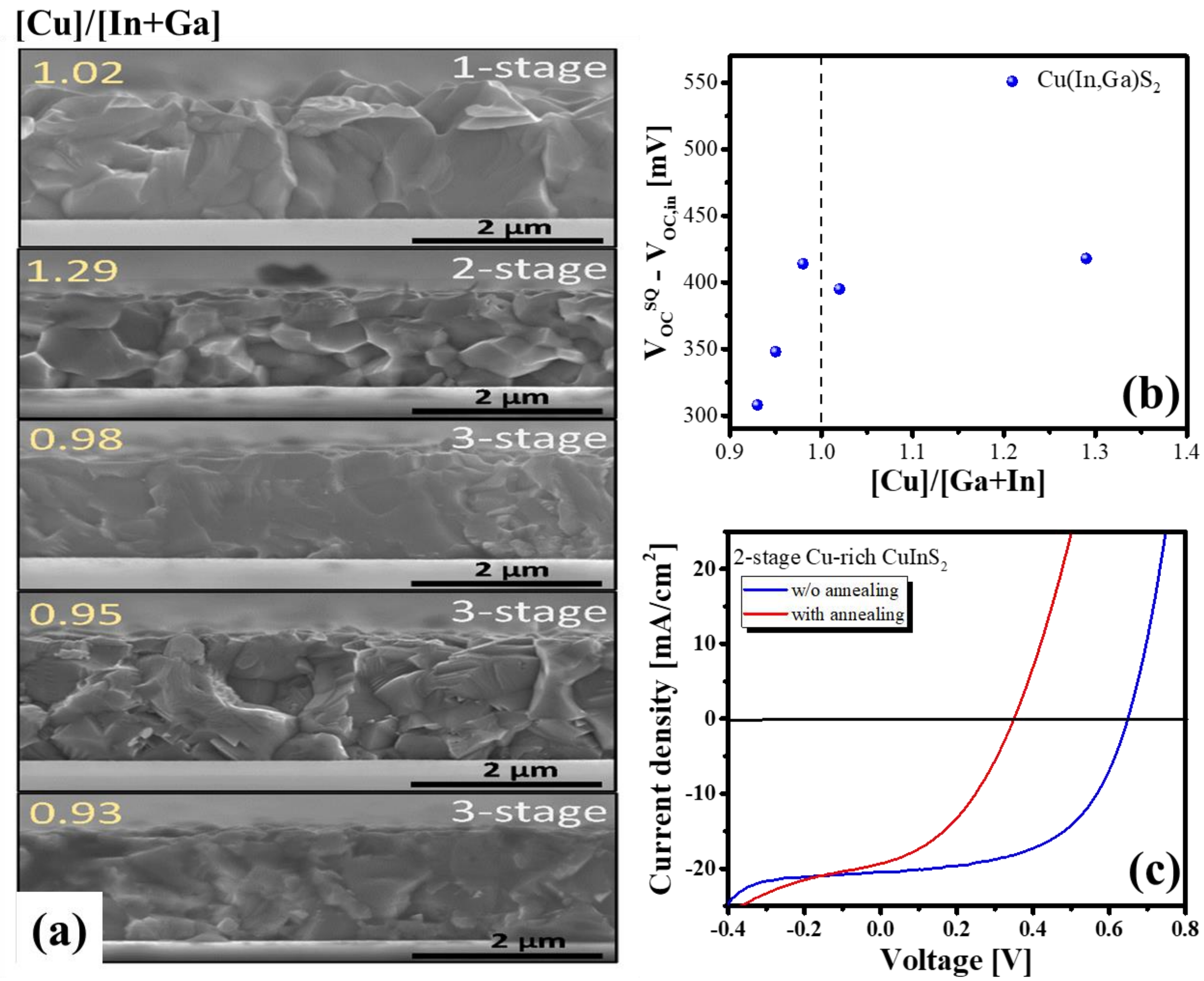


Figure A4.1: ***(a)*** *SEM cross-sectional image of Cu(In,Ga)S_2 absorbers prepared using 1, 2 and 3-stage deposition process. The number in yellow gives the as grown [Cu]/[In+Ga] atomic concentration in the films. (b) Deficit between Shockley-Queisser V_{OC} [177, 237] and $V_{OC,in}$ as a function of stoichiometry of Cu(In,Ga)S_2 absorbers.[73] The Cu-poor Cu(In,Ga)S_2 absorbers possess lower deficit between the V_{OC}^{SQ} and $V_{OC,in}$ compared to Cu-rich absorbers, suggesting a higher optoelectronic property for Cu-poor composition. (c) I-V curves of 2-stage Cu-rich CuInS_2 device before and after annealing. Annealing leads to a significant reduction in device V_{OC} and FF.*

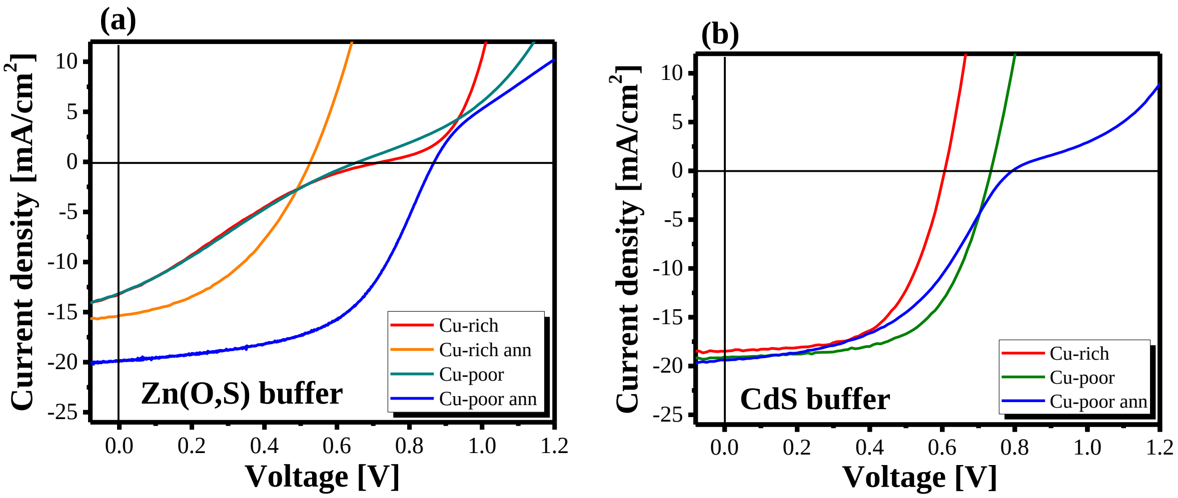


Figure A4.2: *I-V curve of Cu-rich and Cu-poor Cu(In,Ga)S_2 device prepared with (a) Zn(O,S) buffer layer (b) CdS buffer layer.*

Table A4.1: *I-V characteristics of best Cu-rich and Cu-poor Cu(In,Ga)S_2 device with either Zn(O,S) or CdS buffer layer.*

	Efficiency (%)	FF (%)	J_{SC} (mA/cm^2)	$V_{OC,ex}$ (mV)	$V_{OC,in}$ @1sun (mV)	$V_{OC,in} - V_{OC,ex}$ (mV)
Cu-rich/Zn(O,S)	2.0	21.0	13.2	723	872	149
Cu-rich/Zn(O,S) annealed	3.5	42.6	15.4	527	872	345
Cu-rich/CdS	6.7	59.7	18.5	607	872	265
Cu-poor/Zn(O,S)	2.1	24.5	13.2	658	885	227
Cu-poor/Zn(O,S) annealed	9.5	54.9	19.9	868	885	17
Cu-poor/CdS	8.5	60.7	19.1	732	885	153
Cu-poor/CdS annealed	7.2	47.0	19.4	795	885	90

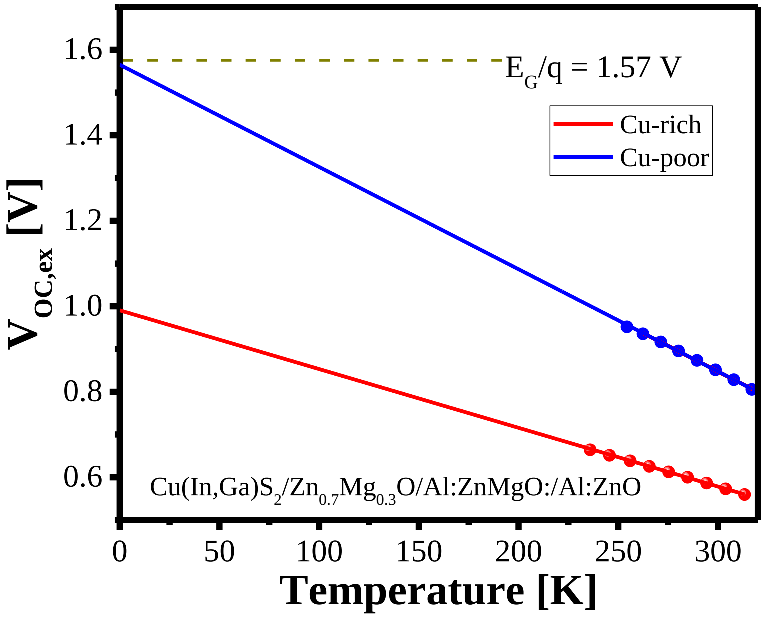


Figure A4.3: *$V_{OC,ex}$ as a function of temperature for Cu-rich and Cu-poor device prepared with $Zn_{0.7}Mg_{0.3}O$ buffer layer, extrapolation to 0 K gives activation energy of saturation current density.*

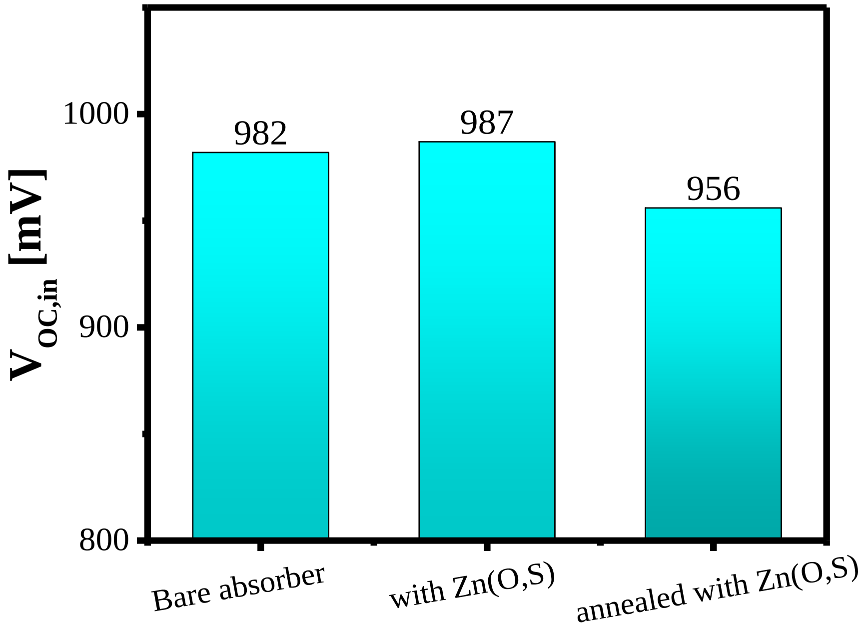


Figure A4.4: *(a) $V_{OC,in}$ bar chart of Cu-poor Cu(In,Ga)S_2 absorber without buffer, with chemical bath deposited Zn(O,S) buffer and annealed Cu(In,Ga)S_2/Zn(O,S) device stack. A reduction of 31 mV in $V_{OC,in}$ is observed after annealing.*

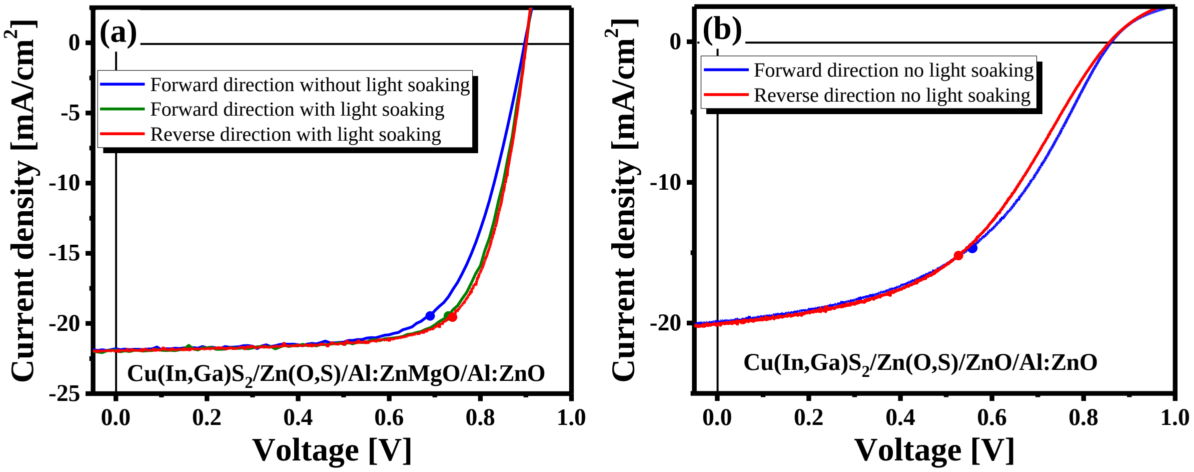


Figure A4.5: *(a) I-V curves of the best Cu-poor Cu(In,Ga)S$_2$ device prepared with Zn(O,S) buffer layer showing the effect of light soaking in hysteresis in I-V curves. In blue without any light soaking measured in the forward direction, in olive with 30 minutes light soaking measured in the forward direction and in red 30 minutes light soaking measured in the reverse direction. The dots show the maximum power point of the respective curves. It is clear that light soaking leads to improvement in the maximum power point, and also the device shows hysteresis with reverse direction measurement leading to a slightly higher maximum power point in the device. (b) I-V curve of another Cu-poor Cu(In,Ga)S$_2$ device prepared with Zn(O,S) buffer layer showing hysteresis in I-v curves.*

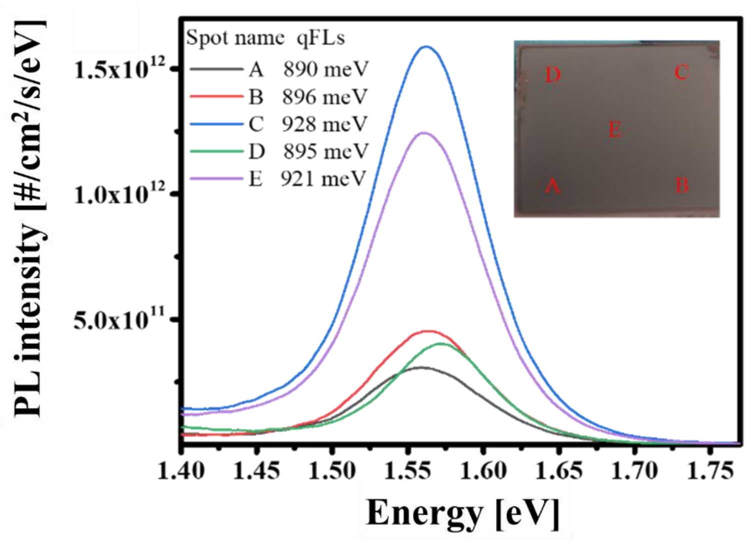


****Figure A4.6:*** *Exemplary calibrated PL spectra of one of the absorbers used to fabricate device. The $V_{OC,in}$ is obtained by transforming this PL spectra using Planck's generalized law as explained in Ref[83, 157]. The PL signal varies in the sample at different spots and hence the $V_{OC,in}$.*

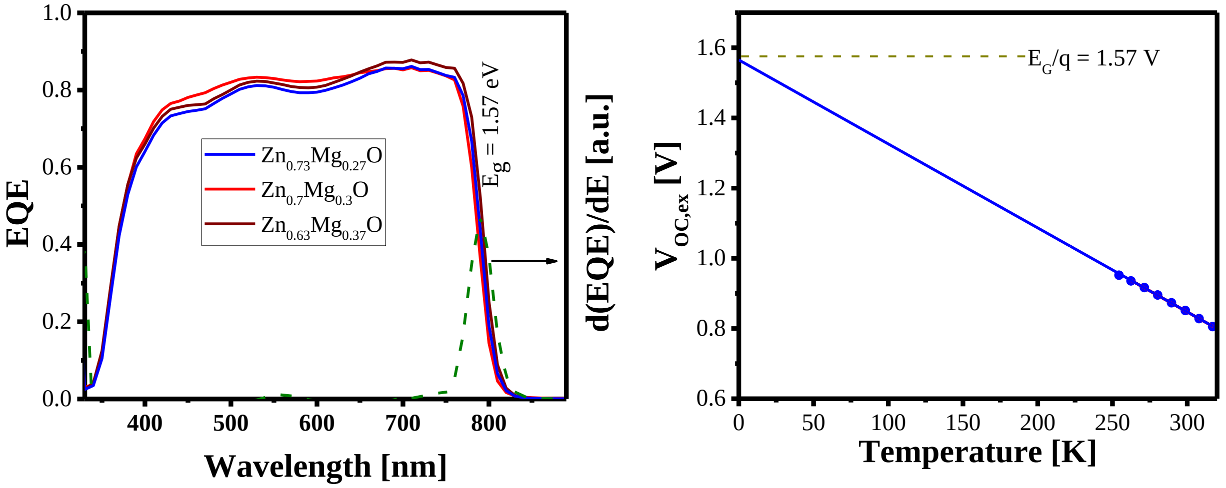


Figure A4.7: *(a) External quantum efficiency of Cu-poor Cu(In,Ga)S_2 solar cell prepared with different $Zn_{1-x}Mg_xO$ buffer layer deposited using ALD. The band gap of the absorber is obtained from derivative of the external quantum efficiency w.r.t. energy derivative. (b) $V_{OC,ex}$ plotted as a function of temperature for Cu(In,Ga)S_2/$Zn_{0.73}Mg_{0.27}O$/Al:ZnMgO/Al:ZnO device, the extrapolation of $V_{OC,ex}$ nearly is equal to the E_G/q suggesting bulk dominated device.*

Influence of annealing during or after buffer deposition on $V_{OC,in}$ and V_{OC}:

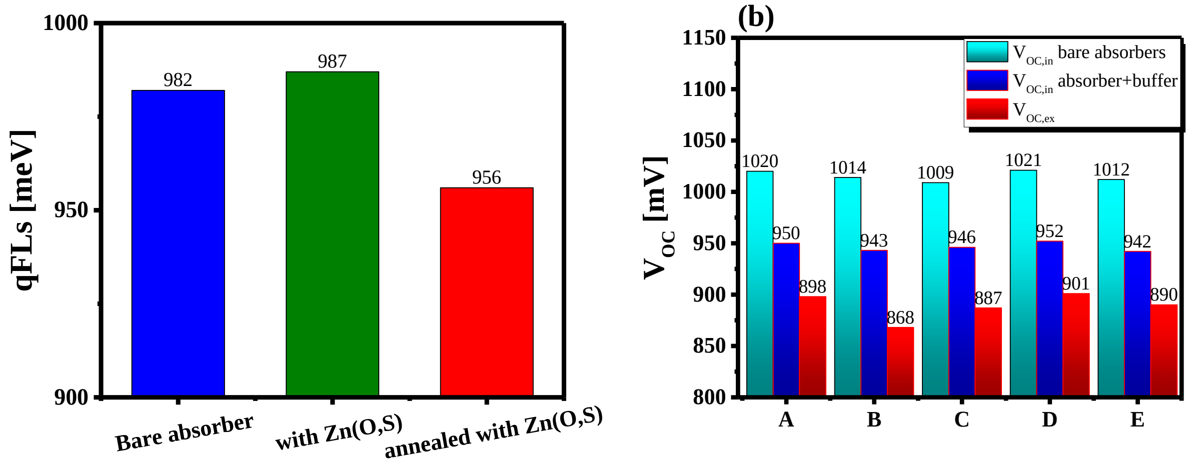


Figure A4.8: *(a) Bar chart showing $V_{OC,in}$ values of Cu(In,Ga)S_2 absorber without buffer (bare absorber), with chemical bath deposited Zn(O,S) buffer and with Zn(O,S) buffer annealed at 200 °C for 10 minutes. (b) Bar chart of Cu(In,Ga)S_2 absorber showing $V_{OC,in}$ of bare absorber, Cu(In,Ga)S_2 absorber with ALD deposited $Zn_{0.73}Mg_{0.27}O$ and open-circuit voltage of the final device. A degradation in $V_{OC,in}$ of absorber has been observed whenever the absorber is annealed during the buffer deposition or after the buffer deposition.*

Table A4.2: *SCAPS-1D numerical simulation parameters used to in this work. For achieving a value of* $V_{OC,in}$ *comparable to optically measured value, a deep defect level at 520 meV is introduced in the* $Cu(In,Ga)S_2$ *absorber layer. A* R_s *of 0.3 Ω-cm*$^{-2}$ *and* R_{sh} *of 1000 Ω-cm*$^{-2}$ *was used.*

Parameter	**Cu(In,Ga)S₂**	**ZnMgO**	**Al:ZnMgO**	**ZnO**	**Al:ZnO**
Thickness (µm)	2.0	0.03	0.07	0.07	0.352
Band gap(eV)	1.57	3.5-3.7	3.5	3.3	3.45
Dielectric permittivity (relative)	10	10	10	10	10
Electron affinity(eV)	4.4	3.95-4.4	3.95-4.4	4.6	4.6
Electron mobility(cm^2/Vs)	20	20	20	20	50
Hole mobility(cm^2/Vs)	10	10	10	10	10
Doping(1/cm^3)	$1x10^{15}$	$1x10^{17}$	$1x10^{17}$	$1x10^{17}$	$5x10^{19}$
Defect density(1/cm^3)	$2x10^{16}$ acceptor 350meV from VBM	-	-	-	-
Capture cross-section Electrons & holes (cm^{-2})	$1x10^{-14}$ & $1x10^{-15}$	-	-	-	-

I-V and EQE of best device:

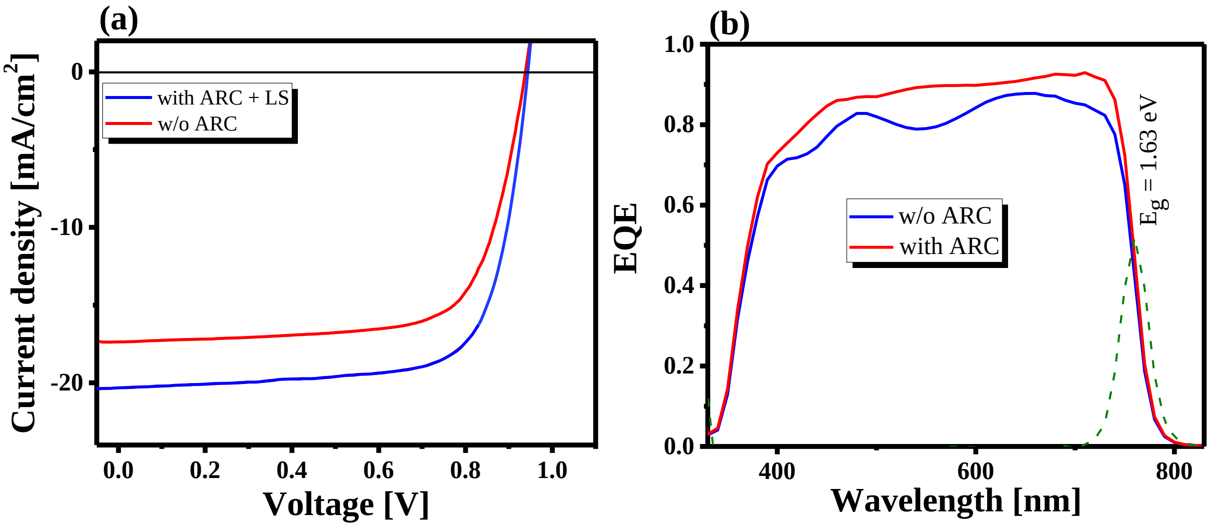


Figure A4.9: *(a) I-V curve and (b) EQE curve of the* $Cu(In,Ga)S_2$ *device having a PCE of 14.0 % prepared with* $Zn_{0.73}Mg_{0.27}O$ *buffer layer and sputtered Al:*$Zn_{0.75}Mg_{0.25}O$ *i-layer with and without anti-reflective coating of* MgF_2*.*

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* Taken directly from [159].

EQE of device prepared with ZnSnO buffer layer

Overall, among all the devices fabricated in the two batches of ZnSnO buffer layers (discussed in section 5.2.2), the of J_{SC} all the devices is almost similar with the exception of $Zn_{0.8}Sn_{0.2}O$ buffer layer device prepared at 120 °C with Al:ZnMgO i-layer, this device shows slightly higher EQE (Fig 5.13b). A comparison of the EQE curves below suggests that this device must have a lower reflectivity compared to other devices. When comparing the same Al:ZnMgO i-layer, it seems that the two devices have different reflectivity in the UV region around 450 nm.

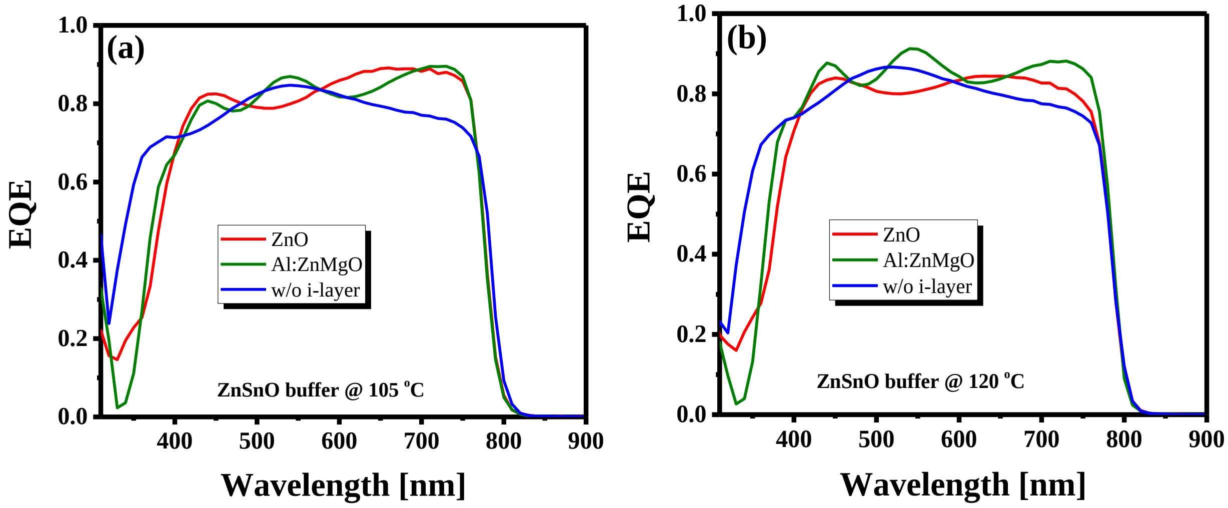


Figure A4.10: *EQE curve of the Cu(In,Ga)*S_2 *device prepared with (a) ZnSnO buffer layer deposited at 105 °C, (b) ZnSnO buffer layer deposited at 125 °C. The red, olive and blue lines represent the devices prepared with ZnO, Al:ZnMgO and without buffer layer.*

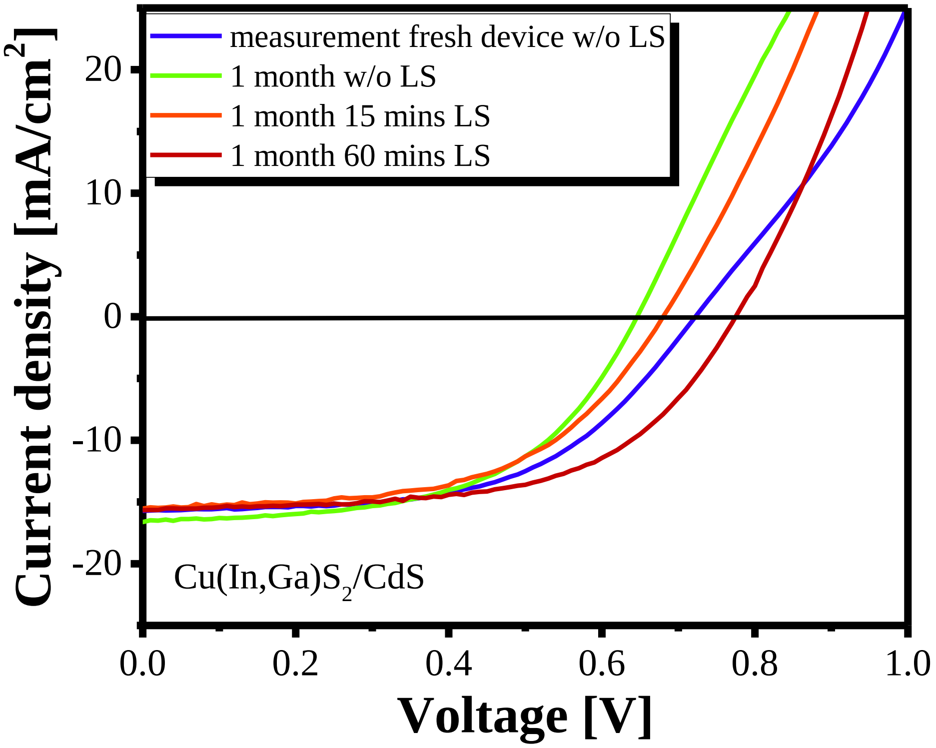


Figure A4.11: *IV curves of the Cu(In,Ga)S$_2$ device prepared with CdS buffer layer measured immediately after making the device and after one month with and without different duration of LS. The results clearly suggest the presence of metastable defects in the device.*

Appendix Chapter 5

Shockley-Queisser V_{OC} and $V_{OC,in}$ Cu(In,Ga)S$_2$ vs CuInS$_2$

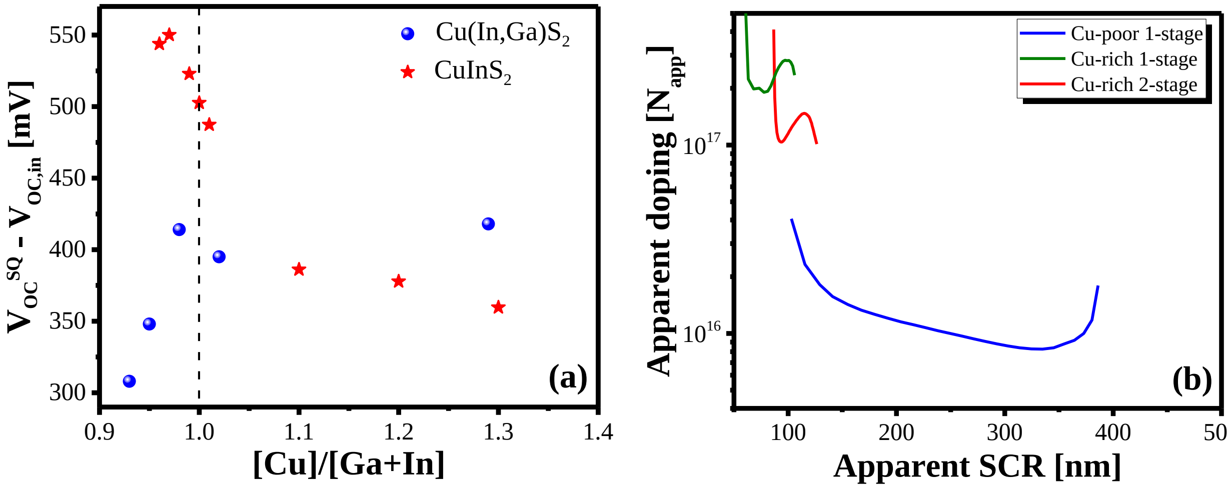


Figure A5.1: *Deficit between Shockley-Queisser V_{OC} [177, 237] and $V_{OC,in}$ as a function of stoichiometry of CuInS$_2$ and Cu(In,Ga)S$_2$ absorbers. Unlike the Cu-poor Cu(In,Ga)S$_2$ absorbers, the Cu-rich CuInS$_2$ absorbers possess lower deficit between the V_{OC}^{SQ} and $V_{OC,in}$ compared to Cu-poor absorbers, suggesting a higher optoelectronic property even for Cu-rich composition. (b) Apparent doping profile versus apparent SCR width for 1-stage Cu-poor (blue) and 1-stage Cu-rich CuInS$_2$ (olive) and 2-stage Cu-rich CuInS$_2$ (red) solar cells.*

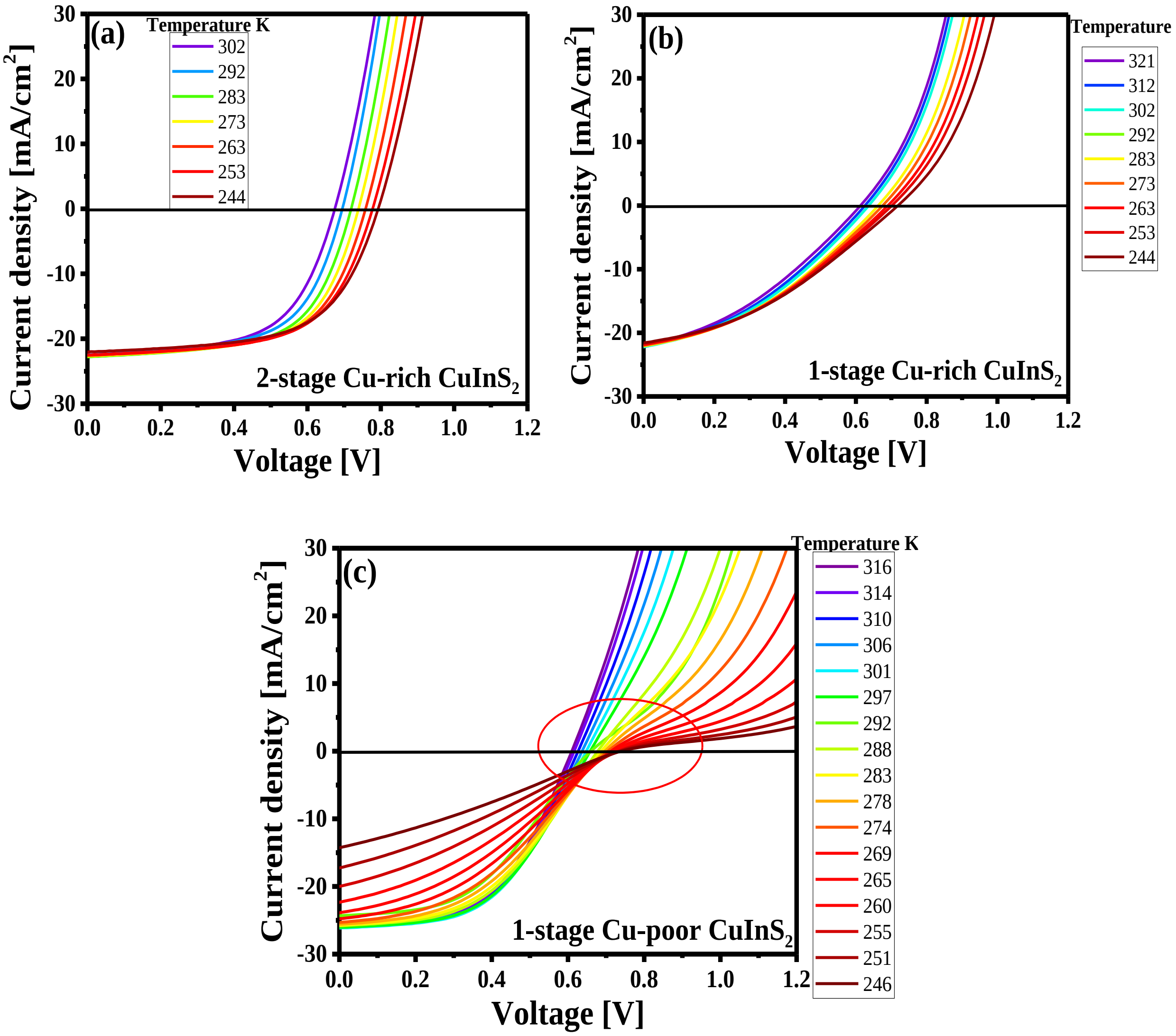


Figure A5.2: *I-V curves measured at different temperatures of best CuInS$_2$ devices with prepared with (a) 2-stage Cu-rich (b) 1-stage Cu-rich and (c) 1-stage Cu-poor as grown absorbers.*

HAXPES spectra of Cu-rich and Cu-poor $CuInS_2$

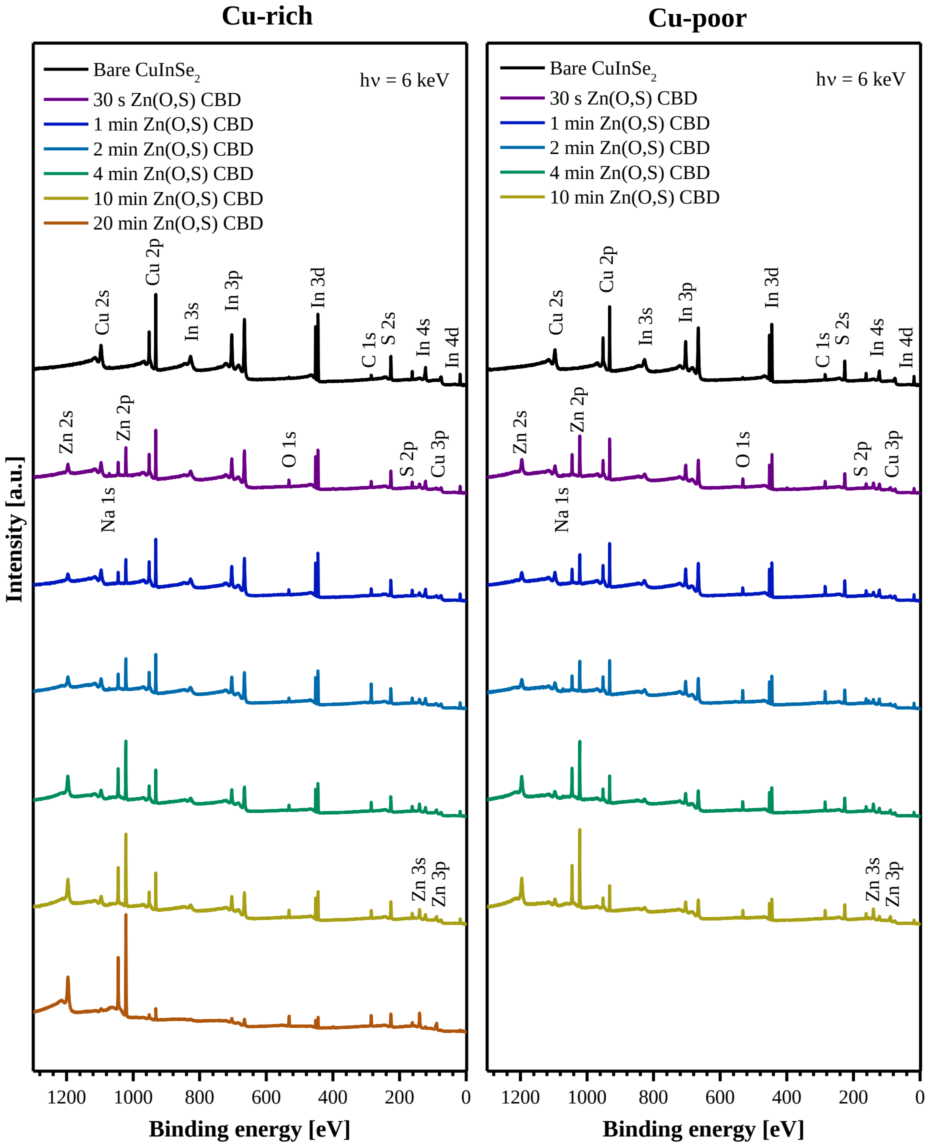


Figure A5.3: *HAXPES (6 keV) survey spectra of Cu rich (left) and Cu poor (right) $CuInS_2$ absorbers with Zn(O,S) layers deposited using CBD for different durations (30 s to 20 min). Spectra are vertically offset for clarity.*

HAXPES S 2p detailed spectra:

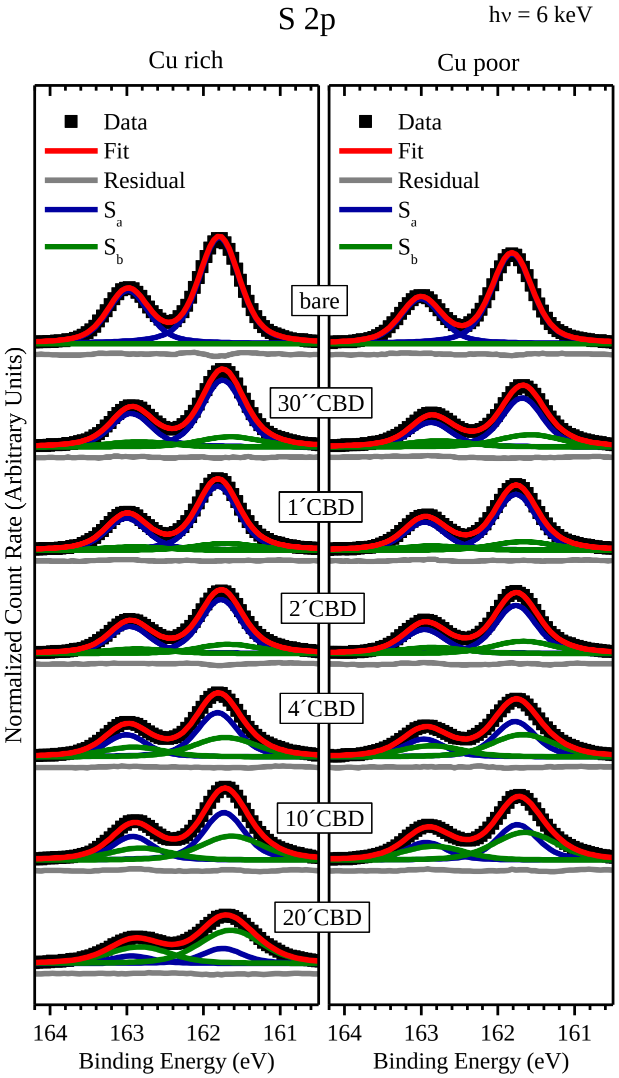


Figure A5.4: *S 2p HAXPES (6 keV) spectra of Cu rich (left) and Cu poor (right) $CuInS_2$ absorbers with Zn(O,S) layers deposited using CBD for different durations (from 30 s to 20 min). Data are shown with a linear background subtracted. Respective fits using pairs of Voigt profiles to represent the respective doublets, are displayed along the data as well as the respective residuals. Spectra are vertically offset for clarity, as are residuals.*

Note, that the shape of S 2p component S_a which was assigned to $CuInS_2$ and component S_b which was assigned to ZnS were allowed to be different due to the expected different crystallinity of the materials. While the high-temperature processed $CuInS_2$ absorber is expected to be well ordered with a high degree of crystallinity, the low-temperature wet chemical deposited Zn(O,S) buffer is expected to have a low degree of crystallinity with even amorphous or nano-crystalline domains resulting in different bond angles and distances leading to a broadening of the Gaussian contribution to the Voigt profile. Also, component S_a (attributed to the $CuInS_2$ absorber) was constrained to follow the same buffer growth–induced intensity attenuation as observed for the Cu and In related photoemission (see **Figure A5.4**).

Zn(O,S) stoichiometry:

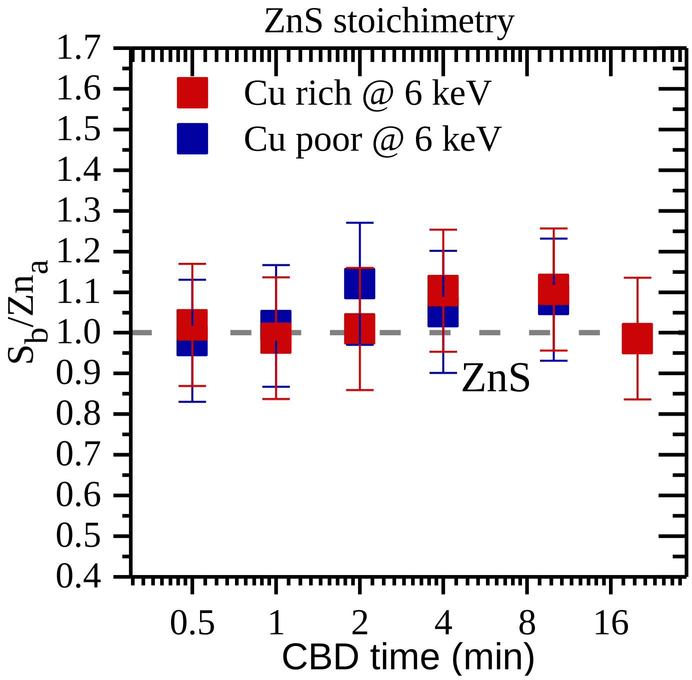


Figure A5.5: *S_b/Zn_a ratio as a measure of S:Zn ratio in the ZnS phase of the Zn(O,S) buffer. Ratio was calculated from spectra displayed in Figure 3 and Figure S14 considering corresponding photoionization cross sections, IMFPs and variations in electron analyzer transmission function.[192, 238, 239]*

To corroborate the assumption of a stoichiometric ZnS and our Zn 3p fit model (Figure 5.4b in the manuscript), we used the information from the S 2p fit (**Figure A5.4**) to calculate Zn_a/S_b ratios, corresponding to the Zn/S ratio of the ZnS phase of the Zn(O,S) buffer layer. It is close to one for all samples as shown in **Figure A5.5**, corroborating the used fit model and the assumption of a stoichiometric ZnS.

Table A5.1: *Binding energies (EB) used for the IIBB calculation displayed in Fig. 5.5.*

Cu-poor	Bare	1´CBD	2´CBD	4´CBD	10´CBD	20´CBD
E_B Zn $2p_{3/2}$		1022.3	1022.2	1022.2	1022.0	1022.0
E_B Cu $2p_{3/2}$	932.9	932.3	932.3	932.2	932.0	
E_B In $3d_{3/2}$	452.3	452.4	452.4	452.3	452.1	
Cu-rich	Bare	1´CBD	2´CBD	4´CBD	10´CBD	20´CBD
E_B Zn $2p_{3/2}$		1022.1	1021.9	1022.0	1022.0	1022.0
E_B Cu $2p_{3/2}$	932.2	932.1	932.1	932.1	932.0	
E_B In $3d_{3/2}$	452.3	452.2	452.18	452.2	452.0	

Bandgap of Zn(O,S) buffer layer:

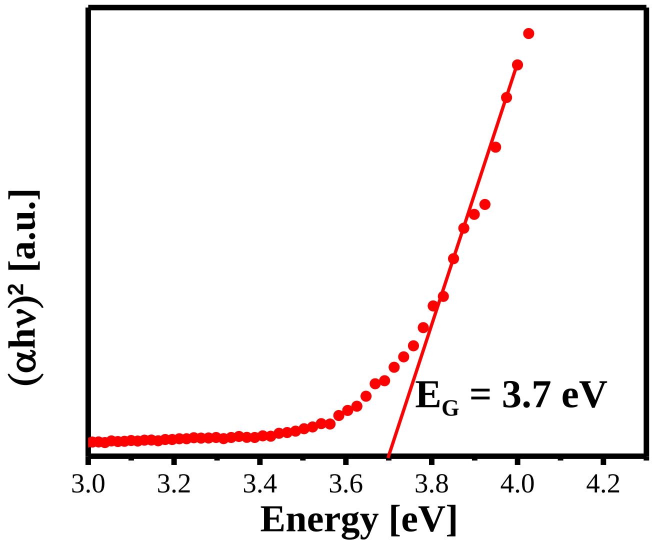


Figure A5.6: *Tauc plot of Zn(O,S) buffer layer, the linear extrapolation gives the band gap of the film.*

*Calibrated photoluminescence measurement and quasi-Fermi level splitting determination

The calibrated photoluminescence measurements to extract the $V_{OC,in}$ have been performed under an equivalent illumination of five suns to ease the spectra acquisitions, to allow for faster and more reliable measurement, in spite of the quite low radiative efficiency of these absorbers. Then, those values have been corrected for one sun illumination, as listed in table 1 in the main part of the manuscript. The correction is based under the assumption that the optical diode factor k is unity, which is defined as:

$$I_{PL} \propto \phi^{k}$$

with I_{PL} and Φ being respectively photoluminescence intensity and excitation density.

Under this assumption, the external radiation efficiency (ERE) is constant as well, as it is defined as the ratio between the integrated PL photon flux density and the incident photon flux density. Because of the low luminescence efficiency, we could not determine *k* for these samples.

The $V_{OC,in}$ is related to the generation under illumination (G_0) and recombination in thermal equilibrium (U_n) by the following relationship [177]:

$$V_{OC,in} = k_B T * \ln\left[\frac{G_0}{U_n} * EQE\right]$$

with k_BT the thermal energy. With ERE constant at different excitations (in the present case at 1 and 5 suns), the $V_{OC,in}$ at 1 sun is thus determined:

$$V_{OC,in(1sun)} = V_{OC,in(5sun)} - \frac{k_B T}{q} * \ln\left(\frac{G_{(1sun)}}{G_{(5sun)}}\right) = V_{OC,in(5sun)} - \frac{k_B T}{q}\ln(5)$$

$$\Rightarrow V_{OC,in(1sun)} = V_{OC,in(5sun)} - 40mV$$

Experimentally we often find k>1,[226] *i.e.* the ERE is higher at higher excitation intensity. In this case the $V_{OC,in}$ at 1 sun would be even smaller, since equation (8) overestimates the $V_{OC,in}$ at 1 sun. But the trends we discuss between samples would remain the same. Thus, we consider a worst case scenario when it comes to determining the additional V_{OC} loss due to interface recombination.

***Experimental details of cathodoluminescence:**

The scanning electron micrographs and cathodoluminescence (CL) hyperspectral images were recorded using a Zeiss Merlin scanning electron microscope equipped with a DELMIC CL system at 10 keV beam energy and at beam currents of 500-700 pA. Fig. S3 shows the CL images obtained on the cross-section of untreated and TU-PDT sample. Both samples show rather low CL intensity. No difference in grain boundary activity was observed.

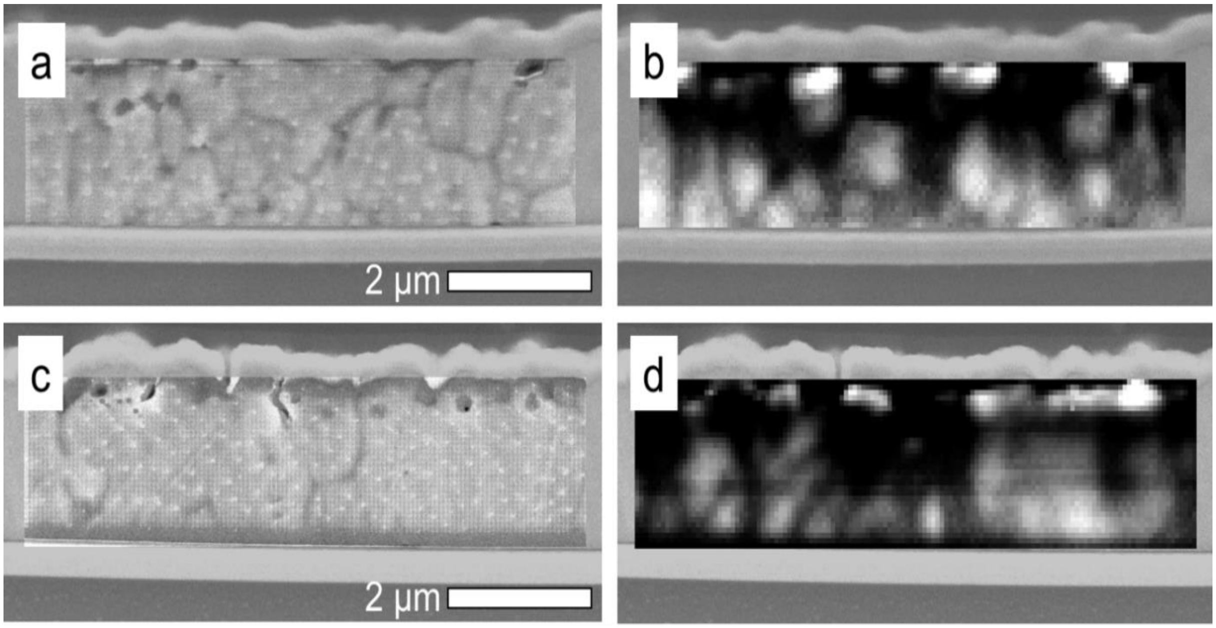


Figure A5.7: *SEM images (a, c) and panchromatic CL images (b,d) acquired on cross-section specimens from* $CuInS_2$ *solar cells with (a,b) and without TU treatment (c,d).*

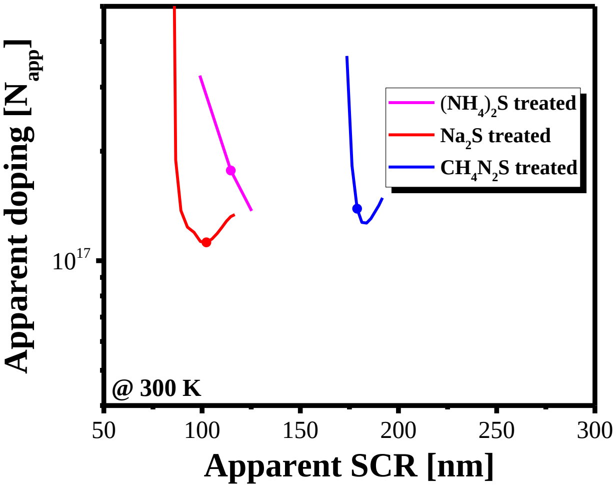


Figure A5.8: *Apparent doping profile versus apparent SCR width for S-PDT Cu-rich* $CuInS_2$ *device. The dot represents the equilibrium value (at 0.0V bias) of SCR width and apparent doping measured using the local derivative.*

**This part is directly taken from our published work [183]. I gratefully acknowledge Aleksandra Nikolaeva and Dr. Daniel Abou-Ras for performing the cathodoluminescence measurements providing the experimental details.*

***Surface analysis by X-ray photoelectron spectroscopy**

To check for the chemical impact of S-PDT on the absorber surface, X-ray photoelectron spectroscopy (XPS) was performed on the samples. For this, four pieces of 10 % KCN etched Cu-rich $CuInS_2$ absorbers from the same absorber deposition run were used. First piece was left untreated (ref), the second was treated AS-PDT (sample ‘1’), the third one with TU-PDT (sample ‘2’) and the last one with NaS-PDT, which delaminated and was not analyzed. All the three remaining pieces were then transferred with the water layer (comes from rinsing the absorber with DI water after KCN and the S-PDT) on top, into the glove box to avoid air exposure. From the glove box, they were then transferred via an N_2 filled cell into the XPS chamber for analysis. The entire procedure was designed to ensure minimum air exposure.

XPS experiments were carried out using a Kratos Axis Ultra DLD instrument equipped with a monochromatic Al Kα source (1486.6 eV) working at 150W. The base pressure during the analyses was better than 5.10^{-9} mbar. The narrow scans for elemental quantification and chemical states investigations were recorded with an energy resolution of 0.6 eV. The samples were sputtered with monoatomic Ar^+ ions of low energy (500 V) to limit the preferential sputtering effects, for 180 s to remove the surface contaminants and for 1080 s to access the deeper composition. The data were processed with the CasaXPS software (v2.3.22) and the curve fitting obtained with 70 % Gaussian – 30 % Lorentzian lineshapes.

Figure S8 (a) shows the S 2p bulk spectra of the above-mentioned three samples. For the TU-PDT absorber, proper fitting of ‘S’ spectrum required fitting with two doublets. The two peaks result from the S $2p_{3/2}$ and S $2p_{1/2}$ spin-orbit split: the first doublet corresponds to $CuInS_2$, which is present in spectra of all samples, and an additional doublet with peaks at 164.2-165.1 eV to account for a bump at higher binding energy that could be signature of C-S-C. [240-242] Simultaneously TU-PDT sample also has a significant amount of N present on the surface, which is absent in the other two samples. Analysis of N 1s bulk spectra shows a peak at 399.3 eV, which corresponds to C-NH2. [243] These results suggest the presence of an additional phase of S and an organic component containing C-NH2. At the surface, from the elemental quantification, amino groups are present in 3.5 at % concentration, which implies the presence of 1.75 at % of TU. Further, from the S2p spectrum, the organic component (S2p-2) represents only 1.1 at % of the total composition (6.6 % of the total sulfur area, and S being 16 at % of the total composition). This suggests that not all the amino groups are present in the form of TU or in the organic sulfur phase. Rather a portion of TU has partially reacted, leaving the amino group behind at the surface. Thus, the results indicate that a part of TU has reacted with the surface (physisorption of TU particular S), and the other part of TU is still present at the surface in the form of fragments. Additionally, table S3 represents the [Cu]/[In] ratio obtained using Cu 3p, Cu 2p, In 3d and In 4d lines. With the analysis depth for the different lines (in a CuInS2 matrix): Cu 3p = 7.9 nm; Cu 2p = 4.2 nm; In 3d = 6.25 nm; and In 4d; 8.2nm (calculated from the TTP2M formula). [191] Unlike the other two samples, the [Cu]/[In] ratio changes dramatically with the use of different element lines. Thus, indicating the presence of a thin layer on top, as this overlayer influences the analysis depth of each element. Therefore, XPS analysis concludes the formation of an organic overlayer on the absorber surface after TU-PDT.

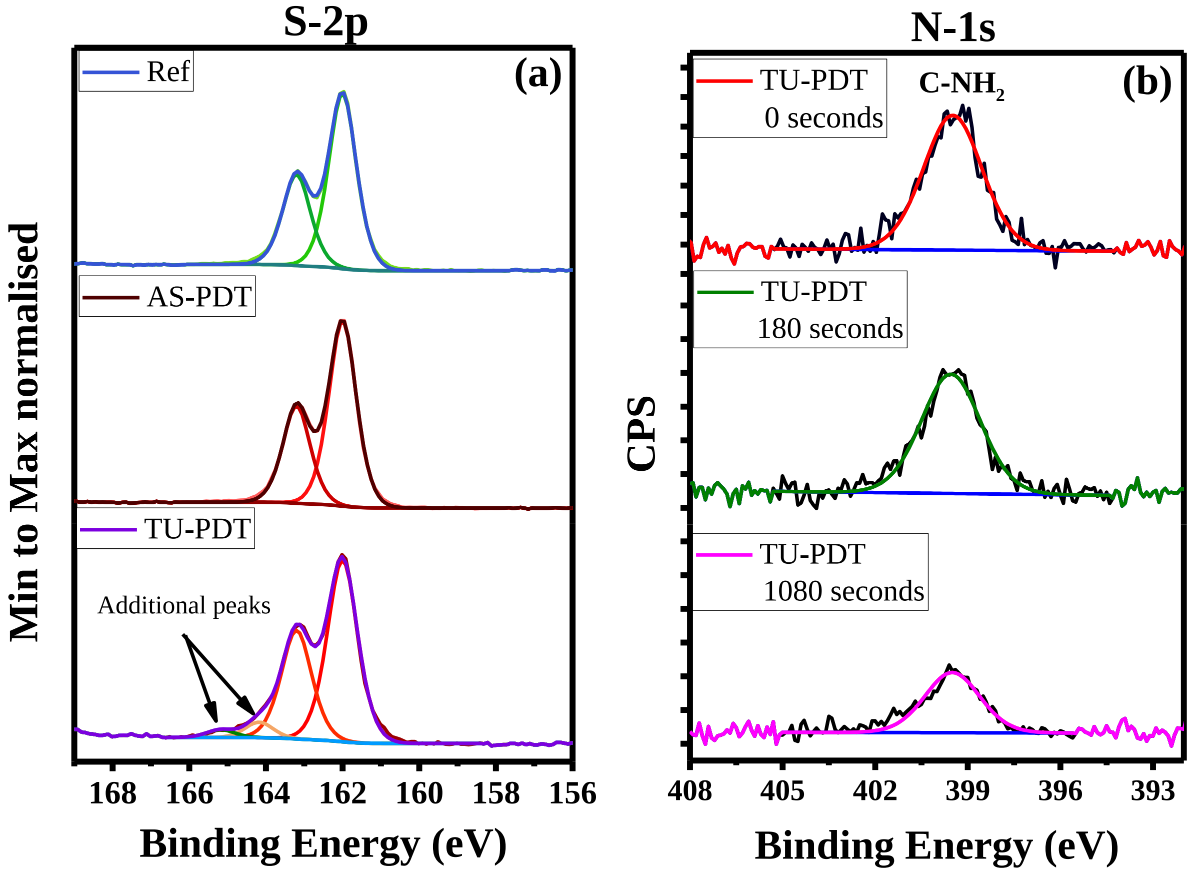


Figure 5.9: *(a) S-2p core level spectrum acquired for untreated, AS-PDT and TU-PDT absorbers, the spectrum is acquired in each case without any sputtering. (b) N-1s core level spectrum of TU-PDT absorber with three different etching times 0 second, 180 seconds and 1080 seconds to acquire information at different depths.*

**This part is directly taken from our published work [183]. I gratefully acknowledge Jérôme GUILLOT for performing XPS and analyzing the data for the samples.*

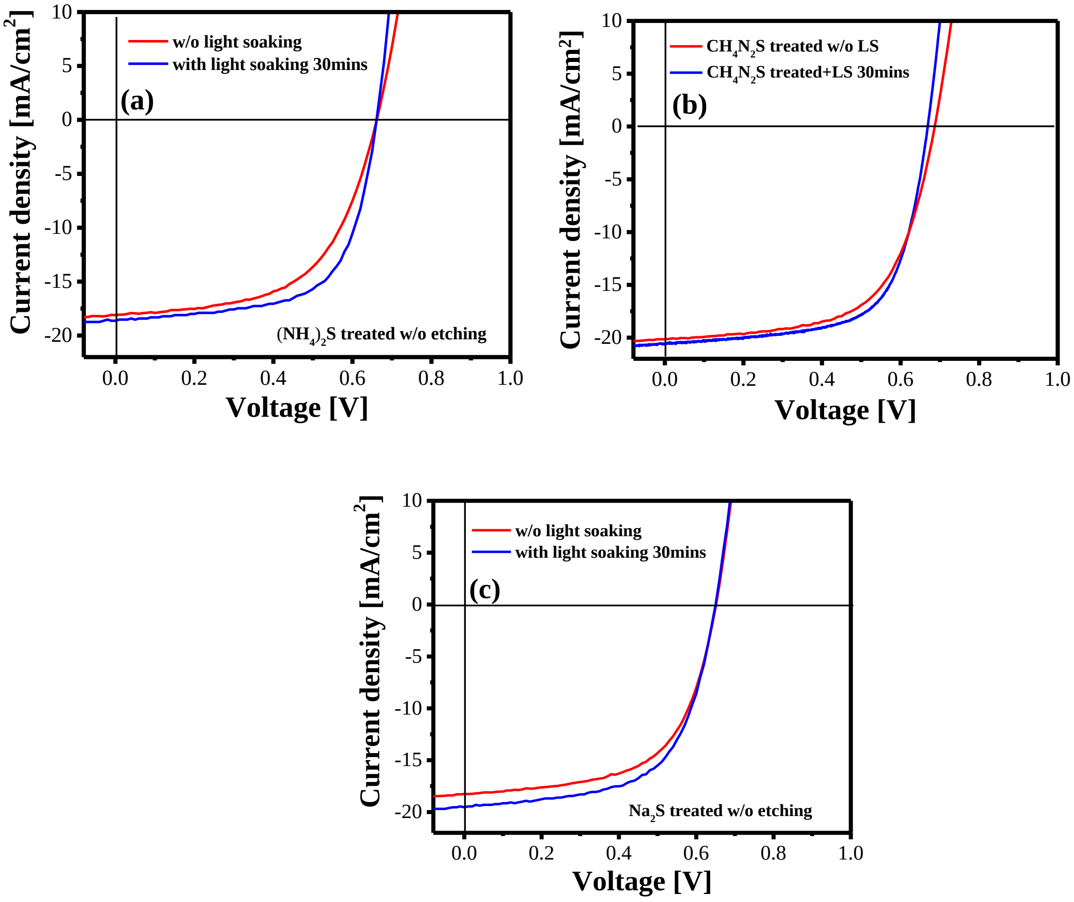


Figure A5.10: *I-V curves of (a) AS-PDT (b) TU-PDT and (c) NaS-PDT Cu-rich* $CuInS_2$ *device prepared without the second KCN etching step. A FF improvement is visible in all the devices after light soaking (LS).*

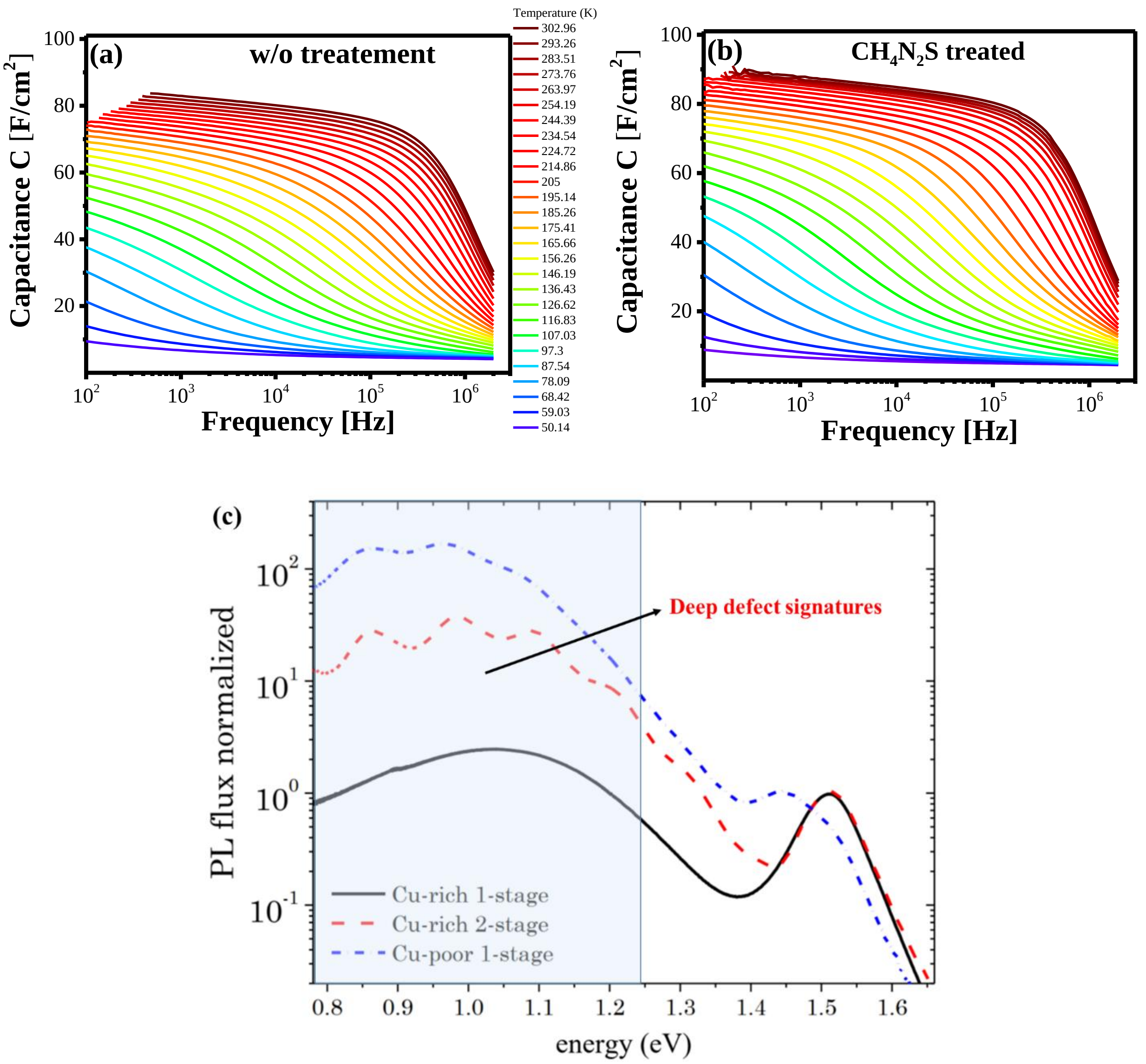


Figure A5.11: *Exemplary admittance spectra of 2-stage Cu-rich $CuInS_2$ device (a) without any post-deposition treatment (b) with CH_4N_2S post-deposition treatment. Both spectra possess almost identical capacitance steps with almost similar activation energy ~ 60 meV of the capacitance step extracted from the Arrhenius plot. (c) Deep defect signature in PL for $CuInS_2$ absorbers adapted from[26].*

***Transient capacitance measurements**

The procedure to measure the capacitance transients is as follows: first, the sample is kept under illumination with certain intensity for 300 seconds starting from t = -300 seconds. Since the LCR meter has an internal resistance of about 100 ohm, and this resistance under illumination puts the device in a certain forward-biased state, to keep the device under short-circuit conditions, a reverse bias voltage is applied to compensate for the photo-voltage from t = -300 seconds to 0 seconds, *i.e.* for the whole illumination period. This was done by measuring the DC voltage generated across the device due illumination, using the LCR meter. Thereafter, a voltage exactly opposite to this measured voltage is applied when the device is under illumination to keep the device under short-circuit condition. During the entire measurement procedure the voltage is monitored to make sure the device is always under short-circuit conditions. After this first step of 300 seconds, the illumination intensity is then set to zero at t=0 sec and the capacitance transient is measured for at least 300 seconds more. Note, no bias was applied on the sample during this second step, *i.e.* for t $\geq$ 0 seconds. Fig. A5.12 shows the evolution of space charge region width with time in three samples: untreated, TU-PDT and TU-PDT followed by KCN etching.

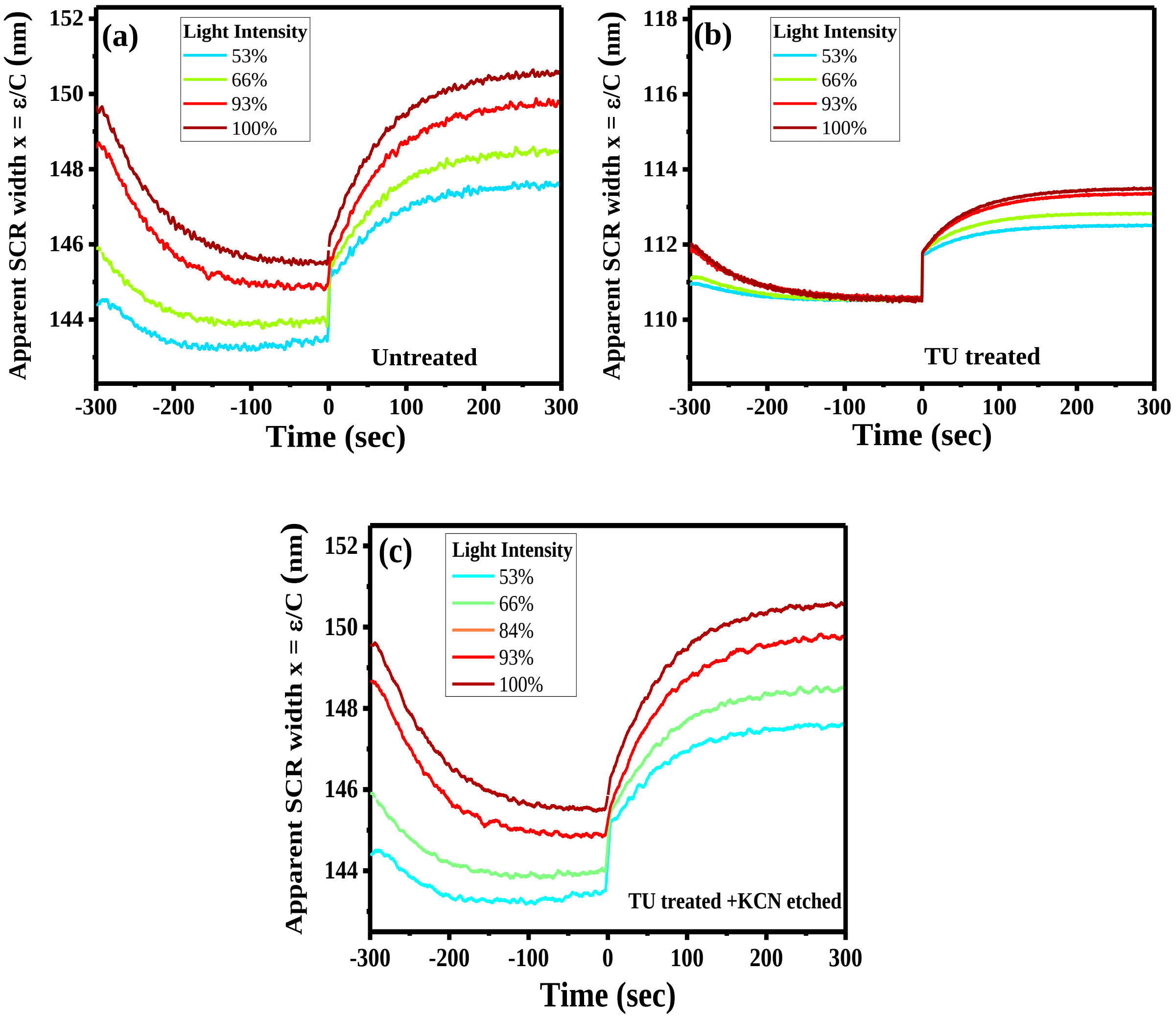


Figure A5.12. *Evolution of apparent SCR width as a function of time for (a) untreated sample (b) TU-PDT treated (c) TU-PDT +KCN etched device; measurements were done keeping the device under illumination for 300seconds and subsequently under dark for 300seconds. Always keeping the device in short-circuit condition: 100 % light intensity is equivalent to 1 sun intensity*

**This part is directly taken as a whole from the published work [183].*

Appendix Chapter 6

**This results are taken from our published work [174, 183].*

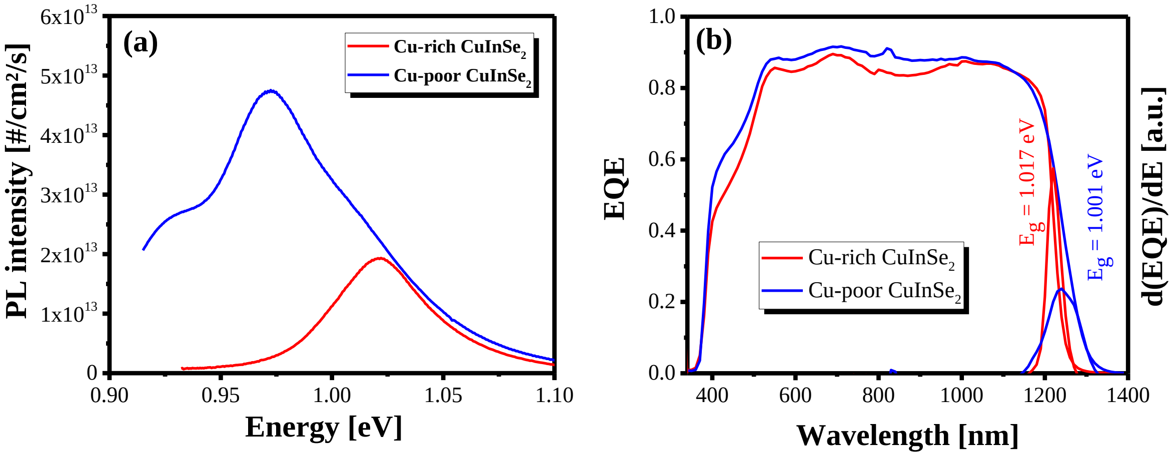


Figure A6.1: *(a) Exemplary measured calibrated PL spectra of Cu-rich and Cu-poor CuInSe₂ absorbers covered with CdS buffer layer. (b) Measured external quantum efficiencies of CuInSe₂ devices prepared with Cu-poor and Cu-rich as grown absorbers.*

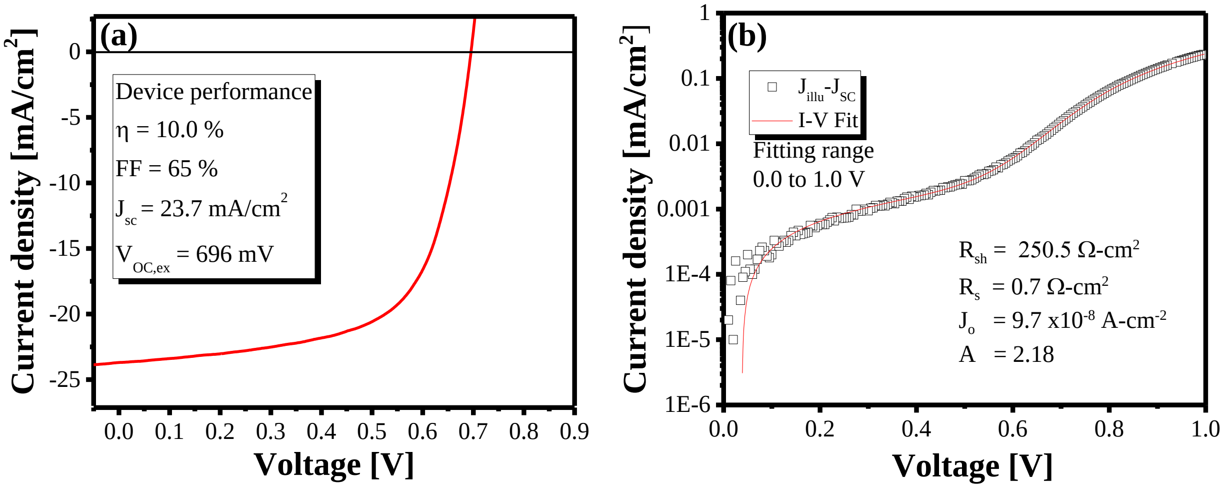


Figure A6.2: *I-V curve of the best CuInS₂ device prepared with Zn(O,S) in this thesis (a) and the I-V fit of the corresponding curve (b). The fit was made on the illuminated curve by shifting it by J_{SC} using the I-V fit routine as explained in section 2.1.2.*

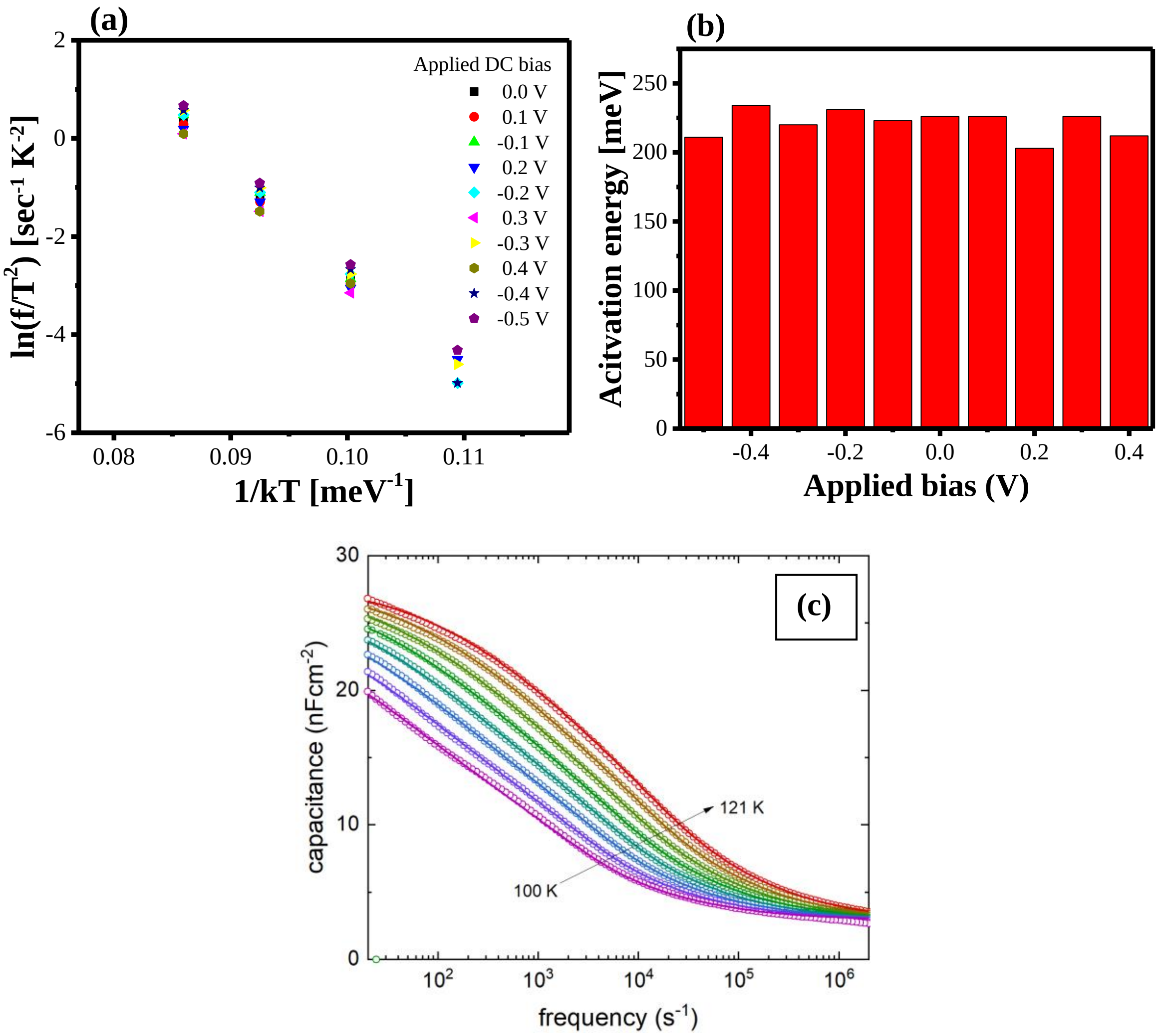


Figure A6.3: *(a) Arrhenius plot corresponding to the admittance spectra of a Cu-rich CuInSe$_2$ device measured at different DC voltage bias. (b) The activation energy obtained from the slope of data form Arrhenius plot. The activation energy is almost the same with different bias. (c) Experimental data (open symbols) and the corresponding fit (solid lines) for the double capacitance step of the sample shown in Fig. 6.4d.*

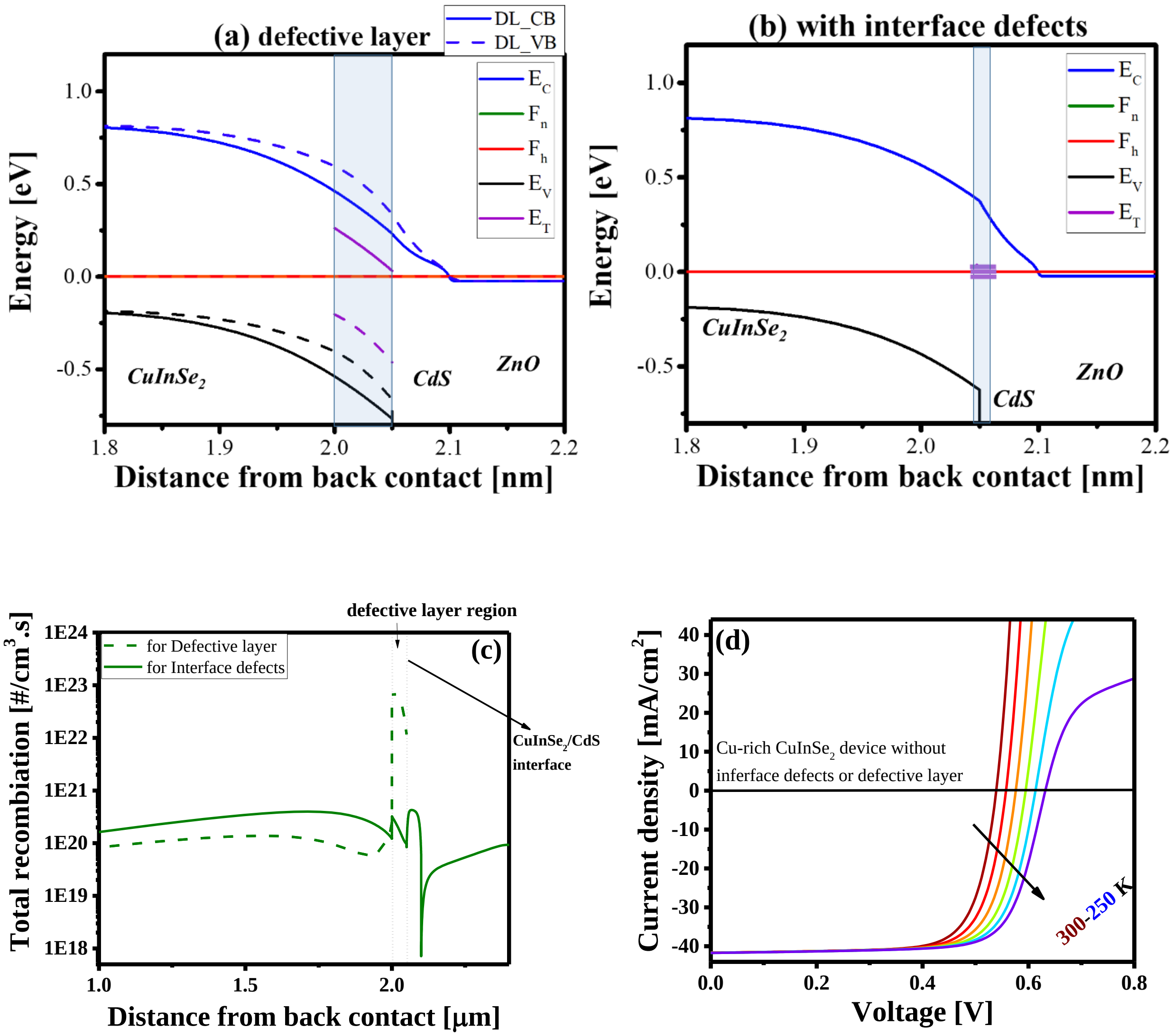
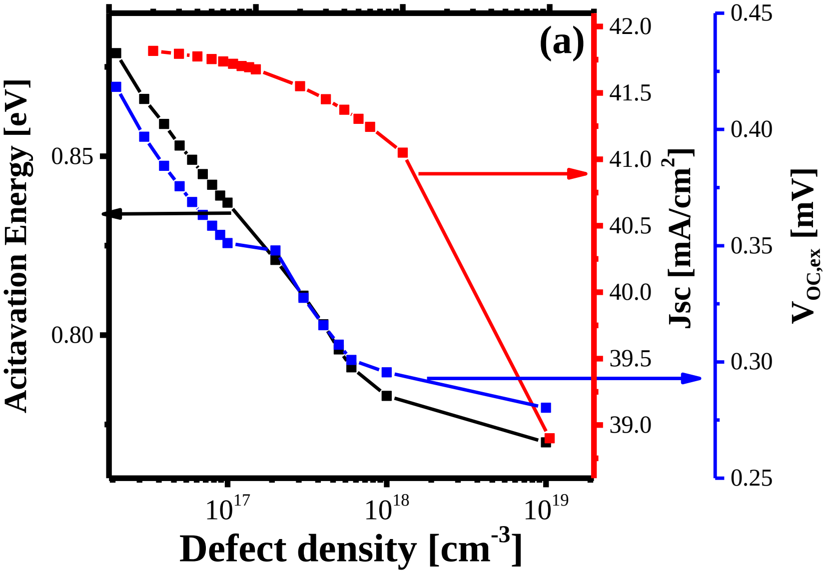


Figure A6.4: *Simulated band diagram of the device at equilibrium with (a) defective layer and (b) interface defects. In yellow the defect position is shown. (c) Recombination profiles as a function of distance from the back contact at* $V_{OC,ex}$ *for simulated devices with a defective layer and with interface defects. For the defective layer model (dashed line) dominant recombination appear to occur near the surface of the absorber, whereas in defective interface model (solid line) they occur at the interface. (d) Simulated I-V curve of a reference device with no defective layer or defective interface. The curves show 'S shape' in first quadrant at lower temperatures.*

Table A6.1. *SCAPS material parameters used to simulate $CuInSe_2$ device in section 6.3 in this manuscript. For achieving a value of $V_{OC,in}$ comparable to as observed in optical measurements, a deep defect level at 300 meV is introduced in the $CuInSe_2$ absorber layer.*

Parameter	**$CuInSe_2$**	**p^+ $CuInSe_2$**	**CdS**	**ZnO/AZO**	**IF defects $CuInSe_2$/CdS**
Thickness (µm)	2.5	0.050	0.050	0.350	-
Band gap(eV)	1.0	1.0	2.40	3.45	-
Dielectric permittivity (relative)	13.6	13.6	10	10	
Electron affinity(eV)	4.6	4.6	4.6	4.6	-
Electron mobility(cm^2/Vs)	20	20	50	50	-
Hole mobility(cm^2/Vs)	10	10	20	20	-
Doping($1/cm^3$)	$1x10^{16}$	$1x10^{16}$	$1x10^{16-17}$	$1x10^{17-19}$	-
Defect density($1/cm^3$) **Single acceptor** **from $CuInSe_2$ VB**	$1x10^{16}$ 300meV	$1x10^{16}$ 300meV & $5x10^{16}$ 220meV	-	-	$1x10^{12}$ **cm^{-2}** 650meV
Capture cross-section electrons (cm^{-2})	$1x10^{-15}$	$1x10^{-12}$ for 220meV	-	-	$1x10^{-12}$
Capture cross-section holes (cm^{-2})	$1x10^{-15}$	$1x10^{-13}$ for 220meV	-	-	$3x10^{-16}$



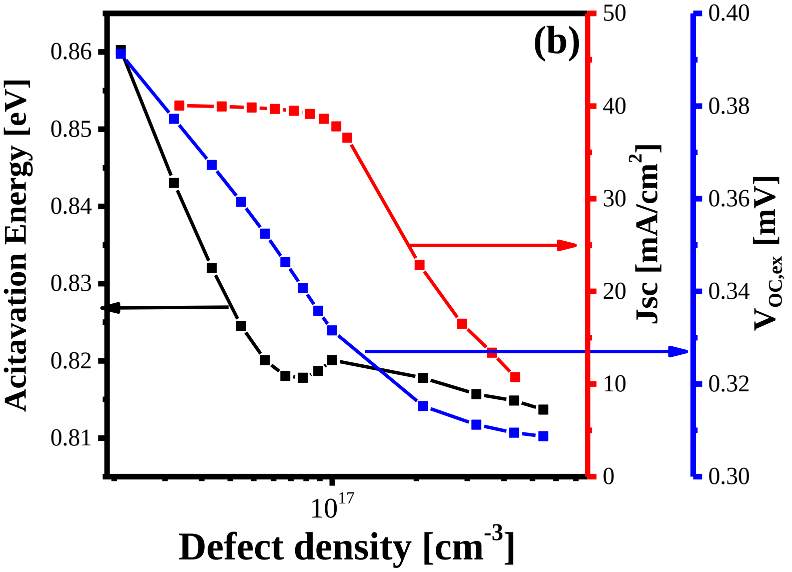


Figure A6.5: *Activation energy (E_a), short-circuit current density (J_{SC}) and external open-circuit voltage ($V_{OC,ex}$) as a function of defect density in the defective layer (a) for the device with the defect placed 220 meV away from CBM (b) for the device with the defect placed 220 meV away from VBM.*

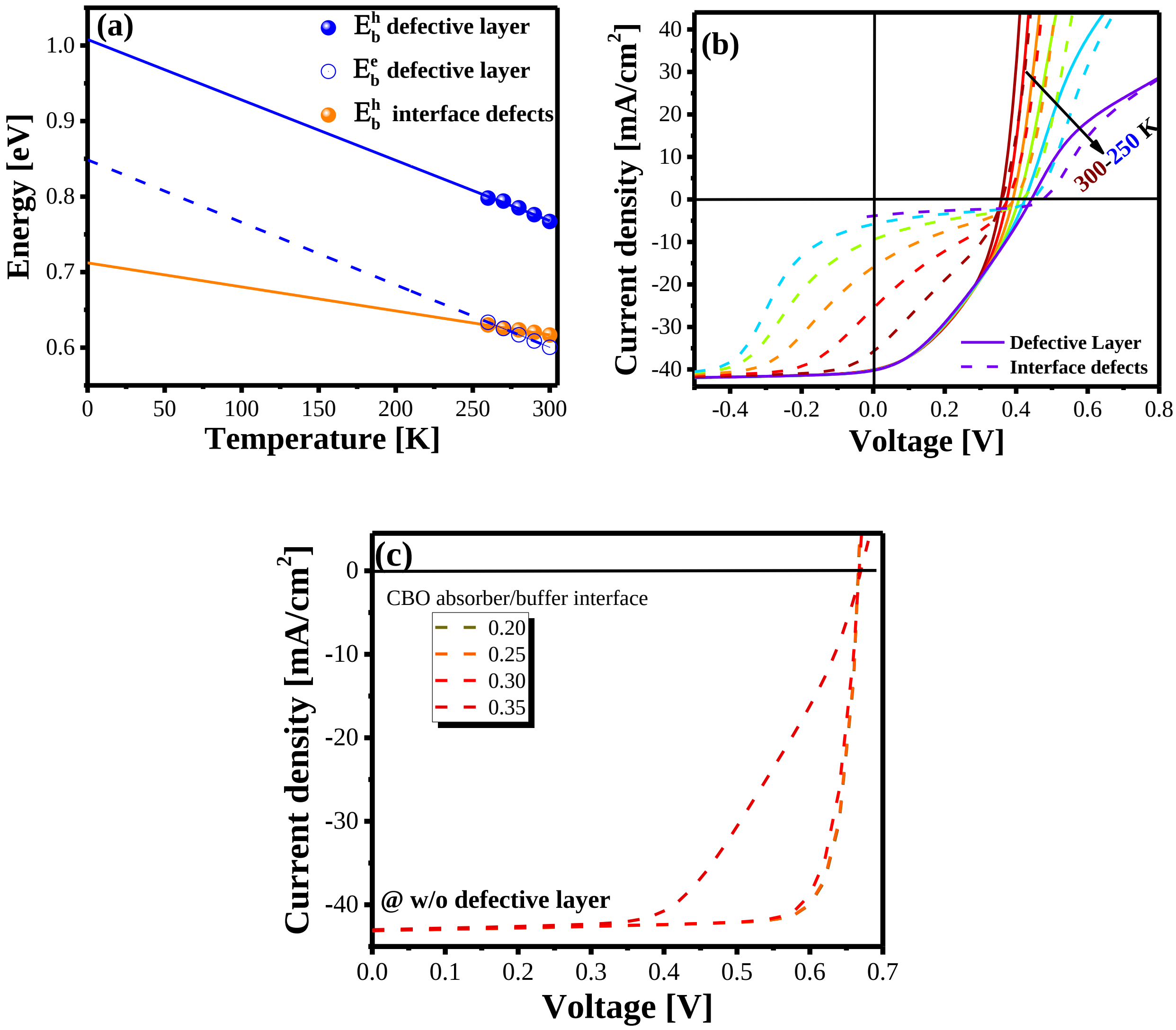


Figure A6.6: *(a) The electron and hole barrier as the function of temperature and its extrapolation to 0 K for DL_VB and interface defects model. (b) Simulated I-V curve at different temperatures of devices with DL_VB and with a defective interface. The former results in 'S shape' in first quadrant (solid lines), whereas later results in 'S shape' in third and fourth quadrant (dashed lines). (c) Simulated I-V curve of a reference device with different CBO at the absorber/buffer interface with no defective layer.*

DLTS measurement of CuInS$_2$ devices

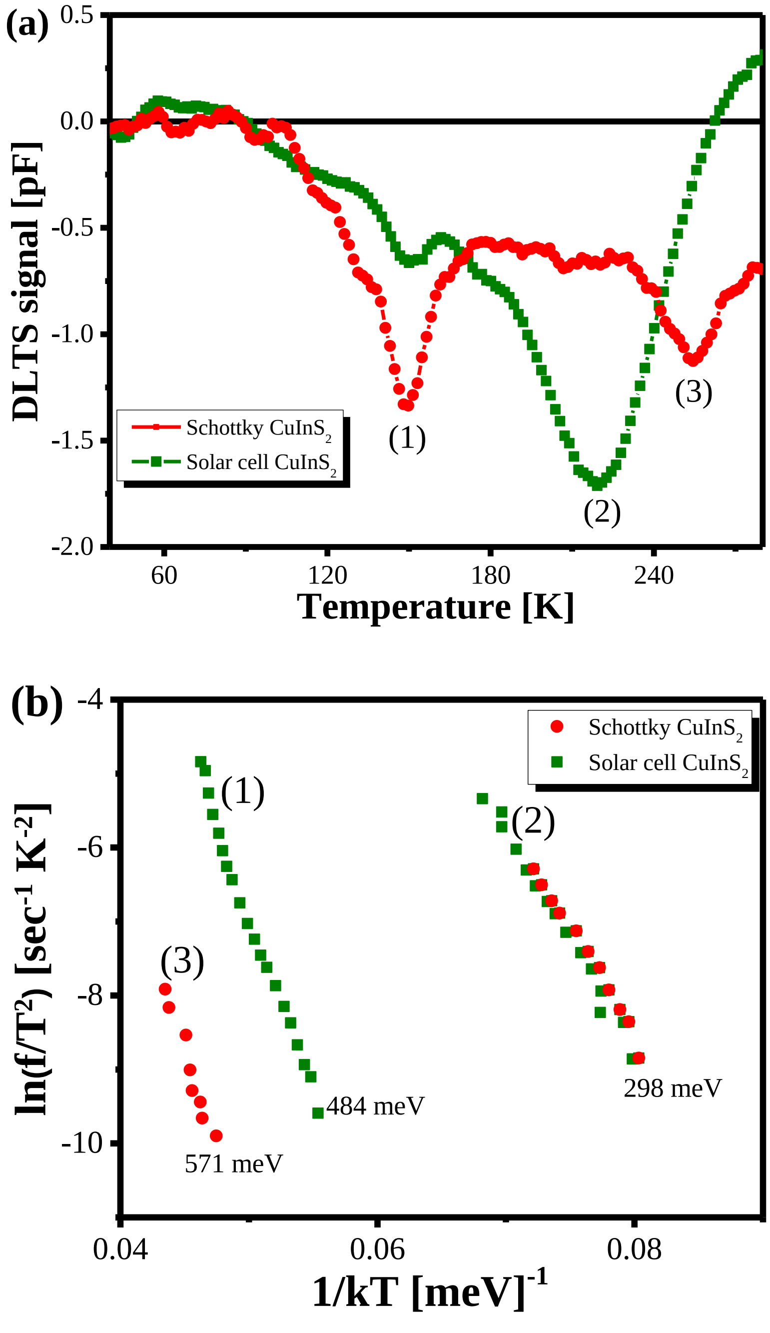


Figure A6.7: *(a) DLTS signals of the KCN etched CuInS$_2$ schottky junction device (red) and solar cell (olive) and (b) the corresponding Arrhenius plot.*

Table A6.2. *SCAPS material parameters used to simulate* $CuInS_2$ *device in section 6.3 in this manuscript. For achieving a value of* $V_{OC,in}$ *comparable to as observed in optical measurements, a deep defect level at 700 meV is introduced in the* $CuInS_2$ *absorber layer.*

Parameter	**$CuInS_2$**	**p^+ $CuInS_2$**	**Zn(O,S)**	**ZnO/AZO**	**IF defects $CuInSe_2$/CdS**
Thickness (µm)	2.5	0.050	0.050	0.350	-
Band gap(eV)	1.5	1.5	3.3	3.45	-
Dielectric permittivity (relative)	13.6	13.6	10	10	
Electron affinity(eV)	4.6	4.6	4.6	4.6	-
Electron mobility(cm^2/Vs)	20	20	50	50	-
Hole mobility(cm^2/Vs)	10	10	20	20	-
Doping($1/cm^3$)	$1x10^{16}$	$1x10^{16}$	$1x10^{17}$	$1x10^{17-19}$	-
Defect density($1/cm^3$) **Single acceptor** **from $CuInS_2$ valence band**	$5x10^{16}$ 700meV	$5x10^{16}$ 700meV & $1x10^{17}$ 1200 meV	-	-	$1x10^{11}$ **cm^{-2}** 800 meV
Capture cross-section electrons (cm^{-2})	$1x10^{-14}$	$1x10^{-12}$ for 1200 meV	-	-	$1x10^{-15}$
Capture cross-section holes (cm^{-2})	$1x10^{-14}$	$1x10^{-13}$ for 1200 meV	-	-	$3x10^{-15}$

List of Publications and Conferences

Publications

First author

(1) Sood, M.; Elanzeery, H.; Adeleye, D.; Lomuscio, A.; Werner, F.; Ehre, F.; Melchiorre, M.; Siebentritt, S. Absorber composition: "A critical parameter for the effectiveness of heat treatments in chalcopyrite solar cells." *Prog. Photovolt.* **2020**.

(2) Sood, M.; Lomuscio, A.; Werner, F.; Nikolaeva, A.; Dale, P. J.; Melchiorre, M.; Guillot, J.; Abou-Ras, D.; Siebentritt, S. "Passivating Surface Defects and Reducing Interface Recombination in $CuInS_2$ Solar Cells by a Facile Solution Treatment." *Sol. RRL.* **2021,** *5* (4), 2100078.

(3) *Shukla, S.; *Sood, M; Adeleye, D.; Peedle, S.; Kusch, G.; Dahliah, D.; Melchiorre, M.; Rignanese, G.-M.; Hautier, G.; Oliver, R.; Siebentritt, S. Over 15% efficient wide-band-gap $Cu(In,Ga)S_2$ solar cell: Suppressing bulk and interface recombination through composition engineering. *Joule* **2021**. (***equal contribution**)

(4) Sood, M; Urbaniak, A.;, Boumenou, K.C.; Elanzeery, H.; Babbe. F.; Werner, F.; Melchiorre, M.; Redinger, A.; Siebentritt, S. "Near surface defects: Cause of deficit between internal and external open-circuit voltage in solar cells." accepted in *Prog. Photovolt.* **2021**.

(5) Sood, M, Bombsch, J.; Shukla, S.; Lomuscio, A.; Hartmann, C.; Frisch, J.; Bremsteller, W.; Ueda, S.; Wilks, R.G.; Bär, M.; Siebentritt, S. "Origin of interface limitation in $CuInS_2$ - based solar cells." *under review* **2021**.

(6) Sood, M.; Gnanasambandan, P.; Adeleye, D.; Shukla, S.; Adjeroud, N; Leturcq, R.; Siebentritt, S. "Electrical barriers and their elimination by fine-tuning ZnMgO composition in $Cu(In,Ga)S_2$: Systematic approach to achieve over 14% efficiency." *under review* **2021**.

Co-author

(7) Elanzeery, H.; Melchiorre, M.; Sood, M.; Babbe, F.; Werner, F.; Brammertz, G.; Siebentritt, S. "Challenge in Cu-rich $CuInSe_2$ thin film solar cells: Defect caused by etching." *Phys. Rev. Mater.* **2019,** *3* (5), 055403, DOI: 10.1103/PhysRevMaterials.3.055403.

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Conference contribution

Oral presentation

(1) Sood, M; Elanzeery, H.; Lomuscio, A.; Werner, F.; Melchiorre, M.; Siebentritt, S. "Impact of Heat Treatment on Cu-rich and Cu-poor $\mathrm{CuInS(e)_2}$ with CdS and ZnOS Buffer Layer" ICMAT, Singapore, 2019.

(2) Sood, M; Shukla, S.; Adeleye, D.; Melchiorre, M.; Siebentritt, S. "Towards 1V Open-Circuit Voltage and Beyond—Reducing Bulk and Interface Losses in Wide Bandgap Chalcopyrite $\mathrm{CuInGaS_2}$ Solar Cell" MRS Spring Meeting and Exhibit, Virtual, 2021.

Poster presentation

(1) Sood, M.; Lomuscio, A.; Melchiorre, M.; Siebentritt, S. "Optimizing buffer layers for reduced interface recombination in $\mathrm{CuInS_2}$ solar cell" MASSENA Business day, Luxembourg, 2018.

(2) Sood, M; Urbaniak, A.; Boumenou, K.C.; Elanzeery, H.; Babbe. F.; Werner, F.; Melchiorre, M.; Redinger, A.; Siebentritt, S. "Sub-surface defects in solar cells: An alternate cause of interface V_{OC} deficit", E-MRS Spring Meeting, Virtual, 2021.

(3) Sood, M.; Gnanasambandan, P.; Adeleye, D.; Shukla, S.; Adjeroud, N; Leturcq, R.; Siebentritt, S. "Electrical barriers and their elimination by fine-tuning ZnMgO composition in $\mathrm{Cu(In,Ga)S_2}$: Systematic approach to achieve over 14% efficiency." MASSENAYSC2021, Luxembourg, 2021.

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