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by

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STRUCTURATION OF PIEZOTRONIC JUNCTIONS FOR
ULTRASENSITIVE STRAIN SENSORS

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Acknowledgments

A wise man once said:
*“Never stop never stopping.
They see me rollin’, they hatin’.”*

Oh boy. Here we are. What a journey it has been. I will try my best to save the semi-inspirational quotes for another day and speak with my heart.

To yourself (technically myself), Dr. Raoul Joly, congratulations, you did it. I hope these lines find you well. If you are reading this in the future, well, it means that you are alive. Obviously. Congratulations again. Maybe you became a quantum human and you are both dead and alive simultaneously! That would be dope. Or maybe you are reading it in the past because you invented time travel. Smart. Or else... Maybe you took the red pill and got freed from the Matrix. Wise choice. Or maybe you’re reading this on Mars because you lost your job due to AI robots with Elon Musk now ruling over... Enough.

Anyway, I hope you are reading this manuscript with a beautiful Japanese wife and a bunch of kids (Raoul Junior? Just an idea, save it for later) ~~in your basement~~ running around your mansion, because yeah, obviously; you are rich, at least in one of the many parallel worlds of the multiverse. Did you keep working in the science/research field (ALD, anyone)? Are you laying down on a beach while mining bitcoins, or the next hot cryptocurrency in Barcelona? Or did you pursue your everlasting dream of becoming a professional tennis player (it’s too late, time to move on dude...)? Are you still listening to Led Zeppelin, Pink Floyd and Radiohead? Did the movie Dune (you watched it yesterday at the time you’re writing, remember) live up to expectations and became the new big sci-fi saga of our era? So many questions. But you know what? It doesn’t matter. I just hope that you feel happy, fulfilled and that you are still as lucky as you’ve always been.

On a more serious tone, this manuscript is the result of a multidisciplinary work, at the interface between different fields within materials science and engineering, where many skilled and talented individuals were involved along the four years span of this PhD project. Even if these words cannot compensate for all the sweat and efforts spent in the cleanroom, in the labs, or behind the computer screens, the least I can do is to take the following lines to acknowledge and emphasize the professional and personal contributions made to this work.

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Raoul Joly,
Luxembourg, September 2021.

Abstract

The piezotronic effect relies on the creation of piezoelectric polarization charges mechanically induced within a piezoelectric semiconductor to modulate the carrier dynamics across electronic contact interfaces. The field of piezotronics is a relatively new area of study, based on a mechanical signal triggering, which is one of the most common kind of interactions between the environment and electronic systems. It started to draw a considerable attention in the early 2010's, by reaching higher electromechanical sensitivities when compared to conventional methods of sensing.

The rapidly spreading Internet-of-Things is accelerating Micro-ElectroMechanical Systems (MEMS) industry to deliver highly sensitive and miniaturized self-sensing sensors with low power consumption and cost-effective production process. Within this context, strain sensors based on the piezotronic effect appear as promising candidates to address these needs. However, several crucial questions remain unanswered or need to be refined, concerning the design and integration of piezotronic junctions with its fabrication process into microsystems or MEMS, the optimal configuration for strain sensing as well as noise studies for such systems.

This PhD thesis proposes to rationalize the piezotronic effect for strain sensors and presents a novel microfabrication process integrating for the first time piezotronic strain sensors in millimetre-sized cantilevers on flexible polymeric substrates by means of maskless laser lithography. The atomic layer deposition (ALD) technique was used for the deposition of ZnO polycrystalline thin films on high work function metals to obtain Schottky junctions. However, such ZnO-based Schottky junctions by ALD have never been post-processed and integrated into a strain sensor. We propose to rationalize the ALD processing to obtain wurtzite polycrystalline zinc oxide thin films with a privileged (002) orientation and to make it compatible with microfabrication processing on polymer.

The difficulties linked with the integration of inorganic thin films onto a polymeric substrate within the developed microfabrication process will be highlighted. We propose appropriate adjustments of the sensor's design and the process flow. Pt/ZnO/Pt back-to-back Schottky diode junctions have been shaped in interdigitated microelectrodes to get piezotronic strain sensing on the clamp area of the cantilever structure. The conduction mechanisms occurring within the piezotronic strain microsensors have been thoroughly studied, based on the thermionic emission model. The developed electrical model will be detailed, emphasizing the presence of interface trap states and their prominent impact on the electrical characteristics. The piezotronic strain sensors' transducing properties will be detailed as well by the mean of force spectroscopy, leading to the expected Schottky barrier height modulation by the piezotronic effect. Furthermore, we investigated for the first time the noise figure of within strain sensors based on the piezotronic effect. These new insights about noise amplitudes and origins are promising matter of optimization to improve the signal-to-noise ratio of the sensor.

Within the last section of this work, we will detail the piezotronic strain sensors size miniaturization for integration in microcantilevers in a full-SU8 body. The miniaturization of our strain sensors makes them more prone for AFM (Atomic Force Microscopy) scanning probe operations on commercial machines, with the aim of greatly improving the sensitivity to small mechanical deformations. The approach taken for the microfabrication of these miniaturized sensors is based on a reversed processing by the mean of a sacrificial layer. This raised new difficulties in terms of metal adhesion and electrical contact continuity, which will be reported.

The results obtained are highly promising and pave the way towards the processing of ultrasensitive strain microsensors on MEMS structures, as well as their great potential for AFM scanning probe operations.

Résumé

L'effet piézolectronique repose sur la création de charges de polarisation piézoélectriques d'origine mécanique induites au sein d'un semiconducteur piézoélectrique, afin de moduler la dynamique des porteurs de charges au travers d'interfaces de contact électroniques. Le domaine des dispositifs piézolectroniques est un champ d'études relativement nouveau, basé sur un signal de déclenchement mécanique, représentant l'une des interactions les plus fréquentes entre l'environnement et les systèmes électroniques. Ce domaine d'études a commencé à attirer une attention considérable au début des années 2010, en atteignant des sensibilités électromécaniques supérieures en comparaison aux méthodes de détection conventionnelles.

La propagation rapide de l'Internet-of-Things a accéléré l'industrie des Micro-ElectroMechanical Systems (MEMS) à délivrer des capteurs ultra-sensibles, miniaturisés, à détection intégrée, présentant une faible consommation énergétique ainsi qu'un procédé rentable de production. Dans ce contexte, les capteurs de déformation basés sur l'effet piézolectronique apparaissent comme des candidats prometteurs afin de répondre à ces besoins. Cependant, de nombreuses questions cruciales demeurent sans réponse ou doivent être affinées, concernant le design et l'intégration de jonctions piézolectroniques avec leurs procédés de fabrication au sein de microsystèmes ou de MEMS, la configuration optimale pour la détection de déformation ainsi que les études de bruit pour de tels systèmes.

Ce projet de thèse propose de rationaliser l'effet piézolectronique appliqué aux capteurs de déformation et présente un nouveau procédé de microfabrication intégrant pour la première fois des capteurs de déformation piézolectroniques dans des leviers millimétriques sur des substrats flexibles polymériques, au moyen de lithographie laser sans masque. Le procédé d'atomic layer deposition (ALD) a été utilisé pour la déposition de couches minces polycristallines de ZnO sur des métaux à haut travail de sortie afin

d'obtenir des jonctions de Schottky. Cependant, de telles jonctions de Schottky basées sur de l'oxyde de zinc déposé par ALD n'ont jamais été post-traitées et intégrées au sein d'un capteur de déformation. Nous proposons de rationaliser le procédé ALD dans l'optique d'obtenir des couches minces polycristallines de ZnO présentant une structure de type wurtzite avec une orientation cristalline préférentielle (002), en rendant leur déposition compatible avec des procédés de microfabrication sur substrats polymériques.

Les difficultés associées à l'intégration de couches minces inorganiques sur un substrat polymérique au sein du procédé de microfabrication développé seront mises en évidence. Nous proposons dans ce sens des ajustements appropriés vis-à-vis du design et du procédé de microfabrication des capteurs de déformation. Des jonctions de diode Schottky Pt/ZnO/Pt montées en opposition ont été structurées en microélectrodes interdigitées afin d'obtenir une détection de déformation via l'effet piézolectronique à l'encastrement de la structure en levier. Les mécanismes de conduction existants au sein des micro-capteurs de déformation piézolectroniques ont fait l'objet d'une étude approfondie sur la base du modèle d'émission thermoionique. Le modèle électrique développé sera détaillé, soulignant la présence d'états d'interface ainsi que leur impact prédominant sur les caractéristiques électriques. Les propriétés de transduction des capteurs de déformation piézolectroniques seront également détaillées par le biais de mesures de spectroscopie de force, menant à la modulation de la hauteur de la barrière de Schottky attendue par l'effet piézolectronique. En outre, nous avons mesuré pour la première fois le facteur de bruit au sein de capteurs de déformation basés sur l'effet piézolectronique. Ces nouveaux éclairages concernant l'amplitude et l'origine du bruit dans de tels systèmes sont prometteurs afin d'améliorer le rapport signal sur bruit des capteurs développés.

La dernière section de ce projet de thèse détaillera la miniaturisation des capteurs de déformation piézolectroniques pour leur intégration au sein de microleviers dans un corps consistant entièrement de résine SU8. La miniaturisation des capteurs de déformation les rend plus enclins aux mesures AFM (Atomic Force Microscopy) en tant que sondes de balayage sur des machines commerciales, dans l'optique d'améliorer considérablement la sensibilité aux faibles déformations mécaniques. L'approche adoptée pour la microfabrication de ces capteurs miniaturisés est basée sur un

processus inversé par le biais d'une couche sacrificielle. Cette méthode inversée a soulevé de nouvelles difficultés en termes d'adhésion des contacts métalliques ainsi qu'au niveau de la continuité des contacts électriques, qui seront reportées.

Les résultats obtenus sont très prometteurs et ouvrent la voie vers la fabrication de micro-capteurs ultra-sensibles intégrés à des structures MEMS, et démontrent leur fort potentiel en tant que sondes de balayage par microscopie à force atomique.

Nomenclature

AFM:	Atomic Force Microscopy
Al ₂ O ₃ :	Aluminium Oxide
ALD:	Atomic Layer Deposition
ALE:	Atomic Layer Epitaxy
AlGaN:	Aluminium Gallium Nitride
AlN:	Aluminium Nitride
BF:	Bright Field
CAD:	Computer Aided Design
CdS:	Cadmium Sulfide
CMOS:	Complementary Metal Oxide Semiconductor
CTE:	Coefficient of Thermal Expansion
CuO:	Copper Oxide
CVD:	Chemical Vapor Deposition
DEZ:	DiEthylZinc
DF:	Dark Field
DI:	Delonized
DNA:	DeoxyriboNucleic Acid
EBME:	Electron Beam Metal Evaporation
EDS:	Energy Dispersive Spectroscopy
EELS:	Electron Energy Loss Spectroscopy
FE:	Field Emission
FeCl ₃ :	Iron Trichloride

FET:	Field Effect Transistor
FFT:	Fast Fourier Transform
GaN:	Gallium Nitride
GF:	Gauge Factor
GPC:	Growth Per Cycle
GI:	Grazing Incidence
HAADF:	High Angle Annular Dark Field
HRTEM:	High-Resolution Transmission Electron Microscopy
IDE:	InterDigitated Electrodes
InGaN:	Indium Gallium Nitride
InN:	Indium Nitride
IPA:	IsoPropyl Alcohol (Isopropanol)
LED:	Light Emitting Diode
MBE:	Molecular Beam Epitaxy
MEMS:	Micro ElectroMechanical Systems
MEZ:	MonoEthyl Zinc
MgO:	Magnesium Oxide
M-I-S:	Metal-Insulator-Semiconductor
ML:	Molecular Layering
MLA:	MaskLess Aligner
MOCVD:	Metal Organic Chemical Vapor Deposition
MOSFET:	Metal Oxide Semiconductor Field Effect Transistor
M-S:	Metal-Semiconductor
M-S-M:	Metal-Semiconductor-Metal
NC:	Negative Capacitance
NO ₂ :	Nitrogen Dioxide
NEMS:	Nano ElectroMechanical Systems
PCB:	Printed Circuit Board
PDMS:	PolyDiMethylSiloxane

PEALD:	Plasma Enhanced Atomic Layer Deposition
PET:	PolyEthylene Terephthalate
PFM:	Piezoelectric Force Microscopy
PGMEA:	Propylene Glycol Methyl Ether Acetate
PLD:	Pulsed Laser Deposition
PS:	PolyStyrene
RIE:	Reactive Ion Etching
SBH:	Schottky Barrier Height
SEM:	Scanning Electron Microscopy
SFM:	Scanning Force Microscopy
SLM:	Spatial Light Modulator
SNR:	Signal-to-Noise Ratio
STEM:	Scanning Transmission Electron Microscopy
TBE:	Top-Bottom Electrode
TE:	Thermionic Emission
TEM:	Transmission Electron Microscopy
TFE:	Thermionic-Field Emission
TLM:	Transmission Line Method
TMAH:	TetraMethylAmmonium Hydroxide
TNPT:	Twin NanoPlaTelet
UHV:	Ultra High Vacuum
XPS:	X-ray Photoelectron Spectroscopy
XRD:	X-Ray Diffraction
ZnO:	Zinc Oxide

List of Symbols

This section aims at summarizing the different physical parameters used in numerical applications with their corresponding units, as well as the constants' values.

Parameter	Description	Unit	Value (if constant)
A	Schottky contact area	m ²	/
A*	Richardson constant for n-type ZnO	A.m ⁻² .K ⁻²	32 A.cm ⁻² .K ⁻²
a	Lattice parameter from ZnO wurtzite structure	m	/
C _{it}	Interface trap states capacitance	F	/
C _m	Measured capacitance	F	/
C _{ox}	Oxide capacitance	F	/
C _p	Parallel capacitance	F	/
C _s	Schottky depletion capacitance	F	/
c	Lattice parameter from ZnO wurtzite structure	m	/
c ₀	Reference lattice parameter from ZnO wurtzite structure	m	5.211 Å
D _{it}	Interface trap states density	eV ⁻¹ .m ⁻²	/
d	Deflection	m	/
E ₀₀	Energy criterion	J	/
E _m	Maximum electric field	V.m ⁻¹	/
f	Frequency	Hz	/
G	Amplification	Ω	/
GF	Gauge factor	1	/
G _m	Measured conductance	S	/
G _p	Parallel conductance	S	/
h	Planck constant	J.s	6.62607004*10 ⁻³⁴
ħ	Reduced Planck constant	J.s	1.0546*10 ⁻³⁴
I	Current	A	/

I_0	Steady-state current for a given applied bias voltage	A	/
$I_{\text{cantilever}}$	Cantilever moment of inertia	kg.m ²	/
I_S	Saturation current	A	/
I_ϵ	Current for a given applied strain and bias voltage	A	/
k	Stiffness	N.m ⁻¹	/
k_B	Boltzmann constant	J.K ⁻¹	1.38064852*10 ⁻²³
L	Cantilever length	m	/
L_S	Sensor length	m	/
l_{if}	Length of an interdigitated finger	m	/
m_0	Free electron mass	kg	9.109*10 ⁻³¹
m^*	Effective electron mass for ZnO	kg	0.28*m ₀
N_C	Effective density of states in the conduction band	m ⁻³	/
N_D	Electron concentration	m ⁻³	/
n_{if}	Number of interdigitated fingers	1	/
P(dBm)	Power	dBm	/
P(W)	Power	W	/
q	Electron charge	C	1.60218*10 ⁻¹⁹
R_{line}	Line impedance	Ω	50
R_R	Resistance for a metal resistor	Ω	/
R_S	Series resistance	Ω	/
S	Noise spectral density	A ² .Hz ⁻¹	/
SNR	Signal-to-noise ratio	1	3
S_R	Noise spectral density for a metal resistor	A ² .Hz ⁻¹	/
S_{total}	Total noise spectral density	A ² .Hz ⁻¹	/
T	Temperature (taken as room temperature)	K	300
t	Cantilever thickness	m	/
t_{Pt}	Thickness of the Pt metal electrodes	m	/
t_s	Sensor thickness	m	/
V	Voltage	V	/
V_D	Built-in voltage	V	/
w	Cantilever width	m	/
Y	Young modulus	N.m ⁻²	/
α	Intrinsic barrier lowering coefficient	m	/
Δf	Resolution bandwidth of the oscilloscope	Hz	/

ΔI	Change in current under a given strain	A	/
ΔI_{\min}	Minimal current change detectable by the instrumentation	A	/
$\Delta\phi_B$	Schottky barrier height lowering due to image-force lowering	V	/
$\Delta\phi_B'$	Schottky barrier height lowering due to static lowering	V	/
$\Delta\phi_B^{\text{piezotronic}}$	Change in the Schottky barrier height due to the piezotronic effect	V	/
ε	Strain	1	/
ε_i	Internal strain	1	/
ε_{\min}	Minimal strain detectable by the instrumentation	1	/
ε_s	Permittivity of ZnO thin film	F.m ⁻¹	8.59* ε_0
ε_0	Permittivity of vacuum	F.m ⁻¹	8.8541*10 ⁻¹²
θ	Glancing angle	rad	/
λ	X-ray wavelength for Cu K α radiation	m	1.5406 Å
ξ	Distance between the Fermi level and the bottom of the conduction band	V	/
ρ	Resistivity	Ω .m	/
τ	Interface trap states time constant	s	/
ϕ_B	Schottky barrier height	V	/
ϕ_B^{eff}	Effective Schottky barrier height	V	/
ω	Angular frequency	Hz	/

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1. Introduction

In this introductory chapter we define the fundamentals of the piezotronic effect. The state-of-the-art sensing applications as well as the constitutive materials making use of the piezotronic effect will thus be described, before detailing the scope and the driving motivations of this study.

1.1. Fundamentals of the piezotronic effect

The piezotronic effect is usually observed in heterojunction systems, at the interface between a piezoelectric semiconductor and a metal, a semiconductor, or an electrolyte [1]. However, the most studied system in the field of piezotronics consists in a junction between a piezoelectric semiconductor and a metal [2,3]. Within this scope, this section will focus on a junction between a high work function metal and an n-type piezoelectric semiconductor, where the work function ϕ_m from the metal is superior to the electron affinity χ_s of the semiconductor.

We will first consider the case of such a junction without any external strain applied. As the distance between the metal and the semiconductor is reduced, the electrons from the semiconductor are tunnelling through the metal until the Fermi level from both materials are aligned. This leads to the creation of a depletion region (also called space charge region) of width W , free from electrons, consisting of fixed positive charges from non-compensated donors. These positive charges located in the semiconductor, together with the negative surface layer formed by the electrons at the surface of the

metal, create an electric field located almost entirely in the depletion region. Consequently, the resulting electrostatic potential induces the band bending, as shown in Fig. 1.1.

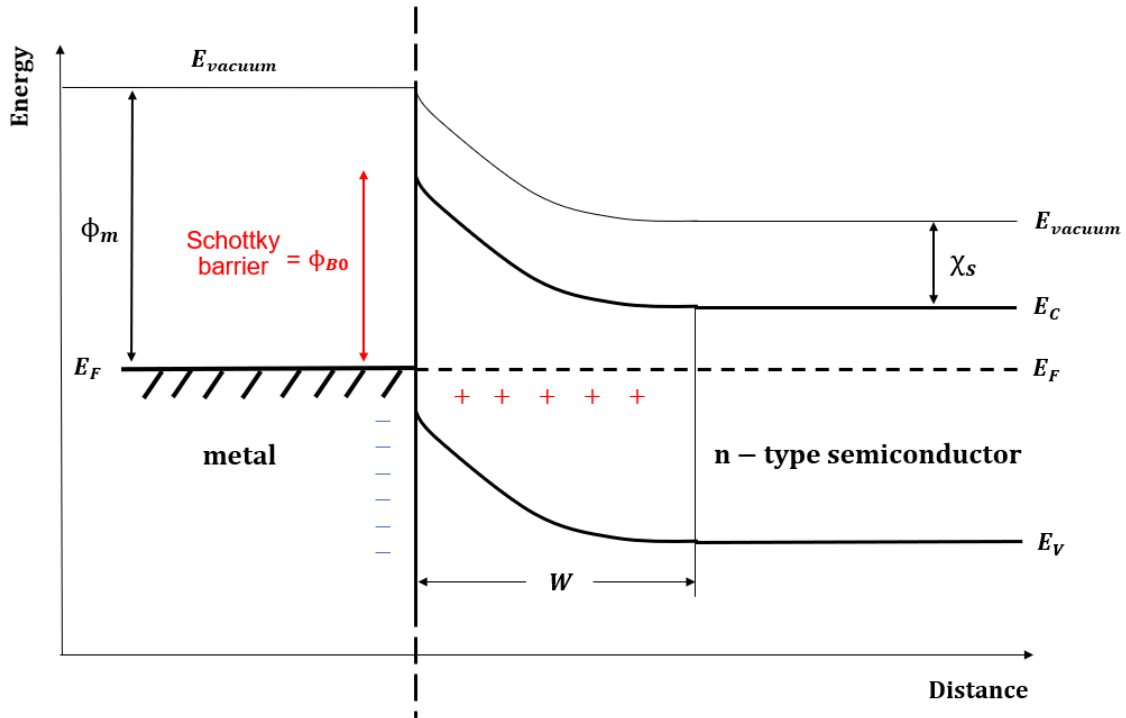


Figure 1.1. Energy-band diagram showing the band bending profile of metal-semiconductor junction, with a high work function metal and an n-type semiconductor. E_{vacuum} , E_F , E_C , E_V : Vacuum level, Fermi level of the metal, conduction band of the semiconductor, valence band of the semiconductor, respectively.

The electrons thus must overcome an energy barrier, called the Schottky barrier, in order to pass from one material to the other. The resulting Schottky barrier height (SBH) ϕ_{B0} is predicted by the Schottky-Mott rule [4,5] to be equal to the difference between the electron affinity of the semiconductor and the work function of the metal, as:

$$\phi_{B0} = \phi_m - \chi_s \quad (1.1)$$

The expression given by equation 1 is limited to the case on an ideal contact between the metal and the semiconductor. In practice, the barrier heights values given by the Schottky-Mote rule are not observed experimentally. Several parameters can lead to

a substantial deviation from the ideal value, such as the presence of interface trap states, an interfacial oxide layer or image-force lowering [6]. The presence of a Schottky barrier at a metal-semiconductor (M-S) junction is the first building block necessary for the apparition of the piezotronic effect. The second building block is linked to the piezoelectric nature of the semiconductor present at the M-S junction, or in other words, to the apparition of electrical charges in the semiconductor in response to an applied mechanical stress or strain.

Within this scope, we will now consider the case of an external strain being applied to the M-S junction. The piezoelectric effect can be observed in non-centrosymmetric crystalline materials, where the applied mechanical strain creates or changes the electric dipole moments by modifying the distance between the center of positive and negative charges. When a piezoelectric material is deformed, piezoelectric polarization charges are thus induced at the M-S junction. These piezoelectric charges have a direct impact on the interfacial band structure and thus on the carrier transport, trapping, generation, and recombination properties [2].

If a compressive strain is applied to M-S junction along the c-axis direction of the semiconductor, negative piezoelectric polarization charges induced at the interface will thus increase the local SBH, as shown in Fig. 1.2(a). However, in the case of a tensile strain, positive piezoelectric polarization charges are induced at the interface and contribute to the decrease of the SBH, as shown in Fig. 1.2(b). The piezotronic effect thus allows for a direct modulation of the interfacial band structure actuated by strain, via the increase or decrease of the Schottky barrier height at the junction between a high work function metal and a piezoelectric semiconductor.

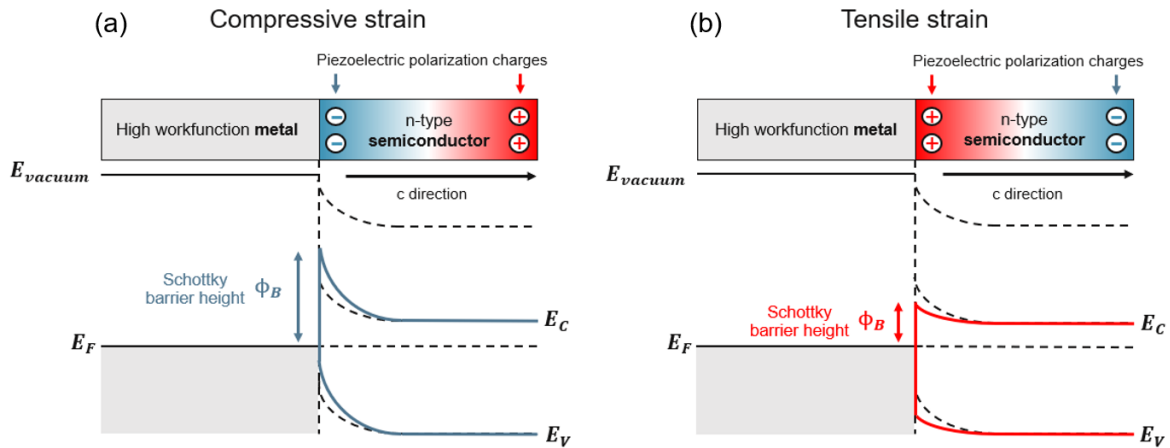


Figure 1.2. Schematic energy diagram showing how strain-induced piezopotential modulates the metal-semiconductor (M-S) contact junction. (a) With compressive strain applied, the negative piezoelectric polarization ionic charges induced near the M-S interface increase the local Schottky barrier height (SBH). (b) With tensile strain applied, the positive piezoelectric polarization ionic charges induced near the M-S interface decrease the local SBH.

It is important to emphasise that the piezotronic effect is an interface phenomenon actuated by a piezoelectric polarization, leading to a change of the interfacial carrier dynamics, which should not be mistaken with a bulk phenomenon such as the piezoresistive effect. Within semiconducting materials, the piezoresistive effect results from a change in the electronic band structure, in the charge carrier mobility or in the density of states in the conduction band under a mechanical strain, leading to a volume effect altering the geometrical section as well as the bandgap of the semiconducting material. However, under the application of a mechanical strain, both the piezotronic and the piezoresistive effects coexist inside a piezoelectric semiconductor and need to be decoupled to evaluate their respective impact on the electromechanical coupling of a device. In 2014, Zhu et al. [7] investigated the separation of the piezotronic and piezoresistive effects in a zinc oxide nanowire. They demonstrated that the piezotronic effect has a dominant role over the piezoresistive effect in the strain-induced current transport properties. Furthermore, the piezoresistive effect also has an impact on the metal as the exerted strain modifies the geometrical section of the metal, leading to a modulation of its resistance. However, this effect is negligible in magnitude for low applied strains or compared to the piezoresistive or piezotronic effects existing in semiconductors.

The carrier transport in M-S structures is dominated by the majority carriers, i.e. electrons with an n-type semiconductor. According to the thermionic-emission-diffusion theory by Schottky [6], the current density J_{n0} flowing through a metal/semiconductor junction under a forward bias V , in the absence of mechanical strain, can be written as:

$$J_{n0} = A^* \cdot T^2 \cdot e^{\left(\frac{-q \cdot \phi_{B0}}{k_B \cdot T}\right)} \cdot \left[e^{\left(\frac{q \cdot (V - I \cdot R_S)}{\eta \cdot k_B \cdot T}\right)} - 1 \right] \quad (1.2)$$

Where J_{n0} and ϕ_{B0} are respectively the current density and the Schottky barrier height in the absence of piezoelectric polarization charges, A^* the Richardson constant, q the elementary charge, T the temperature, k_B the Boltzmann constant, I the current flowing through the structure, R_S the series resistance of the semiconductor and η the ideality factor. The ideality factor is a measure of how closely the M-S junction is following the ideal Schottky-diode behaviour.

Under straining, the created piezo-charges density ρ_{piezo} at the metal/semiconductor interface not only change the height of the Schottky barrier height ϕ_{B0} , but also its width by W_{piezo} , as [3]:

$$\phi_B = \phi_{B0} - \frac{q^2 \cdot \rho_{\text{piezo}} \cdot W_{\text{piezo}}^2}{2\epsilon_S} \quad (1.3)$$

With ϕ_B being the height of the Schottky barrier in the presence of piezoelectric polarization charges, ϵ_S being the dielectric constant of the semiconductor.

Thus, the current density J_n flowing through the M-S junction in the presence of piezoelectric polarization charges can be written as:

$$J_n = A^* \cdot T^2 \cdot e^{\left(\frac{-q \cdot \phi_{B0}}{k_B \cdot T}\right)} \cdot e^{\left(\frac{q^2 \cdot \rho_{\text{piezo}} \cdot W_{\text{piezo}}^2}{2\epsilon_S \cdot k_B \cdot T}\right)} \cdot \left[e^{\left(\frac{q \cdot (V - I \cdot R_S)}{\eta \cdot k_B \cdot T}\right)} - 1 \right] \quad (1.4)$$

Most noticeably, the current transported across the M-S junction has an exponential dependence on the created piezoelectric polarization charges, the sign of which depends on the applied strain ϵ .

It should be noted that equation (1.3) is homogeneous to Joules, while the equation (1.4) is homogeneous to Amperes per meter squared. Thus, the exponential term in equation (1.4) needs to be divided by the elementary charge q to conserve the dimension homogeneity.

Using the definition of the direct piezoelectric effect, the piezoelectric polarization P_i can be expressed as [8]:

$$P_i = e_{ijk} \epsilon_{jk} = d_{ijk} \sigma_{jk} \quad (1.5)$$

Where e_{ijk} and d_{ijk} are the tensors corresponding to the piezoelectric strain and stress coefficients of the semiconductor composed of 18 elements in a 3×6 matrix, ϵ_{jk} and σ_{jk} are the tensors corresponding to the mechanical strain and stress applied to the M-S structure, respectively.

The generalized Hooke's law gives a linear relationship between the stress tensor components and the strain tensor components, as:

$$\sigma_{ij} = C_{ijkl} \epsilon_{kl} \quad (1.6.1)$$

$$\epsilon_{kl} = S_{ijkl} \sigma_{ij} \quad (1.6.2)$$

Where C_{ijkl} and S_{ijkl} are the elastic stiffness coefficients and the elastic compliance coefficients, respectively.

When applied to a metal-wurtzite semiconductor contact, due to crystal symmetry, the tensor corresponding to the piezoelectric coefficients is reduced to three independent components [8]. The previous equation can thus be written as:

$$\begin{bmatrix} P_{xx} \\ P_{yy} \\ P_{zz} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & e_{15} & 0 \\ 0 & 0 & 0 & e_{15} & 0 & 0 \\ e_{31} & e_{31} & e_{33} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \varepsilon_{xx} \\ \varepsilon_{yy} \\ \varepsilon_{zz} \\ \varepsilon_{xy} \\ \varepsilon_{yz} \\ \varepsilon_{zx} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & d_{15} & 0 \\ 0 & 0 & 0 & d_{15} & 0 & 0 \\ d_{31} & d_{31} & d_{33} & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \sigma_{xx} \\ \sigma_{yy} \\ \sigma_{zz} \\ \sigma_{xy} \\ \sigma_{yz} \\ \sigma_{zx} \end{bmatrix} \quad (1.7)$$

Where e_{31} (d_{31}) is the piezoelectric coefficient corresponding to the induced piezoelectric polarization along the c-axis of the hexagonal wurtzite structure per unit of strain (stress) applied in the plane of the structure. Similarly, e_{33} (d_{33}) corresponds to the induced piezoelectric polarization along the c-axis of the hexagonal wurtzite structure per unit of strain (stress) applied perpendicular to the structure. Moreover, e_{15} (d_{15}) corresponds to the induced piezoelectric polarization in the plane of the hexagonal wurtzite structure per unit of shear strain (stress) applied.

By neglecting the polarization induced by a shear strain (i.e. the strain is only applied either in the plane or perpendicular to the wurtzite structure), the equation further reduces to:

$$P_z = e_{33} \cdot \varepsilon_z + e_{31}(\varepsilon_x + \varepsilon_y) \quad (1.8)$$

Where ε_z is the strain applied along the c-axis direction of the M-S structure, ε_x and ε_y are the strains applied in the x and y directions in the plane of the M-S structure.

Additionally, the piezoelectric polarization can be expressed as a function of the piezo-charges density, as [3]:

$$P_z = q \cdot \rho_{\text{piezo}} \cdot W_{\text{piezo}} \quad (1.9)$$

Consequently:

$$e_{33} \cdot \varepsilon_z + e_{31}(\varepsilon_x + \varepsilon_y) = q \cdot \rho_{\text{piezo}} \cdot W_{\text{piezo}} \quad (1.10)$$

Injecting equation (1.10) into equation (1.4) finally results in the following equation:

$$J_n = A^* \cdot T^2 \cdot e^{\left(\frac{-q \cdot \Phi_{B0}}{k_B \cdot T}\right)} \cdot e^{\left(\frac{q \cdot W_{\text{piezo}} \cdot [e_{33} \cdot \varepsilon_z + e_{31}(\varepsilon_x + \varepsilon_y)]}{2 \varepsilon_S \cdot k_B \cdot T}\right)} \cdot \left[e^{\left(\frac{q \cdot (V - I \cdot R_S)}{\eta \cdot k_B \cdot T}\right)} - 1 \right] \quad (1.11)$$

The current transported through the M-S junction can thus be effectively tuned or controlled not only by the magnitude of the strain, but also by the sign of the strain, depending on its compressive or tensile nature. Another crucial feature lies in the remnant nature of the piezoelectric polarization, meaning that the piezotronic effect will remain in a given structure as long as the strain is applied [9]. The modulation of the local Schottky barrier height results in an exponential increase or decrease of the electrical current flowing through the M-S junction, which in turns leads to an exponential increase of the electromechanical sensitivity. This is the rationale of the piezotronic junction.

1.2. State of the art

1.2.1. Early developments in the field of piezotronics

The electromechanical dependence at the base of the piezotronic effect had already been observed experimentally in the prior art. In 1974, Frederick J. Jeffers [10] proposed for the first time in the frame of a patent the realization of a highly sensitive strain sensor on a silicon-based structure by integration of a Schottky junction. The electrical properties of the sensor were modulated upon the application of positive and negative strains, showing that the exponential dependence of the electrical properties on the applied strain with a Schottky junction was already understood. The authors mentioned the used of wurtzite piezoelectric semiconducting materials (e.g. CdS, InN, GaN, ZnO) with a metal electrode to obtain such a diode behaviour under strain.

In 1998, Hiroshi Takahashi et al. [11] proposed in a patent the integration of a diode junction used as a strain sensor on a silicon-based cantilever with a tip for scanning probe applications, as shown in Fig. 1.3(a). The authors demonstrated as well the non-

linear behaviour of the electrical properties from the diode junction under mechanical strain (see Fig. 1.3(b)). Furthermore, they highlighted the comparison between the exponential behaviour of the electrical properties with the piezoresistive effect (see Fig. 1.3(c)), effectively showing that higher sensitivity could be achieved when a Schottky junction is subject to a mechanical deformation.

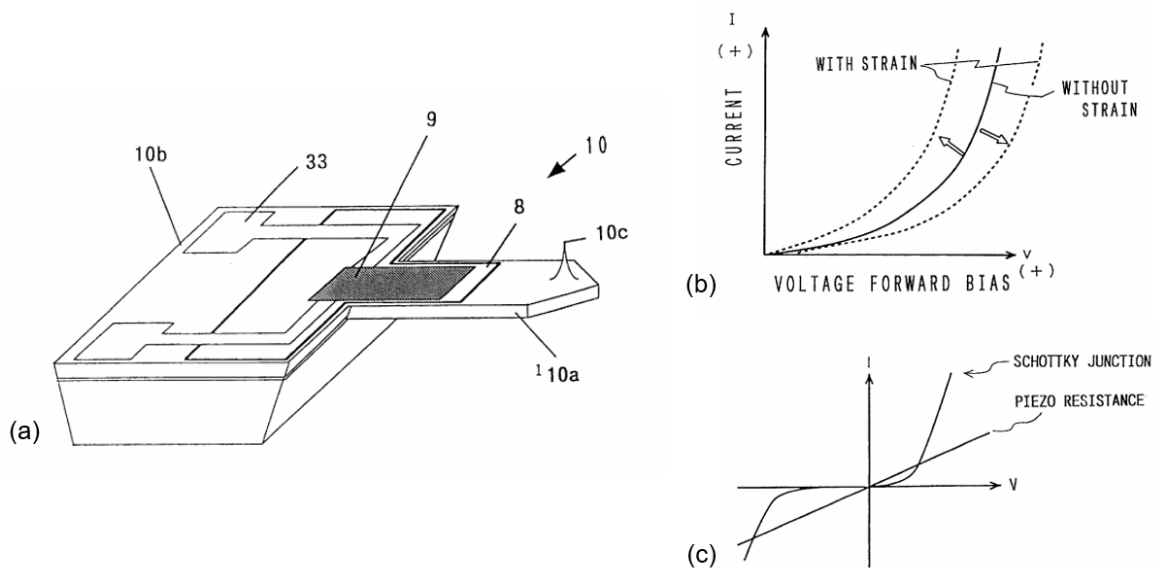


Figure 1.3. (a) Integration of a diode junction on a silicon-based cantilever with a tip for scanning probe application. (b) Electrical properties of the diode junction showing the exponential impact of the strain on the $I(V)$ properties under forward bias voltage. (c) Qualitative comparison between the $I(V)$ properties of the Schottky junction with a piezo resistance. Adapted from [11].

The piezotronic effect was first highlighted in a scientific publication in 2000 by P. M. Verghese and D. R. Clarke [12] by the piezoelectric contributions to the electrical behaviour of ZnO varistors. In 2006, Wang's group [13] showed the piezotronic effect in piezoelectric wurtzite ZnO nanowires with n-type conductivity. In 2007, the term of "piezotronic" was introduced while rationalizing its fundamental principles [14]. It was demonstrated by using ZnO micro and nanowires that a fast response and a higher electromechanical sensitivity could be achieved when compared to the conventional methods of strain sensing [15]. Moreover, the piezotronic effect is based on a mechanical signal triggering, which is one of the most common kind of interactions between the environment and electronic systems. Within this scope, the field of

piezotronics started to draw a considerable attention in the early 2010's, with obvious applications in strain sensing. Shortly after, pressure and force sensing, as well as chemical and light sensing applications making use of the piezotronic effect emerged in the literature. These different fields of study and their recent progress will be summarized in the next sections, with a particular emphasis on the materials, morphologies and device architectures used, as well as the performances achieved in piezotronic strain sensing applications.

1.2.2. Piezotronics for strain sensing applications

As previously mentioned, strain sensing is naturally suited for piezotronic devices due to the strain-generated piezoelectric polarization potential acting as a virtual gate to tune the Schottky interface band structure. The so-called gauge factor (GF) is typically used in order to characterize the sensitivity of strain sensors. The expression commonly used in the literature for the field of piezotronics is based on the absolute value of the ratio of relative change in the electrical current I to the mechanical strain ε , as:

$$GF = \left| \frac{\Delta I}{I_0} \cdot \frac{1}{\varepsilon} \right| \quad (1.12)$$

With I_0 being the steady state current for a given bias, and ΔI the change in current under a given strain ε for the same applied bias. We can notice that the expression of the gauge factor was first derived from piezoresistive sensors [16].

In 2008, Zhou et al. [15] demonstrated the first application of piezotronic strain sensor while using arrays of ZnO microwires and silver paste as a M-S junction, with a flexible polystyrene (PS) substrate, as shown in Fig. 1.4. The working principle is quite straightforward, as a lateral bending is exerted, leading to the generation of compressive and tensile strains along the length of the nanowires. They reached a gauge factor value of 1250, which was at that time higher than the best gauge factor value of 850 achieved for piezoresistive carbon nanotubes [17]. As a matter of comparison, the gauge factor achieved for commercial piezoresistive metallic foils are typically ranging between 2 and 5, while the values for silicon-based sensors are

ranging between 100 and 200 [18]. The gauge factor value for piezotronic strain sensors was further increased to 3740 by Wu et al. [19] in 2012, by using a ZnSnO₃ nanowire/microwire. In 2015, Zhang et al. [20] reported a gauge factor value as high as 4036, with In-doped ZnO nanobelts showing improved mechanical performances. These quick developments and improvements made in terms of electromechanical coupling contributed to increase the interest in the field of piezotronics.

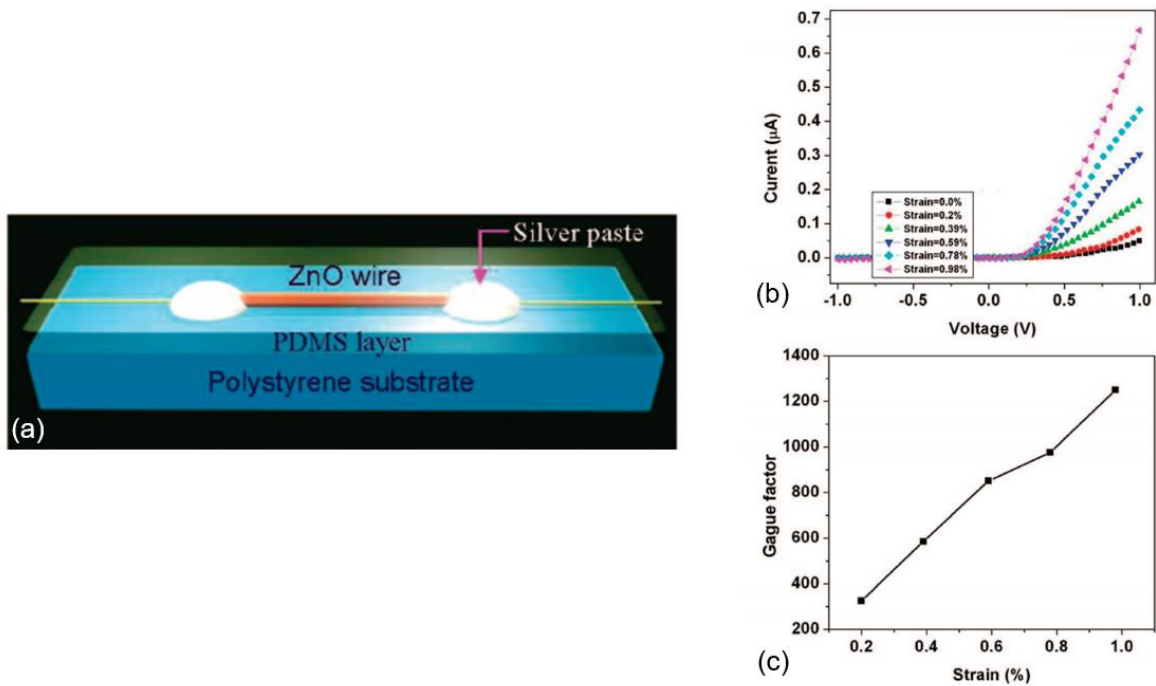


Figure 1.4. Device architecture and electrical performances of a piezotronic strain sensor. (a) Sketch of the device architecture, with a ZnO microwire used as the piezoelectric semiconductor, silver paste as metal electrodes, PS as a flexible substrate and PDMS as an encapsulation layer. Not to scale. (b) I(V) characteristics under different strains values. (c) Gauge factors values obtained from the electrical characteristics, for different strains values. Reprinted from [15].

The basic building block for the piezotronic effect being a piezoelectric semiconductor, materials from the wurtzite family are excellent candidates owing to their non-centrosymmetric crystalline structure. Among them, ZnO [15,20–24] was the most commonly used semiconductor in the early developments of the piezotronic field and keep being a material of choice at the time being owing to its ease of process, direct piezoelectric response and high piezoelectric coefficient. The piezotronic effect was then demonstrated with other non-centrosymmetric semiconducting materials, including GaN [25,26], CdS [27], InN [28] and MoS₂ [29]. Most notably, other materials

like ZnSnO_3 were used [19,30], by providing a higher piezoelectric polarization along the c-axis compared to single ZnO nanowires. Furthermore, doping appeared as a viable solution to improve the electromechanical coupling of the devices. Li [31], S [32], In [20] and Sb [33] were successfully introduced as dopants in ZnO, leading to a higher electromechanical coupling and thus yielding higher sensitivities compared to their non-doped counterpart. Additionally, Wang et al. [34] reported on higher piezoelectric potential and strain sensitivity achieved through alloying of AlN with GaN, compared to the individual binary compounds.

Regarding materials morphology, microwires and nanowires are the most studied and reported structures in the field of piezotronics [15,19,39,21–23,27,35–38], due to their low-dimensional geometries, superior mechanical properties and robustness facilitating their integration into flexible devices [40]. The nanowires are grown perpendicular to their substrate along the c-axis direction, the most common deposition techniques being chemical vapor deposition (CVD) and the hydrothermal method [2]. Regarding substrates, flexible polymeric materials such as polystyrene (PS) or polyethylene terephthalate (PET) are typically used, while using PDMS for the encapsulation of the structure, as shown in Fig. 1.4(a). The encapsulation is particularly important for the protection against environmental contamination, as well as to preserve the long-term performances of the devices [41]. Among these structures, nanowire arrays [23,27] were developed, the presence of multiple wires allowing for a better reliability and stability during the device operation, with direct applications in human-electronics interfacing and smart skin. Other materials morphologies such as nanobelts [20,25,30] and more recently polycrystalline ZnO thin films [42–45] have been reported.

As stated in the previous section, an n-type semiconductor is most commonly used and contacted with a high work function metal to form a Schottky junction, where the current transport is due mainly to majority carriers, i.e. electrons. The early development in the field of piezotronics consisted mostly of proof-of-concept devices making use of metal-semiconductor-metal (M-S-M) junctions, with double Schottky barriers being used [15,21,30]. Among the different works previously reported, the most common high work function metallic electrodes used include silver paste, gold, and platinum [46]. The current transport properties are either symmetric or asymmetric

across the M-S-M junctions, respectively depending if the same metal is used to contact the semiconductor or if two different metallic electrodes are employed. However, one of the metallic contacts used in the device might be ohmic [23] (e.g. Cr, Al), leading to an increased electrical current flowing through the structure. The case of the M-S-M is quite peculiar as one of the Schottky junctions will necessarily be reversely biased, thus limiting and dominating the current transport properties across the device. Several theoretical conduction mechanisms models have been developed to account for the current transport properties through Schottky junctions, depending mainly on the carrier concentration and mobility of the semiconductor [6]. Nonetheless, the conduction mechanisms in such devices are commonly treated by the thermionic model [27], the thermionic emission-diffusion model [3,15], or the thermionic-field emission model [47,48]. A detailed analysis of these current transport processes in M-S-M junctions will be provided in the Chapter 4.

More recently, metal-insulator-semiconductor (M-I-S) junctions making use of the piezotronic effect were reported in the literature. A thin oxide insulating layer is added at the junction between the metal and the semiconductor, which leads to the creation of a piezotronic tunnelling junction. The phenomenon of quantum tunnelling through the insulating layer can be controlled and tuned by the applied mechanical stimuli and is defined by an exponential dependency to the current, which results in a substantial increase of the current and the resulting sensitivity. This electron-tunneling modulation was successfully demonstrated with a MgO monolayer [49,50] and an ultrathin Al₂O₃ oxide layer [51], resulting in an improved electromechanical transducing efficiency with a reported gauge factor value of 2.6×10^8 for the Al₂O₃ oxide layer. Furthermore, piezotronic heterojunctions were investigated as well with a first theoretical framework in 2013 [52]. The working principle remains similar as the M-S junction, as a mechanical strain is applied to a p-n junction between two piezoelectric semiconductors. The strain-induced piezoelectric potential is used to tune the energy band profile of both semiconductors at the local heterojunction interface, which in turns effectively modulates the electrical current transport properties of the structure. Within this scope, heterojunctions consisting of InGaN/GaN [39] and AlGaN/AlN/GaN [37,53] were developed in the recent years.

Moreover, Wang's group introduced in the early 2010's the concept of the piezotronic transistor [3]. As a matter of comparison, the conventional metal oxide semiconductor field-effect transistor (MOSFET) and the nanowire-based field-effect transistor (FET) are shown in Fig. 1.5(a) and (b). Within these structures, a bias voltage is applied from the source to the drain while a gate voltage is used to tune the channel width, thereby controlling the transport of charge carriers. In piezotronic transistors, a M-S-M structure with a piezoelectric semiconductor and two metallic electrodes undergoes the source-to-drain voltage while the gate voltage is substituted by the strain-generated piezoelectric potential at the Schottky junctions, as illustrated in Fig. 1.5(c) and (d). Transistors being one of the basic building blocks of modern electronics, the interest in piezotronic transistors substantially increased in the recent years with several reports demonstrating the use of such systems [26,54–59]. Zhu et al. [59] reported in 2018 a gauge factor value over 10^4 while using a piezotronic strain sensor based on a bipolar transistor structure.

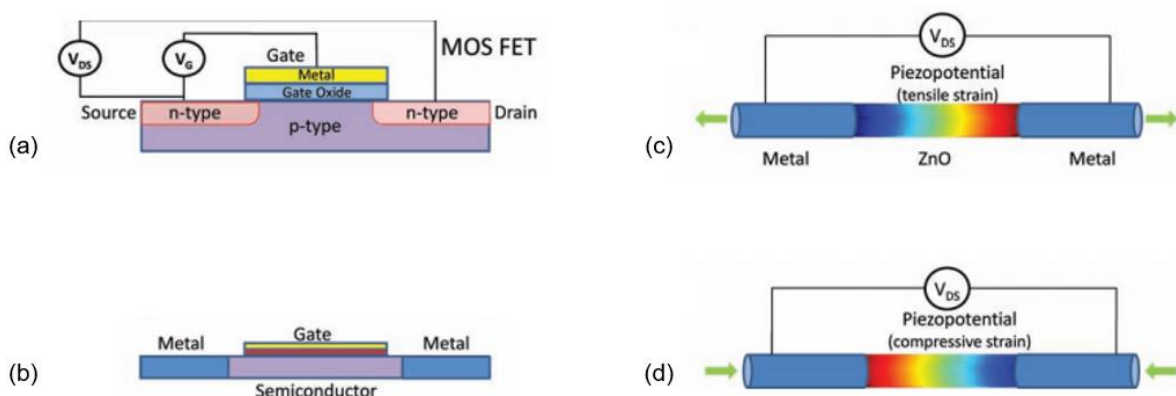


Figure 1.5. Schematics illustrating the analogy between (a) an n-channel MOSFET and (b) a piezoelectric semiconducting nanowire FET. The piezotronic transistor working principle is illustrated (c) under tensile strain and (d) under compressive strain. Reprinted from [3].

The piezotronic strain sensor technologies are typically operating within the microAmpere and microWatt ranges, combined with a fast time response in the millisecond range and quick recovery of the steady-state properties [2]. Piezotronic strain sensors thus appear as a promising candidate for low power consumption sensing technologies, compared to piezoresistive and capacitive sensors operating in

the milliWatt range. The reported fast time responses and high sensitivities pave the way towards the development of new generations of Micro-ElectroMechanical Systems (MEMS) and Nano-ElectroMechanical Systems (NEMS). Several applications can be derived from piezotronic strain sensing, including autonomous, self-sensing sensors in the frame of the Internet-of-Things, self-powered flexible electronics and wearable systems, as well as in the automotive or aeronautic industry.

1.2.3. Piezotronics for pressure and force sensing applications

The piezotronic effect can easily be transferred to pressure and force sensing applications, as a mechanical stimuli can be applied by either pressure or force to a M-S junction. The working principle remains similar as strain sensing, where a piezoelectric potential is created at a local Schottky barrier, thus modifying the interfacial band structure and tuning the resulting electrical properties of the device. Early developments within this field consisted mostly of single nanowire [47] or nanowire arrays [27,60,61] structures, where a force is applied along the c-axis direction of the nanowires. These devices showed high performances in terms of sensitivity and spatial resolution [2], with reported force sensing thresholds as low as 4 nN [62].

More recently, the development of piezotronic transistor arrays [31,63–65] emerged in the literature towards pressure and force sensing applications, reaching unprecedented sensitivities for such devices. In 2017, Liu et al. [64] reported on a gauge factor value of 1.5×10^7 by using a piezotronic transistor array consisting of ZnO nanoplatelets. The same year, Wang et al. [65] improved the record gauge factor value in the 10^9 range, using a similar device architecture based on ZnO twin nanoplatelets, as highlighted in Fig. 1.6. They reported on pressure sensitivity of ~ 1500 meV/MPa, a pressure sensing threshold as low as a few kPa, together with a fast response time inferior to 5 milliseconds, which shows great prospect for high resolution tactile imaging.

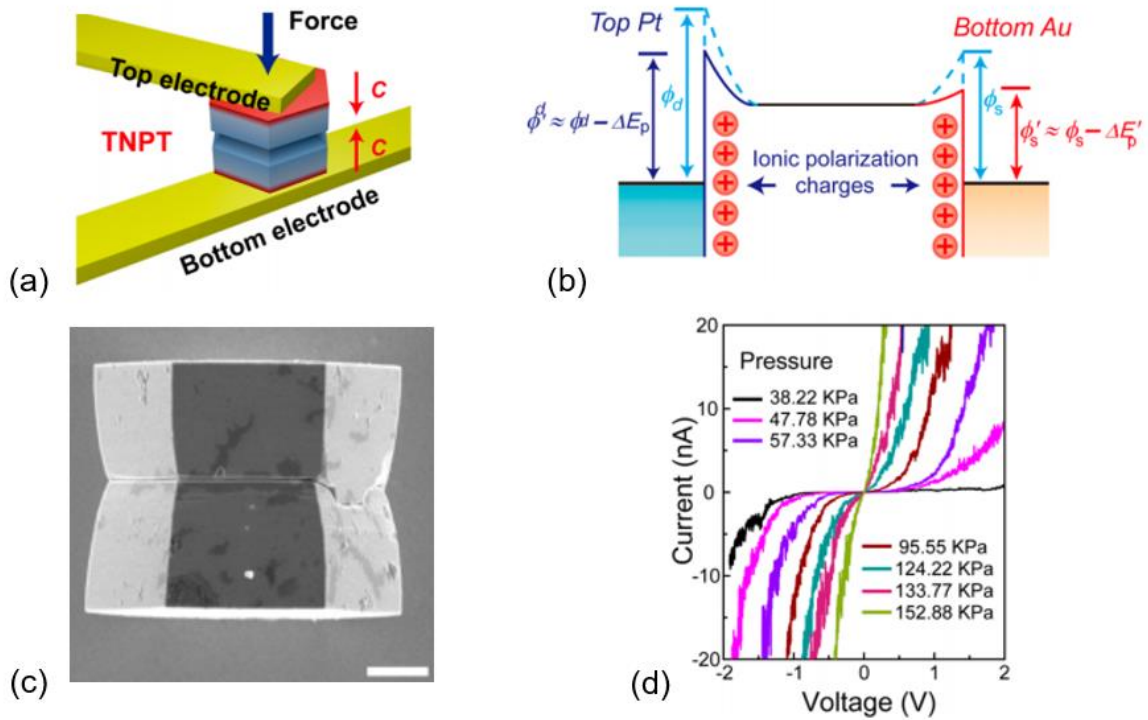


Figure 1.6. (a) Schematic illustration of a piezotronic transistor based on ZnO twin nanoplatelets (TNPT). The red arrows represent the positive c-axes of ZnO twin nanoplatelet. (b) Band diagrams of the working mechanism of the piezotronic effect with TNPT. (c) Side view of scanning electron micrographs of a ZnO twin nanoplatelet, the scale bar indicating 1 μm . (d) $I(V)$ characteristics under different applied pressures. Reprinted from [65].

Among other structures, Baraki et al. demonstrated the use of polycrystalline ZnO varistor ceramic as piezotronic pressure sensor [66,67]. They highlighted the existence of potential barriers at ZnO grain boundaries, tuning the current transport properties by the strain-induced piezoelectric potential. In 2019, Liu et al. [51] reported a piezotronic tunnelling junction gated by mechanical stimuli in a Pt/Al₂O₃/p-GaN heterostructure, where a Pt coating applied on an AFM tip is used as the metal electrode, Al₂O₃ as the insulating oxide layer and GaN as the piezoelectric semiconductor. The corresponding structure and its electrical properties under different applied pressures are shown in Fig. 1.7(a) and (b). The Pt-coated tip is used as a metal electrode to measure the electrical properties of the device while simultaneously applying compressive forces through conductive atomic force microscopy (c-AFM). They achieved a remarkable gauge factor value of 2.6×10^8 , which further demonstrates the great potential of piezotronic junctions for tactile imaging (i.e. translating the sense of touch into a digital image), as shown in Fig. 1.7(c).

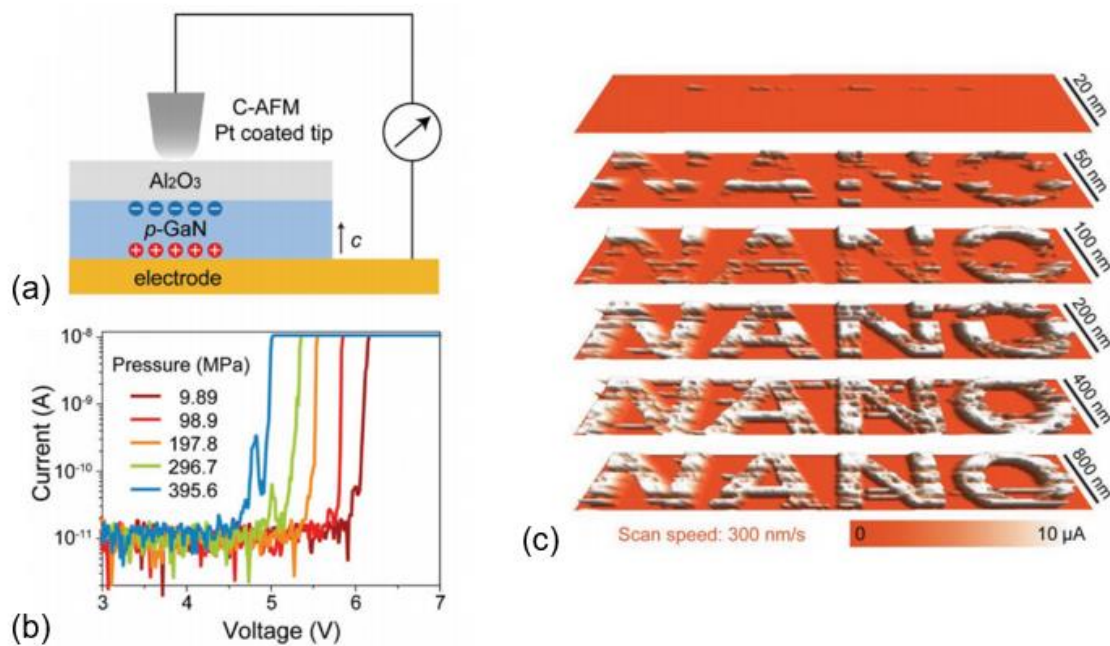


Figure 1.7. (a) Schematic of Pt/Al₂O₃/p-GaN tunneling junction along the c-axis of p-GaN with (b) The corresponding I-V characteristics upon different applied pressures. (c) 3D current response of tactile imaging, with the current response contour plot for imaging the spatial profile "NANO" of applied force with various pixel sizes. Reprinted from [51].

These piezotronic devices can find several applications as ultrasensitive pressure and force electrical triggers, including human-machine interface, artificial skin, adaptive biomedical probes or handwriting recognition.

1.2.4. Piezotronics for chemical sensing applications

Following the promising early developments of piezotronic strain and pressure-based devices, chemical sensing applications were developed in the early 2010's. Semiconducting nanowire based field effect transistors (FETs) appeared as an ideal candidate for such applications, owing to their large surface to volume ratio, their flexibility, as well as their ability of surface functionalization used to detect specific biomolecules [68]. The strain-induced piezoelectric potential along the nanowire leads to a non-uniform distribution of the target molecules, which are concentrated mostly

near the nanowire surface due to the electrostatic interaction of the local piezoelectric polarization charges with the charged molecules. As a consequence, the sensor is more proactive to detect the target molecules even at extremely low overall concentration, thus naturally improving the sensitivity and lowering the detection limit of these devices [69]. Within this scope, several biosensors based on the piezotronic effect emerged in the literature with enhanced sensitivity towards pH [69], protein kinases [70,71], glucose [72], H₂O₂ [73] or DNA [74] detection. It is worth mentioning that these devices all make use of ZnO as a piezoelectric semiconducting material, due to its biocompatibility and biosafety at the cellular level [75]. The piezotronic biosensors have obvious applications in the medical sector, as self-powered health-monitoring devices with enhanced sensitivity.

Another field of research is directed towards the development of gas sensing devices. In 2013, Niu et al. [48] reported on oxygen sensors whose sensitivity was enhanced by the coupling of gas molecule adsorption and the piezotronic effect. A pre-treatment with UV light was applied for pre-removal of oxygen on the device. Further exposure to oxygen leads to the adsorption of oxygen molecules, creating an electron depletion layer on the nanowire surface, thus reducing the carrier concentration in the device and tuning the band bending profile, as shown in Fig. 1.8(a) and (b). A strain is then applied to the nanowire, the strain-induced piezoelectric charges adding another way of modulation of the electrical properties of the device (see Fig. 1.8(c)).

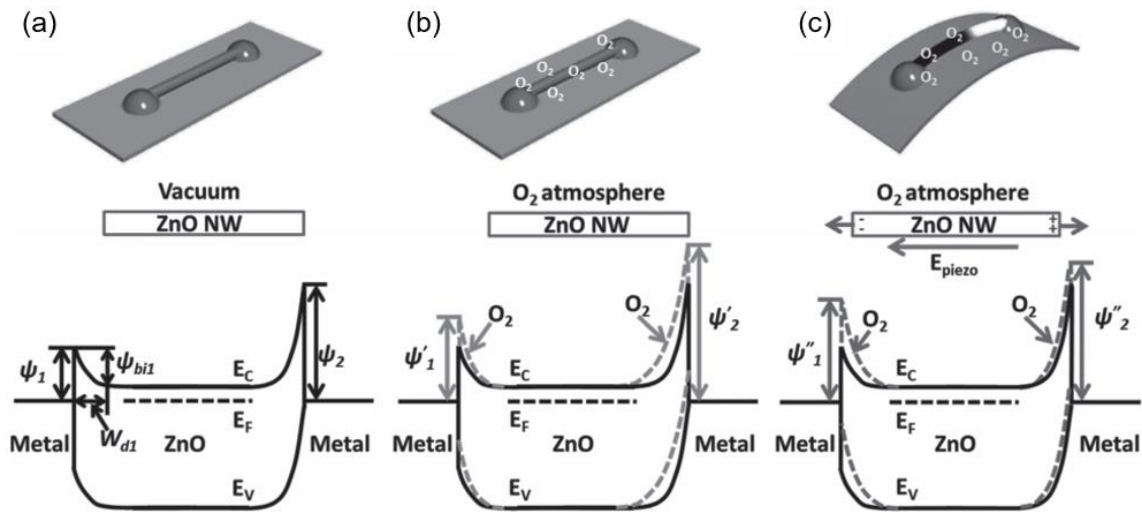


Figure 1.8. Illustration of a ZnO nanowire-based sensor with the corresponding energy band diagram. (a) Under vacuum, no strain applied. (b) In an oxygen atmosphere, no strain applied. (c) In an oxygen atmosphere with a tensile strain applied. Reprinted from [48].

Similar works were reported concerning the detection of flammable or toxic gases (e.g. hydrogen (H_2) and nitrogen dioxide (NO_2)) [76], as well as humidity sensing [77,78], showing high sensitivity and low power consumption. Such devices have great potential applications as life protection, environment monitoring or automobile engine control systems.

1.2.5. Piezotronics for optoelectronic sensing applications

Piezo-phototronics was introduced in 2010 as an emerging field exploring the three-way coupling among mechanical, optical and electrical properties in materials with non-centrosymmetric crystal structure [79,80]. In other words, in a given structure (e.g. a M-S junction) as well as in the presence of a light source, the photon excitation is combined with the piezotronic effect to tune the device optoelectronic properties. Recent studies demonstrated that the strain-induced piezoelectric polarization charges at a local interface can tune and control the charge carrier generation, separation, transport, or recombination by modifying the local electric field distribution in a M-S junction or in a heterojunction [81]. Two distinct working areas can be identified within the piezo-phototronics field [82]. On the one hand, the photo-generated charge carrier

generation and separation process can be promoted by the strain-induced electric field, leading to a substantial improvement of the performances of photodetectors [35,83–87], solar cells [88–91], as well as in the photocatalyst activity [92]. On the other hand, the carrier injection or recombination process can be tuned by modifying the local electrical field in order to control the electroluminescence properties of a given device, showing great prospect towards improved emission efficiency in light-emitting diodes (LEDs) [93–95]. The piezo-phototronics field thus appear as a great candidate for the next generation of high-efficiency artificial lighting and high-performance solar cells, with several applications in flexible electronic devices and power sources.

1.3. Scope of the study

1.3.1. Context

The interest for zinc oxide thin films has become increasingly important in the last decades for applications in the fields of thin-film transistors [96], gas sensors [97], light-emitting diodes [98] and nanogenerators [13,99]. ZnO wurtzite material has already been extensively used as a piezoelectric material for actuation of microstructures [100,101], and accounts for the most reported material in the field of piezotronics. However, the incorporation of semiconducting materials into MEMS remains a challenging task, due to the low deposition temperature needed for the compatibility with CMOS technologies [102] and also with polymeric substrates, as well as to the use of materials compatible with cleanroom facilities. Most of the structures presented in the previous section are based on proof-of-concept devices limited to the laboratory scale. Moreover, up to now, no consistent study has emerged to demonstrate the optimized configurations for piezotronic materials properties and electrodes interface configurations, particularly for reliable microfabrication processing for MEMS. Most notably, the integration of strain self-sensing sensors based on piezotronic diode junction inside plastic cantilever for scanning probe application is not present in the literature.

When it comes to cantilever motion detection, we can find different methods of sensing, the most common methods being the optical, capacitive, piezoresistive and piezoelectric. These methods have identified strengths and weaknesses in terms of sensitivity, operating regimes and ease of integration, as reported in Table 1.

Methods of sensing	Strengths	Weaknesses
Optical	<ul style="list-style-type: none"> - Very high detection sensitivity in displacement (thermomechanical noise floor) 	<ul style="list-style-type: none"> - Bulky system with difficult integration - Sensitivity to thermal drift - Difficult laser alignment (even more for micrometer structures)
Capacitive	<ul style="list-style-type: none"> - High detection sensitivity in displacement - No Flicker noise - Main approach used in MEMS for gyroscopes, accelerometers 	<ul style="list-style-type: none"> - Narrow and high aspect ratio electrodes gap is challenging to fabricate - Electrodes gap is sensitive to defects, moisture, dusts and thin-film damping - Operation at high voltage superior to 10 V
Piezoresistive	<ul style="list-style-type: none"> - Easy integration on standard silicon-based process - Operation in DC and AC regimes 	<ul style="list-style-type: none"> - Moderate sensitivity with gauge factors from 2 (metal electrodes) to 150 (graphene electrodes) - Sensitivity to thermal drift (without differential measurement) - Inherent Flicker noise
Piezoelectric	<ul style="list-style-type: none"> - Very easy calibration set by a resonance curve - High sensitivity in AC regime (with high Q factor as in ultrahigh vacuum UHV environments) 	<ul style="list-style-type: none"> - Operation only limited to AC regime - Low sensitivity in low Q environments (air, liquid)
Piezotronic	<ul style="list-style-type: none"> - Breakthrough in strain sensitivity with very high gauge factors until 10^8 - Operation in DC and AC regimes 	<ul style="list-style-type: none"> - No microsystems and MEMS integration demonstrated - No study about the optimal configuration for strain sensing - No noise studies to estimate the signal-to-noise ratio

Table 1. Strengths and weaknesses of the different methods of sensing for cantilever motion detection.

The piezotronic effect emerged recently as a promising candidate wherever a high sensitivity is needed, which can be applied to cantilever motion detection. It is understood that the piezotronic effect consists a breakthrough in strain sensitivity with very high gauge factors reported in the literature until 10^8 , and that it can be operated in both DC and AC regimes. However, several crucial questions remained unanswered or need to be refined, concerning the design and integration of piezotronic junctions with its fabrication process into microsystems or MEMS, the optimal configuration for strain sensing as well as noise studies for such systems. We aim to answer these questions within this work.

1.3.2. Motivation

The structure of this section follows the general structure of the thesis. Each subsection provides the reader with a brief overview of the corresponding chapter, detailing on the motivation as well as the approach adopted.

Deposition, microfabrication and characterization techniques

This chapter briefly introduces and describes the different techniques used within the frame of the study. Among deposition techniques, thermal atomic layer deposition (ALD) has been used for the ZnO thin films processing, electron beam metal evaporation (EBME) for the fabrication of platinum metal electrodes and spin coating for the photoresists' deposition. Additionally, maskless photolithography, reactive ion etching (RIE) and wet etching have been used for thin films microfabrication and patterning, together with wire bonding for the sensors' integration into the electromechanical bench. A wide range of characterization techniques have been employed, including ellipsometry for the thickness determination, X-ray diffraction (XRD), scanning and transmission electron microscopy (SEM, TEM) for structural characterization, as well as X-ray photoelectron spectroscopy (XPS) for elemental and chemical analysis. Additionally, four-point probe, current-voltage (I-V) and

capacitance-voltage (C-V) measurements have been realized to evaluate the electrical characteristics of the metal-semiconductor-metal junctions, while force spectroscopy measurements and noise analysis have been performed to describe the sensors performances. More details are available on Chapter 2.

ZnO thin films elaboration by thermal atomic layer deposition

Wurtzite ZnO thin films grown with a preferential crystallinity perpendicular to their substrate, i.e. along the c-axis orientation, is one the most used semiconducting material in the field of piezotronics. Among semiconducting materials, zinc oxide (ZnO) has attracted considerable attention in the field of semiconductor devices due to several features, such as the material compatibility with cleanroom facilities, low temperature processing or its amenability to wet chemical etching [103,104]. The resulting material physical and chemical properties make it viable and appealing for micro and nanotechnology applications, including the fields of biomedical, energy, sensors and optics [105]. A few works reported on the use of atomic layer deposition (ALD) to deposit ZnO at the junction with metals in order to obtain Schottky junctions [106]. However, such ZnO-based Schottky junctions by ALD have never been post-processed and integrated into a strain sensor. Due to its high film conformality, low temperature processing, self-limiting nature and stoichiometric control at the nanoscale level, ALD has emerged as an ideal technique to add new functionalities in Micro-ElectroMechanical Systems (MEMS) compatible with the low temperature requirements for CMOS technologies [102]. ALD technique can coat high aspect ratio topographies, with flawless interfaces and low temperature process compatibility on polymeric flexible surfaces. Nonetheless, by this mean, the critical control of the ZnO crystalline orientation with high piezoelectric properties, as well as the control of the charge carriers' density and mobility necessary for the obtention of a Schottky junction are highly challenging. We propose to rationalize the ALD processing to obtain wurtzite polycrystalline zinc oxide thin films with a privileged (002) orientation and to make it compatible with microfabrication processing on polymer. More details are available on Chapter 3.

Polymeric cantilevered piezotronic strain sensors

The rapidly spreading Internet-of-Things is accelerating MEMS industry to deliver highly sensitive and miniaturized self-sensors with low power consumption and cost-effective production process. However, up to now, no consistent study has emerged to propose the optimized configurations for piezotronic materials properties and electrodes interface configurations on sensors for microfabrication processing for MEMS. As the sensors consist in a stack composed of several thin film materials, many issues are faced during the microfabrication of the devices, related with the coating of fragile flexible polymeric substrates, as well as the discrepancy between the coefficients of thermal expansion of the different materials. Therefore, we propose a reliable microfabrication process flow composed of simple materials, easily reproducible steps, and compatible with low temperatures processing. Furthermore, the use of interdigitated metal electrodes in contact with the ZnO thin films leads to the formation of several back-to-back Schottky diode junctions, i.e. metal-semiconductor-metal (M-S-M) junctions. This peculiar architecture is well adapted for MEMS processing, but the conduction mechanisms involved remain mostly unclear and are not well documented in the literature. Similarly, the noise figure of piezotronic junctions has never been explored. We propose to rationalize the electrical and transducing characteristics of such junctions by the means of current-voltage (I-V) and capacitance-voltage (C-V) analysis. Additionally, the integration of strain self-sensing sensors based on piezotronic diode junction inside plastic cantilever for scanning probe application is not present in the literature, and it will be presented in the final part of this section. More details are available on Chapter 4.

Full-SU8 body piezotronic strain microsensors

This section is dedicated to the strain sensors size miniaturization for integration in microcantilevers in a full polymer body. The miniaturization of our strain sensors makes them more prone for AFM (Atomic Force Microscopy) scanning probe operations on commercial machines, while greatly improving the sensitivity to small mechanical

deformations. Miniaturized structures are also more prone for sensors' array architectures able to perform faster parallelized analysis for two-dimensional mapping of strain as AFM force spectroscopy [107,108]. Furthermore, a new microfabrication flow chart has been developed to address the problematic of the cantilever miniaturization. This raised several issues in terms of metal adhesion and electrical contact continuity, with the corresponding development of adapted solutions. The electrical and transducing properties of these devices will be analysed and compared to the benchmark polymeric cantilevered strain sensors described in the previous section. More details are available on Chapter 5.

Conclusions and Perspectives:

Ways to improve electromechanical coupling in metal-semiconductor-metal junctions integrated in piezotronic strain sensors

In outlook we introduce promising ways to improve the electromechanical coupling in M-S-M junctions integrated in our piezotronic strain sensors. The first one consists in directly acting on the ZnO semiconducting material properties via doping with transition metals, which greatly improves the piezoelectric response of the semiconductor. The second method relies on the use of an ultrathin oxide insulating layer added at the junction between the metal and the semiconductor, leading to the creation of a piezotronic tunnelling junction. The phenomenon of quantum tunnelling can be controlled and tuned by the applied mechanical stimuli and is defined by an exponential dependency to the current, which results in a substantial increase of the sensitivity. Moreover, the great potential of the developed piezotronic strain sensors for scanning probe applications is highlighted with the corresponding AFM images obtained. More details are available on Chapter 6.

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2. Deposition, microfabrication and characterization techniques

This chapter aims at introducing and describing the different thin film deposition, microfabrication and characterization techniques used, as well as the manner in which they have been implemented within the frame of the study. More experimental details corresponding to each technique will be given in the relevant sections in the following chapters.

2.1. Thin film deposition techniques

Dielectric thin films and thin metal layers serve as the main bricks composing the piezotronics junctions realized in this work. Hence, it is essential to use peculiar deposition methodologies in order to guarantee the reproducibility of the structural and electrical properties of both materials.

2.1.1. Atomic layer deposition (ALD)

The atomic layer deposition (ALD) technique is a variation of Chemical Vapor Deposition (CVD) based on saturated, self-limiting and separated reactions. ALD was first discovered and developed under two different names; molecular layering (ML) since the 1960s in the Soviet Union and atomic layer epitaxy (ALE) since 1974 in Finland [1]. The ALD growth is typically achieved by using two gaseous precursors, where the material growth occurs in a layer-by-layer fashion through separated surface reactions on a substrate. This deposition method was used to realize the zinc oxide thin film composing the piezotronics junctions of this work.

A typical ALD cycle using two gaseous precursors (named A and B) consists in four steps, as illustrated by Fig. 2.1:

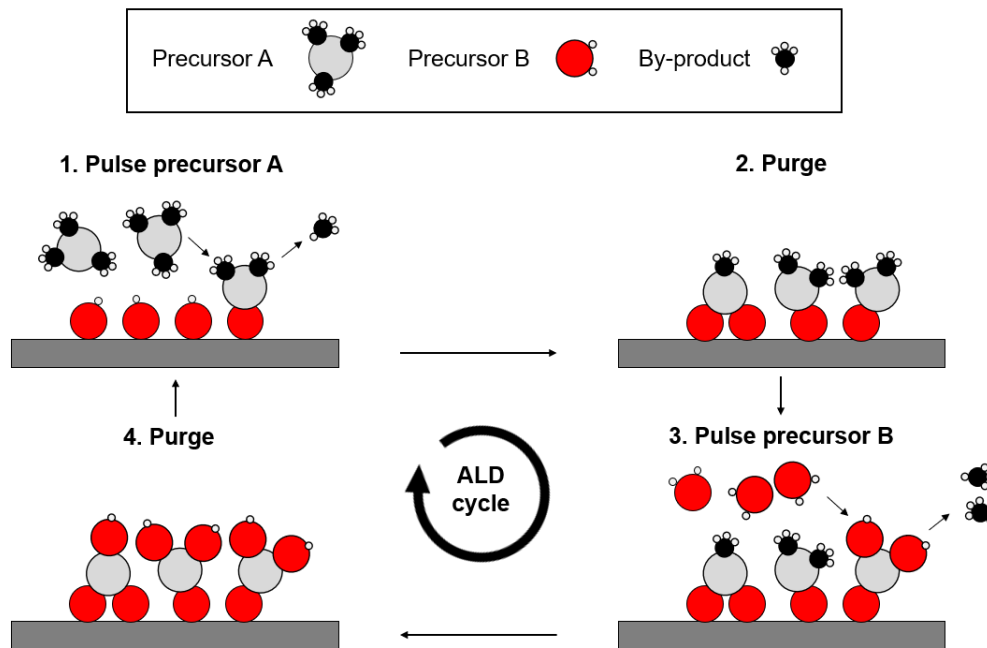


Figure 2.1. Schematic representation of a typical ALD cycle.

1. The pulsing of precursor A, resulting in the first chemisorption.
2. A first purge with an inert carrier gas allowing the removal of unreacted precursor A and reaction by-products.
3. The pulsing of precursor B, resulting in the second chemisorption.
4. A second purge, allowing the removal of unreacted precursor B and reaction by-products.

The gaseous nature of the precursors used in the ALD reactor, combined with the self-limiting nature of the surface reactions give ALD the unique ability to deposit thin films with a thickness control at the atomic layer level. For every pulse of a given precursor, a monolayer is added on the substrate surface, which results in the uniform deposition of thin films with excellent conformality, allowing the coating of complex architectures with high aspect ratio as MEMS structures [2] as illustrated on Fig. 2.2.

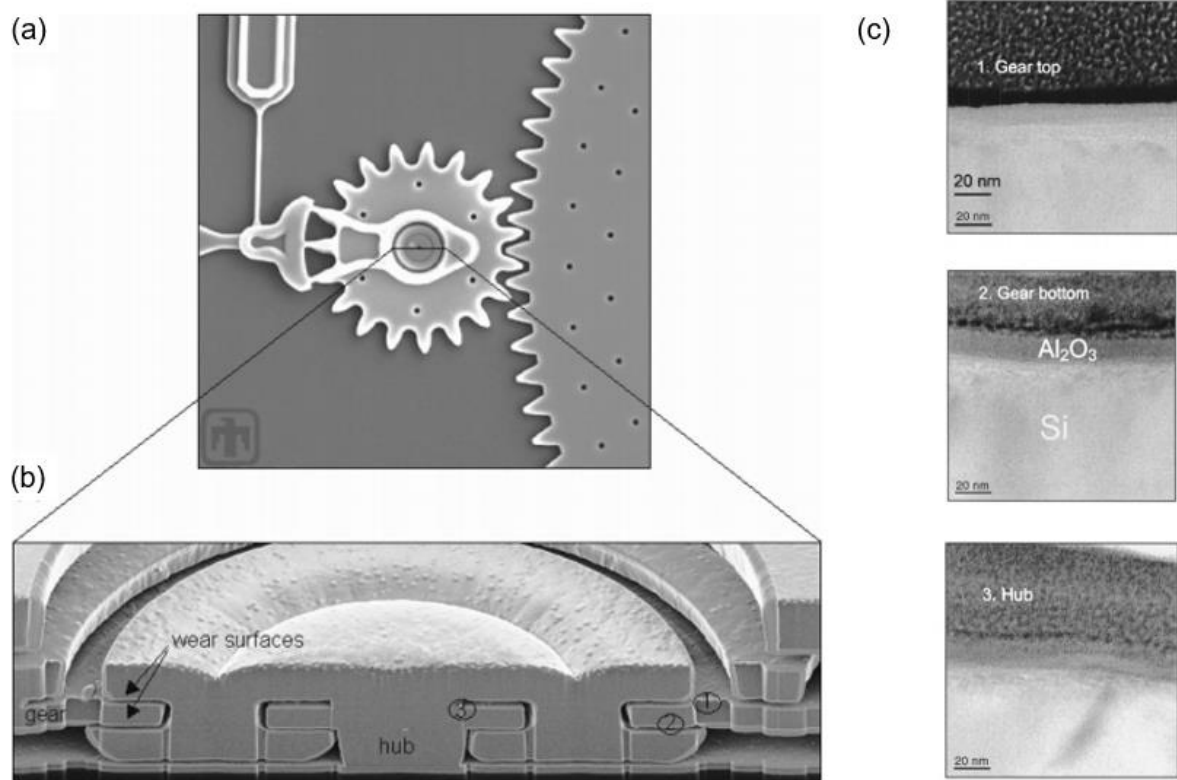


Figure 2.2. Conformal coating of Al_2O_3 thin films by ALD deposited on Si MEMS microengine structure. (a) MEMS microengine consisting of a gear turning on a hub. (b) Cross section of the hub showing the contact surfaces between the gear and the hub, as well as the buried channel inside the hub. Locations denoted from 1 to 3 are examined by transmission electron microscopy (TEM). (c) Corresponding TEM cross sections showing the conformal Al_2O_3 coating achieved by ALD. Reprinted from [2].

Moreover, ALD depositions can be realized at low temperatures [3], making it compatible with challenging substrates, i.e. brittle, flexible or polymeric substrates. Owing to these outstanding features, a wide variety of materials have been developed and made compatible with the ALD technique, including metallic oxides, noble metals, nitrides, carbides, fluorides, sulfides or phosphates, as summarized in Fig. 2.3.

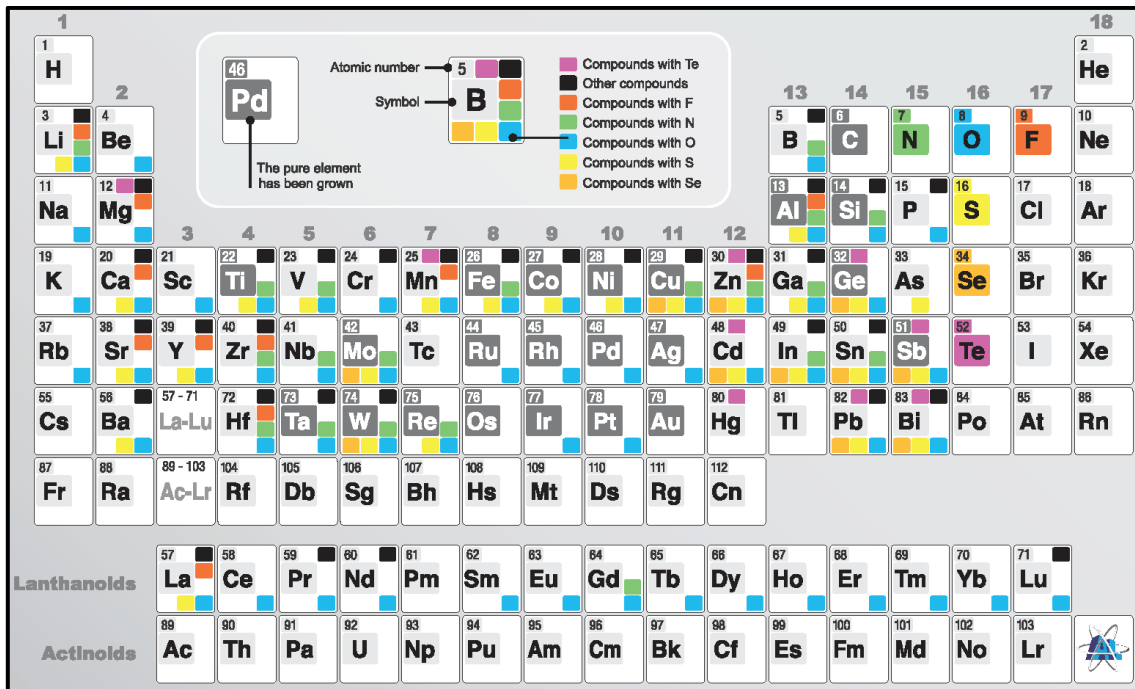


Figure 2.3. Overview of the materials prepared by ALD. The growth of pure elements as well as compounds with either tellurium (Te), fluorine (F), nitrogen (N), oxygen (O), sulfur (S), selenium (Se) or other compounds is indicated via different colour shadings. Reprinted from [4].

The growth rate is expressed as the thickness deposited for every ALD cycle, and is called growth per cycle (GPC), in units of Å/cycle or Å/loop. Due to the steric hindrance of the ALD precursors, the GPC is inferior to an atomic monolayer of the deposited material and thus depends strongly on the nature of the reactants. Furthermore, the deposition temperature has a critical influence on the GPC, as illustrated in Fig. 2.4.

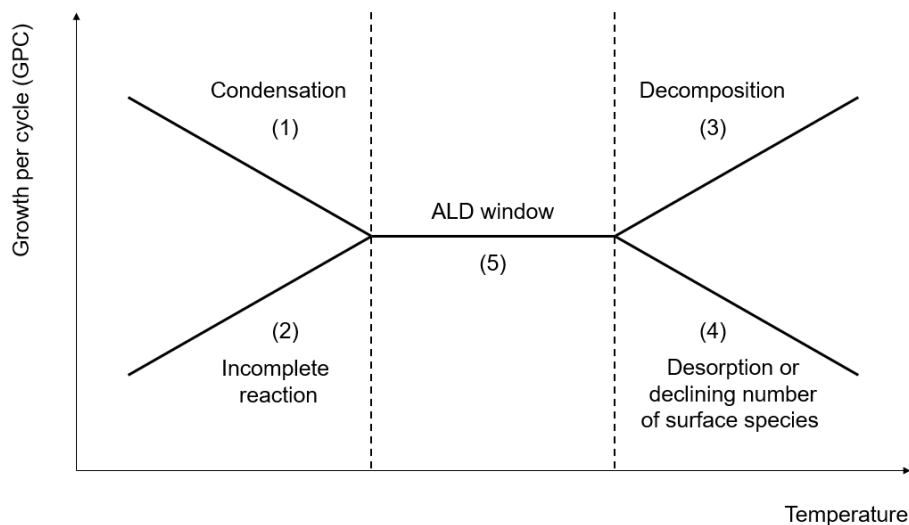


Figure 2.4. Relation between the growth per cycle (GPC) and the deposition temperature.

Five different situations can be identified, referring to the different regions in Fig. 2.4.:

- Region 1: at low deposition temperatures and for decreasing values of the GPC, where more than a single monolayer is adsorbed due to condensation, resulting in non-saturating reactions.
- Region 2: at low deposition temperatures and for increasing values of the GPC, where the reaction is limited by its activation energy, and/or the kinetics of the reaction is too long compared to the cycle time performed.
- Region 3: at high deposition temperatures and for increasing values of the GPC, linked with the decomposition of the precursor on the substrate's surface before reacting with the second precursor.
- Region 4: at high deposition temperatures and for decreasing values of the GPC, linked with the desorption of the precursor or to a decreasing density of surface species with which to react.
- Region 5: a range of temperature with constant GPC values, called the "ALD window", where the growth rate is independent of the temperature and is determined by the density of surface species available and the steric hindrance of the precursor.

Moreover, the pulsing and purging times are the main components of an ALD cycle. The pulsing time should be long enough to allow the surface saturation of the precursor with the surface species. Similarly, the purging time should be long enough to evacuate the entirety of the reaction by-products, as well as to avoid both precursors from mixing and reacting in the gaseous phase.

Within the frame of this work, we used a commercial ALD reactor (TFS-200, Beneq, Finland) in a thermal configuration for the deposition of ZnO thin films, as shown in Fig 2.5. The samples are transferred from a load-lock located inside the cleanroom facilities to the reaction chamber, in order to avoid any surface contamination. The details concerning the ZnO thin films deposition by ALD are provided in Chapter 3.

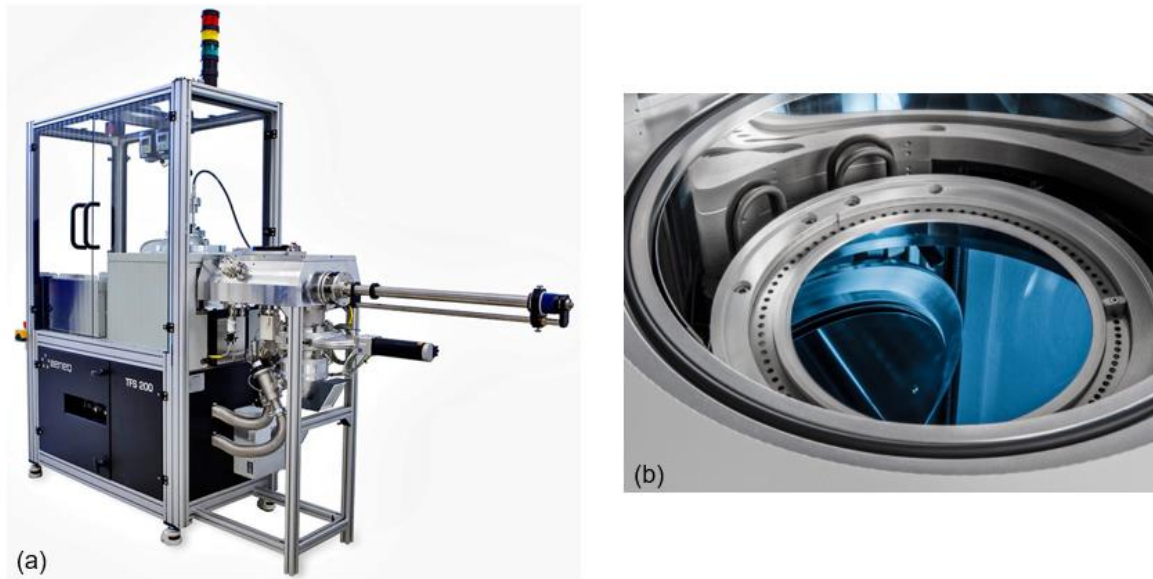


Figure 2.5. (a) ALD equipment (Beneq TFS 200) used for this study. (b) Close-up on the ALD reaction chamber with a 8 inches coated silicon wafer inside. Reprinted from [5].

2.1.2. Electron beam metal evaporation (EBME)

The electron beam metal evaporation (EBME) technique consists in the evaporation of a source material using high energy electrons focused as an intense beam. This equipment was used to deposit the thin metal films composing the metal electrodes of the piezotronics junction of this work. A tungsten filament is used with high applied voltages, causing the thermionic emission of electrons unified as a beam by a strong magnetic field. The electron beam is accelerated to a high kinetic energy towards the crucible containing the material to be deposited. The energy of the electron beam is then transferred to the source material as thermal energy, leading to its evaporation. Consequently, the evaporated material traverses the vacuum chamber to coat a substrate. The deposition takes place in ultra-high vacuum conditions (i.e. between 10^{-8} and 10^{-7} mbar), in order for the mean free path to be longer than the distance between the electron beam source and the substrate. The deposited thin film thickness is measured *in situ* by quartz crystal balance monitoring. Thin films deposited by EBME typically present a columnar morphology [6]. This technique is particularly suited for the deposition of Schottky metallic contacts, owing to the low pressures ensuring a high purity of the deposited material. Additionally, the evaporated metallic atoms do

not possess a high kinetic energy (i.e. inferior to 1 eV [6]), which results in little or no migration once deposited on the substrate. The resulting metallic coatings by EBME thus present a lower grain size when compared to sputtering, where the metallic particles are sputtered at a higher kinetic energy [7]. Furthermore, the water cooling of the crucible confines the electron beam to the source material, which effectively eliminates any unwanted contamination from its vicinity. The EBME technique is particularly interesting when integrated into a microfabrication process due to the directionality of the deposited material, as compared to a conventional deposition realised by sputtering. This comparison is further extended with ALD, as illustrated by Fig. 2.6.

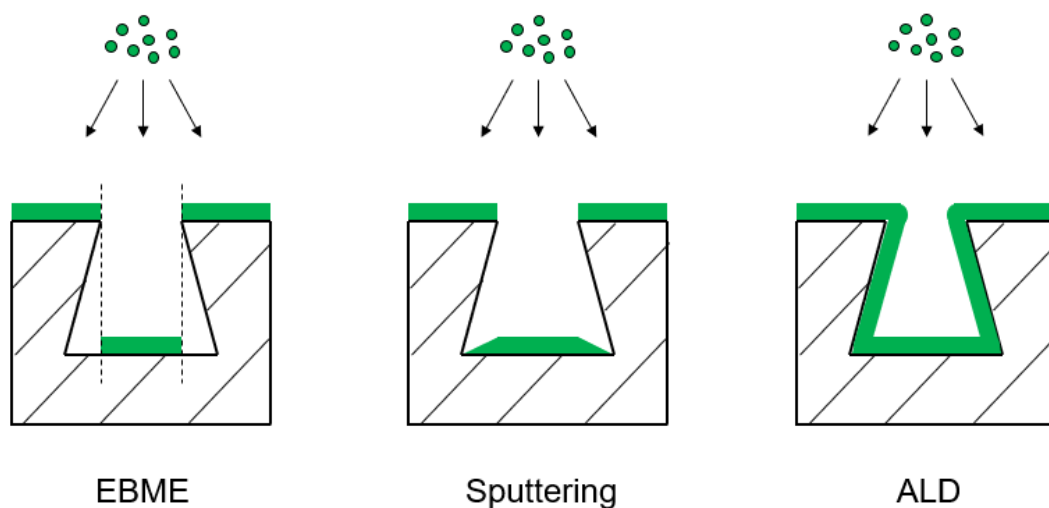


Figure 2.6. Conformity of EBME compared to sputtering and ALD. The green layer represents a given material deposited by these techniques.

The directionality of the EBME technique allows for an easier patterning of the deposited metal electrodes via a lift-off process. Further details will be provided in the section 2.2.1.

Within this scope, the EBME technique (E-gun Meca2000, France) was used in this work for the deposition of platinum and gold metal electrodes (200 nm), acting as one of the building blocks for the M-S Schottky junctions. Prior to that, an additional titanium thin film (5 nm) was deposited on the polyimide substrates to promote the adhesion of

the Pt metal electrodes. The depositions were typically realised in the 10^{-8} mbar range, with a deposition rate of $1 \text{ \AA}\cdot\text{s}^{-1}$.

2.2. Thin film microfabrication, patterning and integration techniques

The microstructuring of the dielectrics thin film and the metal electrodes will shape the functionality of the piezotronics sensors. We applied the methodologies from microfabrication with standard stages of processing adapted to the peculiar materials stacking of our devices made of inorganic thin layers and flexible organic substrate.

2.2.1. Spin-coating

The spin-coating technique is used to deposit uniform thin films from few nanometers up to several micrometers thickness scale, where the material to be deposited is contained within a solvent. It is typically used in microfabrication processing for the deposition of photo-patternable polymer layers, i.e. photoresists, as etching masks, shadow masks, sacrificial layers, or as an encapsulating layer. The main steps of the deposition process are illustrated in Fig. 2.7(a). This technique is operated with a substrate mounted on a rotating chuck, maintained flat with applied vacuum. The rotational speed is typically in the thousands of revolutions per minute (rpm) range. When the chuck starts rotating the dispensed solution spreads on the substrate's surface due to centrifugal force, while the excess resist is spun off the edge of the substrate. This results in an uniform deposition, linked with viscous force and surface tension. Part of the solvent is evaporated from the resist thin film after deposition. Typical values of the residual solvent concentration are between approximately 10% for thin resists, to 35% for thick resists [8]. The thickness of the spin-coated material is mostly determined by the spin speed and the solution viscosity, as illustrated by Fig. 2.7(b). The spin time depends on the viscosity of the applied resist, as only a few seconds are necessary for the thinner resists while tens of seconds might be required for thicker, viscous resists. The initial acceleration usually only lasts a few seconds to reach the desired speed, which is then maintained at a constant value. Furthermore, a two-step approach is often used for the spin coating of photoresists [8]. A low speed

below 1000 rpm is first applied during a few seconds to distribute the resist on the surface's substrate, which is followed by a high acceleration above 1000 rpm/s towards the desired spin speed. This leads to a better substrate coverage and limits the apparition of cracks on the spin coated resist. The cleanness, and sometimes the chemical activation of the substrate is also an important point to control in order to insure the uniformity and the adhesion of the spin coated photoresist on top.

Within the frame of this project, several photoresists (positive and negative tones) were deposited by spin-coating, including LOR3A, S1813, SU-8, and SX AR-P 3500/8. These photoresists were used for different purposes (i.e. patterning/etching masks, encapsulating layer, cantilever body) which will be detailed in Chapter 4 and 5.

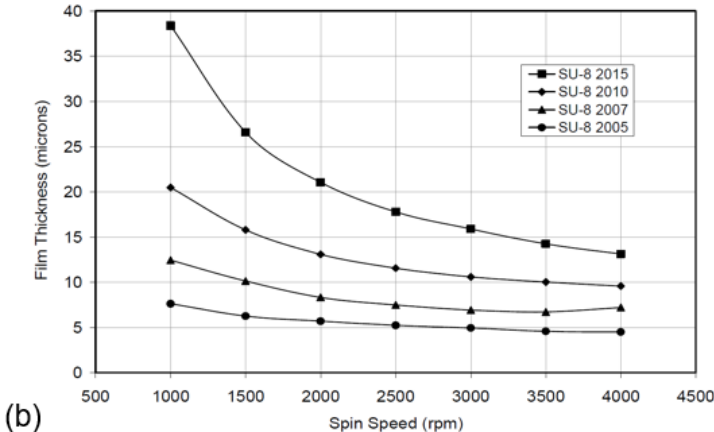
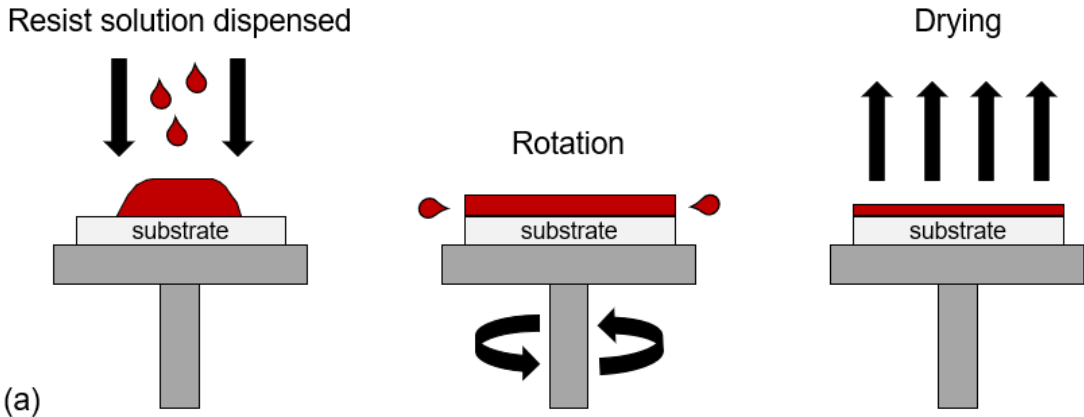


Figure 2.7. (a) Schematic diagram illustrating the main steps of the spin-coating method. (b) Film thickness vs spin speed curve used for thickness determination of SU-8 photoresist. The curves in the graph correspond to different viscosities of the SU-8 photoresist, as referenced by the legend. The part (b) of this figure is reprinted from [9].

2.2.2. Maskless photolithography

Photolithography can be described as the transfer of a pattern to a photosensitive material via a selective exposure to a radiation source, such as UV light. This technique is particularly adapted for MEMS microfabrication as it allows for the patterning of materials up to the hundreds of nanometers scale. As a light-based technique, the resolution of photolithography is limited by the wavelength of the light used, as stated by the Rayleigh criterion [10]. Typical resolutions achieved by photolithography techniques are now in the hundreds of nanometers range [11]. The photosensitive materials used are typically photoresists which experience a change in their properties when exposed to a UV light. Subsequently, the resist is placed in a developer solution, which will etch away the exposed or unexposed area, depending on the nature of the photoresist. There are two different types of photoresists, i.e. positive and negative tone photoresists. Their difference is illustrated in Fig. 2.8. Positive photoresists experience a change in their chemical structure when exposed to a UV light, and thus become more soluble in the appropriate developer solution. Consequently, only the exposed areas of positive photoresists are etched away by the developer, while the unexposed areas remain intact. On the opposite, negative photoresists exposed to UV light become polymerized (i.e. cross-linked) and are thus not dissolved by the developer solution, while their unexposed areas are removed by the developer.

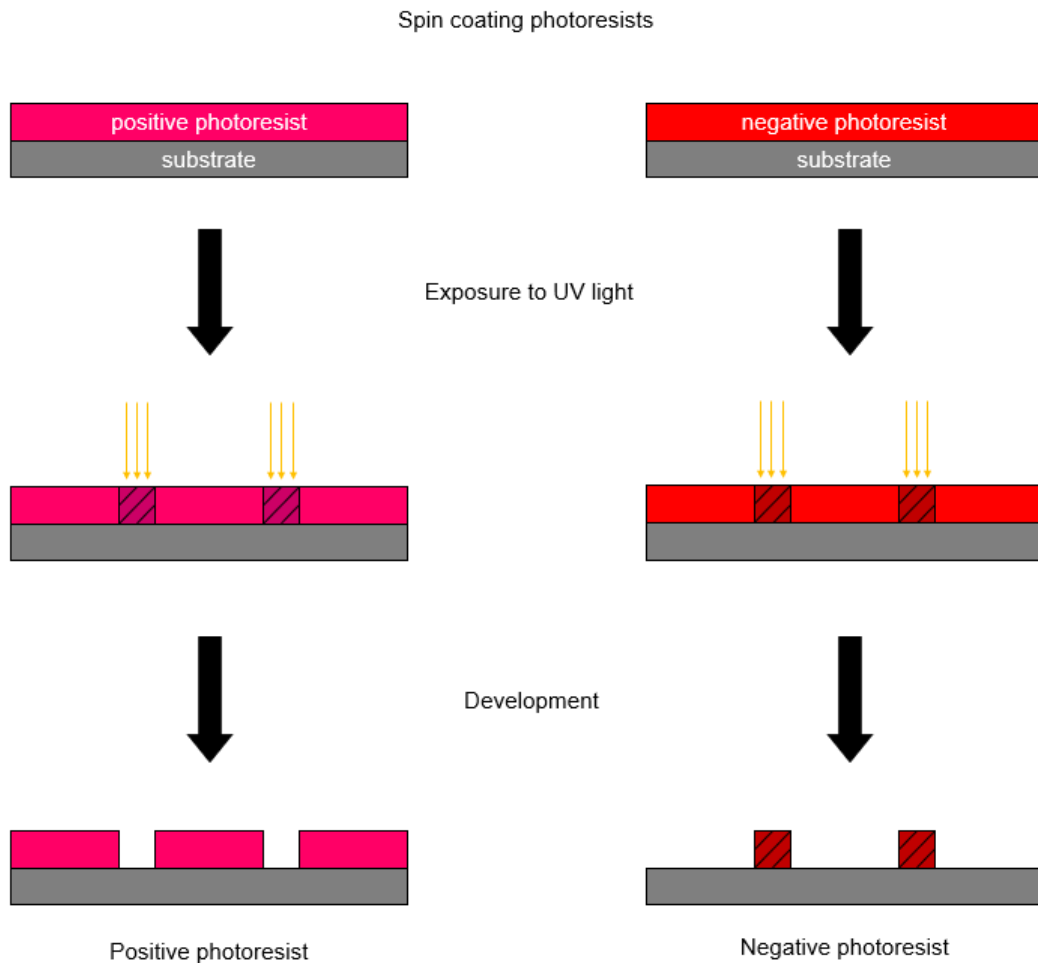


Figure 2.8. Schematic illustrating the difference between a positive and a negative photoresist during their exposure and development processes.

Within this context, the maskless aligner (MLA) technology was developed in the 2000's [12] part of the new generation of direct write lithography tools. No photomask is needed as a computer-aided design (CAD) layout is directly exposed onto the photoresist covering the processed substrate by the mean of a UV laser. Any design change can thus be simply and rapidly implemented by modifying the CAD layout. On the contrary, traditional photolithography is performed with a UV lamp and a mask aligner allowing faster UV exposure of few seconds of the pattern. But this later methodology of lithography requires the manufacturing of a photomask, resulting in delays of several days for any change made in the design or in the microfabrication process. The difference between both techniques is illustrated in Fig. 2.9.

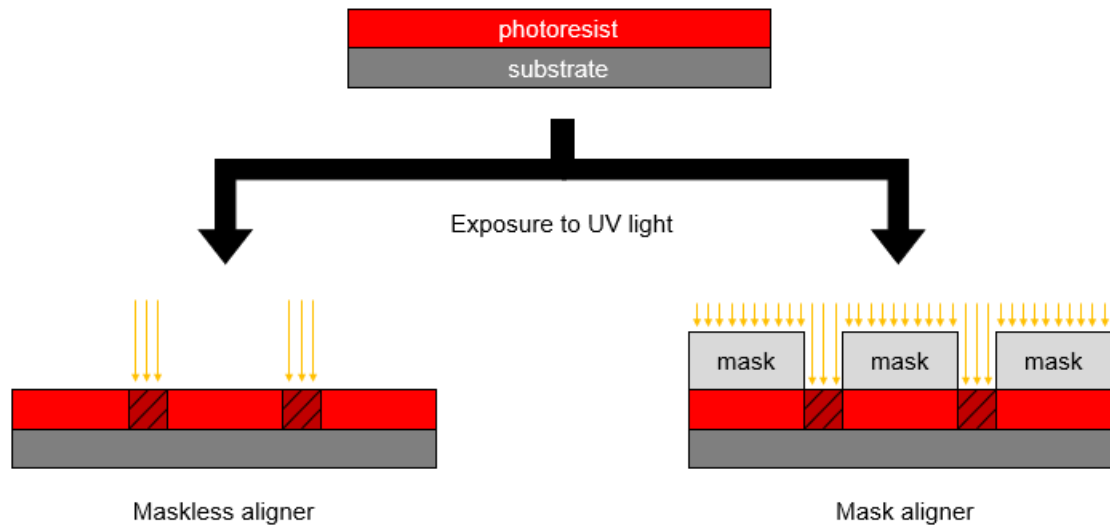


Figure 2.9. Schematic illustrating the difference in the exposure process performed without and with a mask aligner.

The use of direct writing by maskless photolithography thus allows for more flexibility in terms of research and developments of new process and a substantially shorter prototyping cycle. On the other hand, photolithography by mask aligner is more adapted to industrial processing and mass production by fixed and secured processes.

Maskless photolithography makes use of a spatial light modulator (SLM) to project the design directly onto the surface of the wafer [13], as shown in Fig. 2.10.

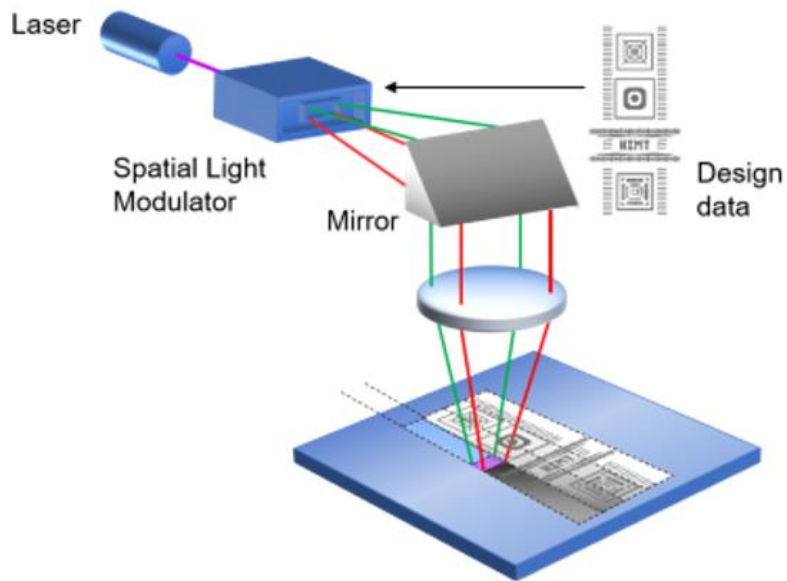


Figure 2.10. Schematic illustrating the working principle of maskless photolithography. Reprinted from [13].

The SLM is used as a programmable mask, where the CAD is divided in a matrix consisting of several individual frames. These frames are then projected by the optical system directly onto the photoresist, in a frame-by-frame fashion, while the substrate is moving accordingly. The writing time (i.e. the duration of the exposure) depends on the total area of the exposed layout as well as on the photonic dose, expressed in $\text{mJ}\cdot\text{cm}^{-2}$. As these systems are equipped with a laser having a defined wavelength, the SLM tunes the writing time to meet the appropriate dose on every frame.

The typical processing of a photoresist follows a standard protocol including several distinct steps, as illustrated by Fig. 2.11. in the case of a negative photoresist such as SU8:

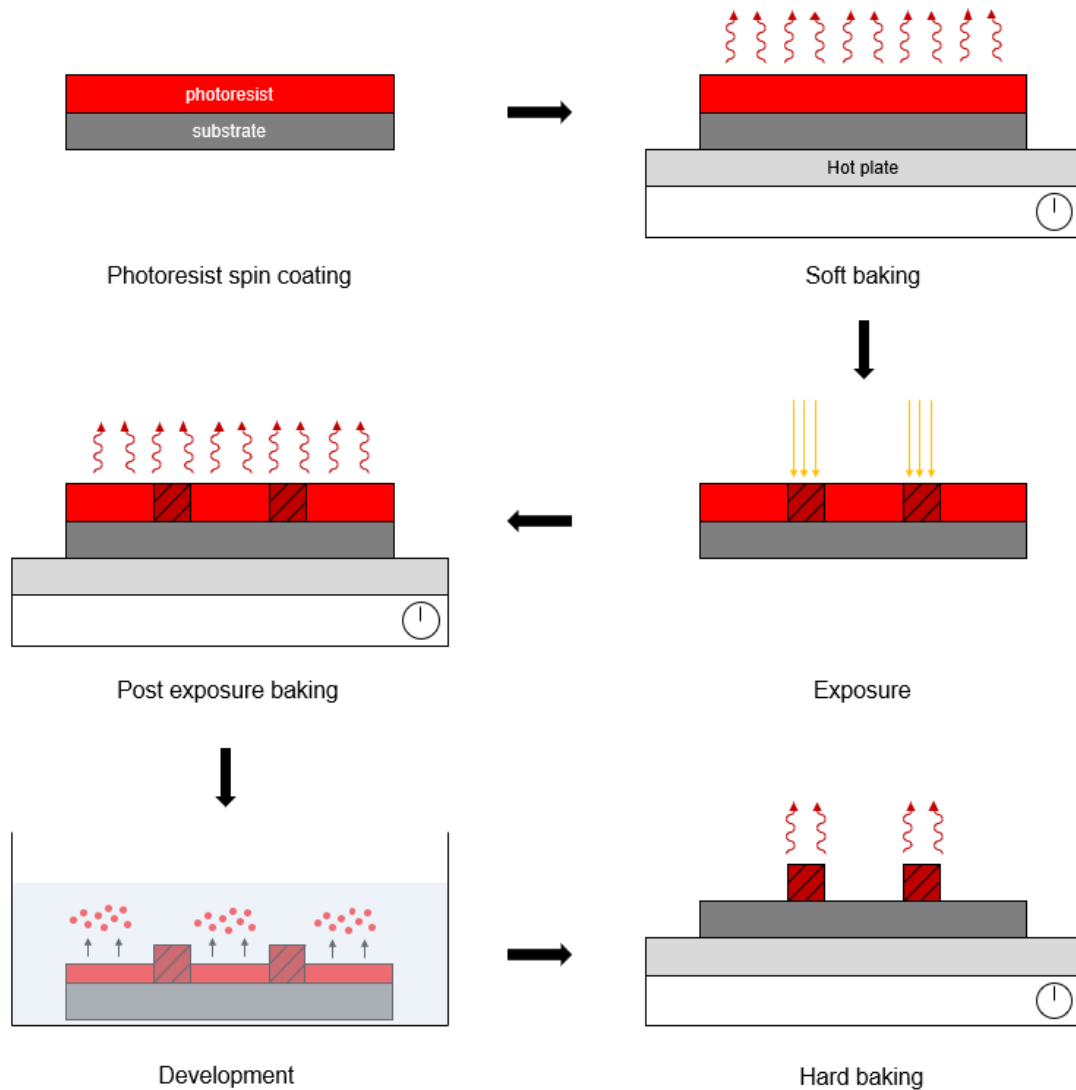


Figure 2.11. Schematic illustrating the standard protocol for a given negative photoresist processing used in photolithography.

- The first step involves the spin coating of the photoresist on a substrate (typically a silicon wafer), as described within the previous section.
- This is followed by soft baking, where the photoresist is heated at both a defined temperature and duration. This is a crucial step in the photoresist process, where the remaining solvents are removed from the photoresist. If the soft bake temperature is too cool or its duration too short, a significant amount of solvent might remain in the photoresist, which could cause a decrease in the adhesion of the photoresist to its substrate. Contrariwise, if the temperature is too high or

the duration too long, thermal cross-linking might occur during the bake, which leads to a decrease of the development rate.

- Subsequently, exposure is selectively performed on defined areas of the photoresist by the mean of UV light.
- The post exposure baking is taking place directly after the exposure. While the exposure is initiating the polymerization of the photoresist, the post exposure baking brings energy in the form of heat for the cross-linking mechanism to extend to the entirety of the material.
- Development is then performed by immersing the photoresist and its substrate in a developer solution, where the non-exposed areas of the photoresist are etched away by the developer.
- Finally, a hard baking can be realised to improve the physical (i.e. stress relieving), chemical and thermal stability of the photoresist for further processes, as well as to improve its adhesion on the substrate's surface.

The different temperatures and durations corresponding to each bake described in this protocol must be carefully adapted and optimized for every single photoresist used.

Furthermore, lift-off is a common technique performed in microfabrication processes consisting in the selective deposition of a thin film material (e.g. metal, dielectric, nanowire bundles) on a given substrate using photoresists to shape it into tracks. More precisely, a bi-layer is used with two resists presenting different properties, as shown in Fig. 2.12.:

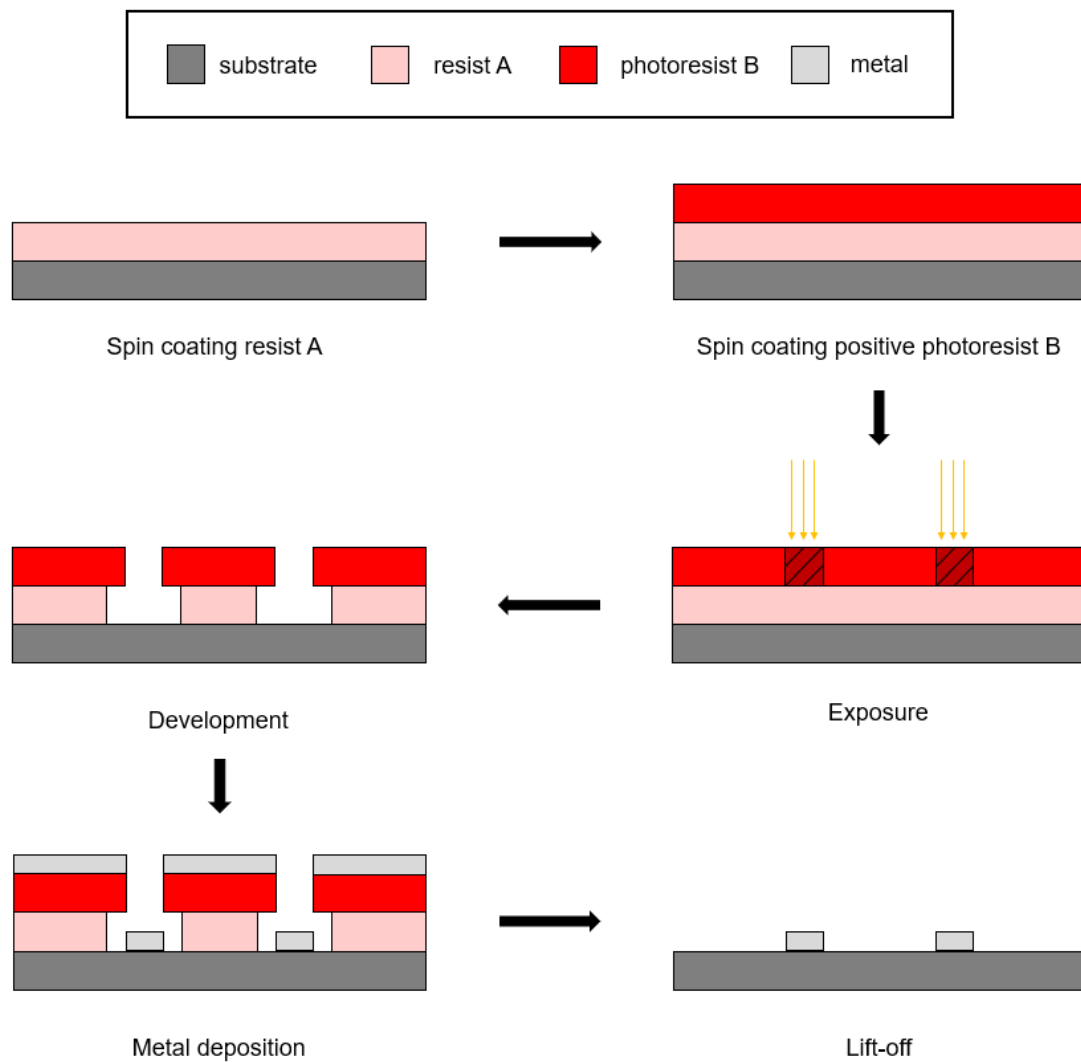


Figure 2.12. Schematic illustrating a standard lift-off process using a resist bi-layer.

A first, non-photosensitive resist is spin coated on the substrate and baked. Subsequently, another positive photoresist is spin coated and baked, which results in a bi-layer on top of the substrate. The positive photoresist is then selectively exposed on defined areas. The following development of the resists is the critical step of this process. As previously explained, the positive photoresist on top of the bi-layer will be etched by the developer solution on the areas where it has been exposed. However, the underlying resist will be etched away isotropically, i.e. on the depth of the corresponding exposed areas as well as on the sides of these areas. This results in an undercut, whose length is controlled by the duration of the development. The metal is then deposited on the uncovered areas of the substrate as well as on the non-exposed

areas of the positive photoresist. The use of EBME for the metal deposition is highly recommended due to its high directionality as described in the previous section. This avoids the deposition of metals on the sidewalls of the underlying resist, which facilitates the subsequent removal of the resist. Finally, the resist is stripped away with an appropriate solvent solution, where the undercut greatly facilitate the access of this solution to the underlying resist. The metal thus only remains on the areas where the positive photoresist had been exposed.

Within the frame of this work, a maskless aligner (MLA150, Heidelberg Instruments, UV wavelength of 375 nm) has been used for this work, represented in Fig. 2.13. The different microfabrication processes performed as well as details on the resists used and their corresponding processing will be given in chapters 4 and 5.

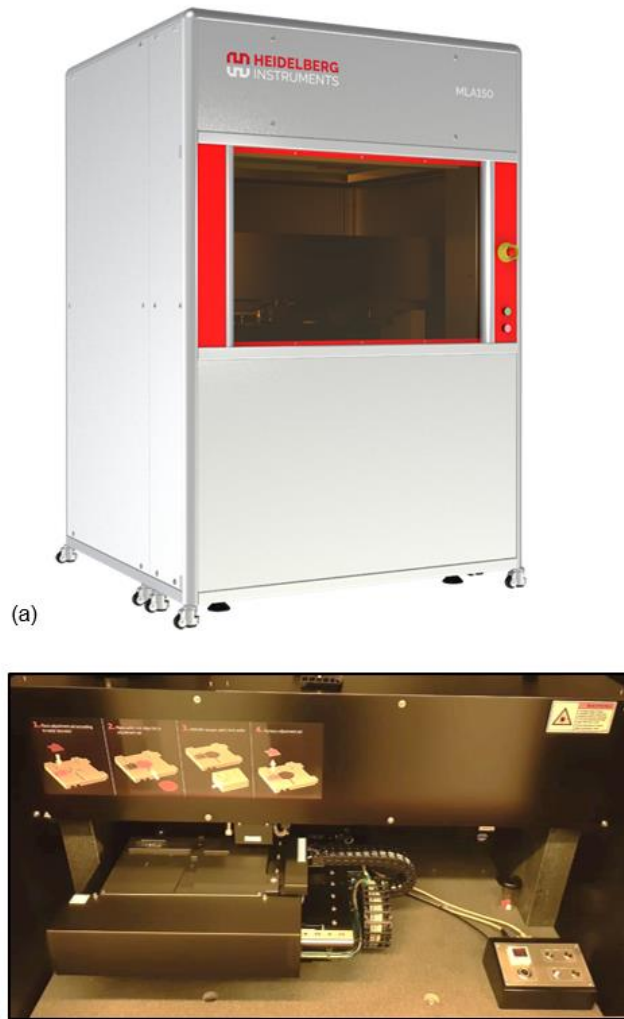


Figure 2.13. (a) Maskless aligner (MLA150, Heidelberg Instruments) used for this study. (b) Stage system with optics plane. The part (a) of this figure is reprinted from [14].

2.2.3. Reactive ion etching (RIE)

The reactive ion etching (RIE) process consists in etching substrates or thin films, where a plasma process is performed in a low-pressure chamber via the discharge/excitation of radicals and ionic species with radiofrequency power. However, this technique can be used for a different purpose, i.e. to perform a plasma pre-treatment on a given substrate's surface. The aim of this pre-treatment is to increase the surface wettability by introducing chemical moieties (e.g. hydroxyl, carboxyl, carbonyl), which effectively prepares the surface for any subsequent coating. This leads to an improved adhesion, wettability and surface coverage between the pre-treated substrate and the deposited material. An additional goal is to remove organic contaminants from an inorganic substrate's surface.

Argon (Ar) and oxygen (O₂) are the two most common gases used to perform such plasma treatments. More precisely, the argon (Ar) plasma is commonly used to activate the substrate's surface via the bombardment of Ar ions or atoms, which removes organic contaminants by physical ablation. The oxygen (O₂) plasma treatment is performed to clean the substrate's surface owing to its ability to eliminate organic contaminants via chemical reactions with the oxygen radicals. Moreover, oxygen is commonly used for the activation of polymeric substrates, where the oxygen is reacting with carbon chains to induce hydroxyl (OH) groups at the polymers' surface [15]. Alternatively, a mixture of Ar and O₂ can be used for surface pre-treatment, consisting in a combination of physical ablation performed by the argon gas and chemical reactions for increased wettability with the oxygen gas.

Within this scope, plasma treatments were performed prior to the ZnO and Pt thin films depositions, to increase the surface activation and wettability on their respective substrates. Thus, the adhesion of the platinum metal electrodes deposited by EBME to the polyimide substrate was improved using an Ar:O₂ plasma activation for a few seconds prior to metal evaporation [16]. Similarly, prior to the deposition of ZnO by ALD, a plasma pre-treatment was applied on the sensors' surface (i.e. on both polyimide and Pt), consisting in a soft oxygen/argon plasma.

2.2.4. Wet etching

Wet etching is a selective material removal process making use of liquid chemicals or etchants. The material to be removed is deposited on a substrate and reacts with the etchants when immersed into the liquid etchant solution, usually following reduction-oxidation reaction. The wet etching is mainly controlled by two variables:

- The etching rate, which depends on the etching solution concentration and the temperature applied during the etching process. The increase of these parameters both contribute to an increase of the etching rate [17,18]. Additionally, magnetic stirring for agitation of the etching solution is also used to improve the etching rate, to a minor extent.
- The etching time, i.e. the duration for which the sample is immersed in the etching solution.

The material to be removed can be either completely etched, or etching masks making use of photoresists might be used to selectively etch a given material on the non-covered areas. As most of the materials are being etched isotropically (i.e. uniformly in all directions), a common problem in wet etching processes is related to the apparition of under etching below the photoresists, as illustrated in Fig. 2.14. Within this scope, special attention should be given to the sizing of the etching masks, in order to anticipate the apparition of under etching.

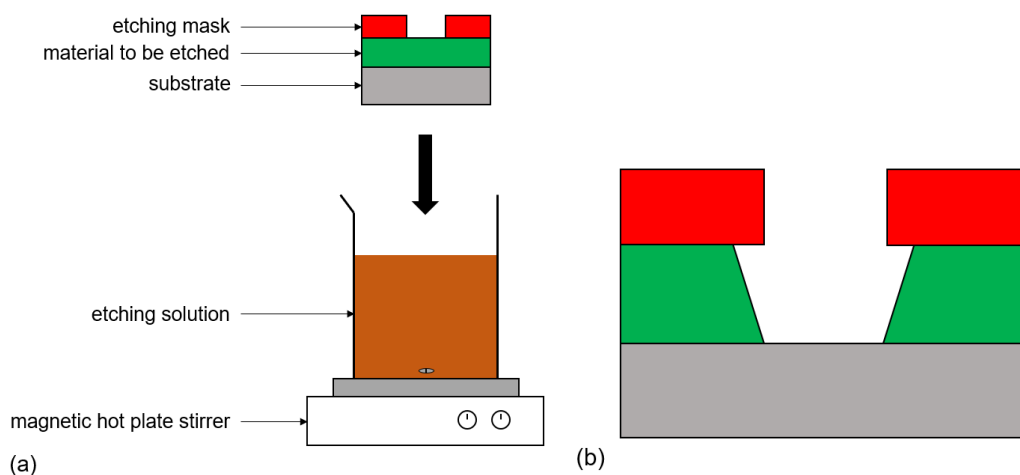


Figure 2.14. (a) Schematic representation of the experimental setup prior to wet etching. (b) Details on the sample stack after wet etching, highlighting the appearance of under etching below the photoresist.

Furthermore, wet etching can be performed for the releasing stage of MEMS structures by the mean of a sacrificial layer. The whole structure is thus sequentially built upon the sacrificial layer, which involves a different approach in the microfabrication process. As the structure is released at the last stage of the microfabrication process, the sacrificial layer must be selectively etched without affecting the supporting structure integrity and the material's properties.

Wet etching has been used for the selective removal of ZnO thin films using a FeCl_3 740 mmol solution. The samples were etched during 2 minutes at room temperature with a 400-rpm magnetic stirring agitation using a magnetic stirrer (RH series, IKA). More details are provided in the Chapter 4 related to the deposition and shaping of zinc oxide thin layer. Additionally, wet etching was employed with a FeCl_3 solution for releasing of the microsensors chip polymeric body and cantilevers structures by the mean of a copper sacrificial layer. More details are provided in the Chapter 5.

2.2.5. Wire bonding

The wire bonding technique allows the interconnexions between the small metal electrodes of the microdevices and the metal pads of an external casing or a PCB (printed circuit board) to establish an electrical communication of the different signals with an external instrumentation. This technique is based on the ultrasonic bonding method, which is a type of friction-based welding, not to be mistaken with a process using high temperatures to melt two metals together. The wire to be connected to the substrate is pressed onto its surface, while being moved laterally. There are three parameters controlling the ultrasonic wire bonding process, i.e. the ultrasonic power, the force and the time:

- The ultrasonic power determines the vibrational energy transferred from the tip (i.e. capillary) to the wire and is a key factor for a successful bonding. More precisely, a too low value of the ultrasonic power would result in a weak bond, while a too high value could damage the substrate.
- The force is aimed at supporting the plastic deformation, it controls the amount of mechanical force applied on the wire.

- The time sets the time period where both the ultrasonic power and force are applied during a given bonding cycle.

These three parameters are intrinsically correlated and need to be optimized in order to find an optimal process window to achieve a reliable bond, both in terms of mechanical and electrical performances. Additionally, temperature can be introduced as a fourth parameter in the case of gold wire bonding. The temperature can effectively alter the bonding strength and ultrasonic transmission and leads to a better bond quality when increased to moderate temperatures [19].

Within the frame of this work, after the completion of the microfabrication process, the platinum metal electrodes of the sensors were connected to a printed circuit board (PCB) via wire bonding using a thermosonic wirebonder (TPT HB16, Accelonix, the Netherlands). A ball bonding process was performed at a temperature of 50 °C, with gold wires of 25 µm diameter. The ball bonding bond is performed on the platinum metal electrodes located on the sensors, while the second bond (i.e. wire tail) is realized on gold pads located on the PCB. The ultrasonic generator is providing a constant frequency value of 62 kHz applied until the bonding is completed. The values of the parameters used to perform these bonds are detailed on Table 2.1.:

Parameters	Bond 1 - to platinum electrodes of the chip with the sensor device	Bond 2 - to gold pads of the PCB
Ultrasonic power (mW)	550	350
Time (ms)	300	275
Force (mN)	400	250

Table 2.1. Details of the parameters used to perform the wire bonding between the sensor and the PCB.

Most notably, the ultrasonic power as well as the force applied to the first bond for the ball bonding had to be substantially increased compared to standard values in order

to perform a reliable bond. This is linked to the fact that the 200 nm thick platinum metal electrodes are deposited upon a flexible polyimide substrate, dissipating a part of the applied force.

Furthermore, prior to the wire bonding, a plasma activation (100 W, 2 minutes, in Ar:O₂ gases environment at 100 mTorr) was performed on the mounted sensors to improve the metal-to-metal adhesion [20]. This realization of this plasma treatment should not be neglected as it improved considerably the reliability of the bonds.

A so-called double reversed loop [21] has been used to perform the bond bonding between the platinum metal electrodes of the sensors and the gold pads of the PCB. The double reversed loop led to a higher repeatability of the performed bonds when compared to a basic loop where the wire is only pulled vertically and stretched until the second bond location. This loop is characterized by a curved shape, as shown in Fig. 2.15. This loop ensures a stable connection by lowering the tension between the ball and the wire. Additionally, this geometry is particularly suitable for structures presenting a height gap between the metals to be bonded. This applies in our case as there is an approximate 170 μm height gap (i.e. thickness of the polyimide substrate and the double-sided polyimide used to stick the sensors to the PCB) between the platinum electrodes on the sensors and the gold pads on the PCB.

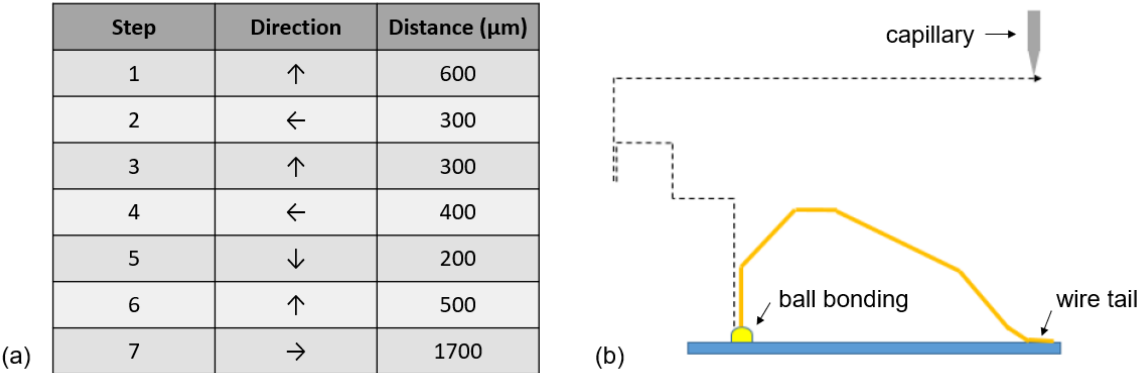


Figure 2.15. (a) Table detailing the different steps performed to realize the double reversed loop structure, with the corresponding directions and distances. (b) Schematic of the capillary movement with the corresponding wire shape obtained. Adapted from [21].

2.3. Characterization techniques

2.3.1. Ellipsometry

Spectroscopic ellipsometry is an optical, non-destructive method, used to measure the change in polarized light upon transmission or reflection through a material's interface of interest, where the wavelength is scanned over a broad range. Ellipsometry measures the quantities Δ and Ψ , which are both functions of the wavelength. Furthermore, the polarized incident light is decomposed into the component s , which oscillates perpendicular to the plane of incidence, and the component p , which oscillates parallel to incident plane. Δ is thus defined as the change in phase difference between the components s and p , with respect to the reflected plane, while Ψ is described as their amplitude ratio upon reflection. These parameters are linked together via the following equation, which is used to calculate the reflection coefficients r_p and r_s [22]:

$$\tan(\Psi) \cdot e^{(i\Delta)} = \frac{r_p}{r_s} \quad (2.1)$$

These measured parameters are then adjusted through a fitting algorithm via experimental ellipsometric data for the determination of a material's thickness, refractive index and absorption coefficient. Thickness ranging from a few nanometers up to tens of micrometers can be determined. Within this scope, the thickness of ZnO thin film samples was estimated by ellipsometry (J. A. Woollam M2000 Ellipsometer) by measurements carried out for wavelengths between 300 nm and 1000 nm, with three different incident angles of 65°, 70°, and 75°.

2.3.2. X-ray diffraction (XRD)

X-ray based techniques are commonly used to obtain structural information about a material of interest. When applied to thin films, X-ray diffraction is a powerful tool to characterize the crystalline structure, the preferred crystalline orientations, the

crystallite size or the residual stresses of a polycrystalline material. XRD relies on the constructive interference of an X-rays monochromatic beam scattered at specific angles from each set of lattice planes in a material. This results in the obtention of a diffraction pattern, where XRD peaks are appearing at specific angles depending on the crystalline structure of the material, allowing for subsequent phase identification with online databases. More precisely, the material's interatomic distances determine the positions of the diffraction peaks, while the atomic types and positions determine the diffraction peak intensities. The grazing incidence (GI) technique is especially adapted for thin films characterization. It consists in applying a small angle between the incident beam and the thin film surface, which allows for a suppression of reflections from the substrate. As a result, only the thin film of interest is probed, and the penetration depth can be controlled by adjusting the angle of the incident beam.

X-ray diffractometry (XRD) (Diffractometer Bruker D8 Discover with Cu K α radiation and a 5-axis Eulerian cradle) was thus conducted in a grazing incidence configuration ($\omega=0.3^\circ$) to estimate the crystalline quality and the preferred crystalline orientation of the ZnO thin films deposited by ALD at various low temperatures deposition (i.e. between 60 °C and 100 °C), on different substrates (i.e. silicon, platinum and polyimide). Additionally, calculations of the ZnO thin films lattice parameters and internal strain calculations as a function of the deposition temperature were performed. More details are provided in the chapter 3.

2.3.3. Optical microscopy

The optical microscopy is a well-established technique using visible light together with a system of lenses to magnify images of sub-millimeter scale samples. In the case of a transmission optical microscope, the light of a source is passed through a condenser lens which focuses the light on a given sample to obtain maximum illumination. The light which passed through the sample is collected by the objective lens. A magnified image of the sample is the provided on the detector by the tube lens. The principle remains similar for reflected-light microscopes, at the difference that the light is reflected on the sample before reaching the objective lens. Optical microscopy was

mainly used in the cleanroom facilities to investigate the impact of the different microfabrication steps on the developed piezotronic sensors. It is equipped with a specific inactinic light source to check the different stages of the microfabrication process flow to prevent UV flooding exposure effect of the photoresist layer.

2.3.4. Scanning electron microscopy (SEM)

Scanning electron microscopy (SEM) is used by focusing an electron beam over a surface, where the electrons are interacting with the material's surface to investigate its topography, microstructure and its chemical composition. This technique is operated under vacuum, where electrons are created by an electron gun and accelerated down a column through a combination of lenses and apertures and focused as an electron beam. The accelerating voltage is typically in the range of a few hundred volts up to 30 kV [23]. After interacting with the surface, these electrons produce different signals in the form of secondary electrons, backscattered electrons or characteristic X-rays which are subsequently collected by an appropriate detector. More precisely, emitted secondary electrons and backscattered electrons are used for imaging the surface of a sample while emitted X-rays are used for elemental analysis via energy-dispersive X-ray spectroscopy (EDS). The interaction between the electron beam and the material's surface is illustrated in Fig. 2.16. The spatial resolution and the sample-beam interaction volume are highly correlated with the type of electrons or X-rays collected, as secondary electrons are emitted from the top few nanometers below the material's surface. This range extends to the top few hundreds of nanometers for backscattered electrons, while X-rays are collected from a much larger volume, i.e. from the top two micrometers of a given material.

The microstructure of the ZnO thin films was thus analysed by scanning electron microscopy (SEM) on a Helios 650 FIB-SEM instrument (FEI Company, USA). Cross-sectional configurations were carried out to further confirm the thickness of the ZnO thin films measured by ellipsometry.

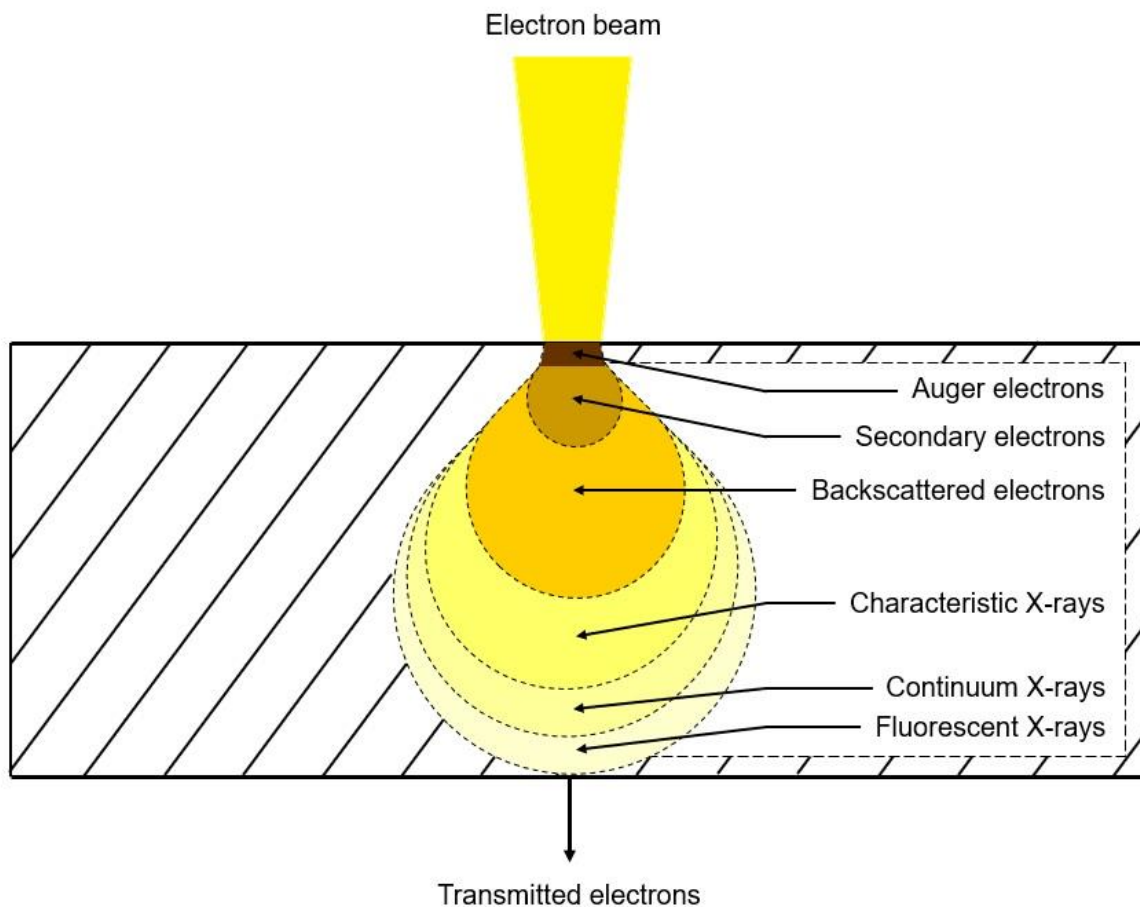


Figure 2.16. Schematic illustration of the electron beam interaction with the material's surface and the corresponding generation of electrons and X-rays.

2.3.5. Transmission electron microscopy (TEM)

The working principle of the transmission electron microscopy (TEM) is similar as the SEM in the way that a beam of electrons is focused on a material's surface. However, where SEM is using reflected or knocked-off electrons, TEM is making use of transmitted electrons passing through a material to create an image, which offers additional information about the material's bulk crystal structure and morphology. The accelerating voltage for TEM techniques is typically in the range of 40 kV up to 300 kV [23], which allows for improved resolution when compared to SEM techniques. Within this scope, High-resolution TEM (HRTEM) is used for the imaging of material's crystallographic structure down to the atomic scale. This technique is based on phase contrast, with resolutions as low as 0,05 nm achieved [23]. HRTEM has been used in

this work to investigate the morphology and elemental composition of the interface between the deposited platinum metal electrodes and the ZnO thin films. TEM investigations were carried out using a JEM - ARM 200F Cold FEG TEM/STEM operating at 200 kV and equipped with a spherical aberration (Cs) probe and image correctors (point resolution 0.12 nm in TEM mode and 0.078 nm in STEM mode).

2.3.6. X-ray photoelectron spectroscopy (XPS)

X-ray photoelectron spectroscopy (XPS) is a technique used for the determination of chemical and elemental states at a material's surface. It is conducted in ultrahigh vacuum conditions, typically in the 10^{-9} mbar range, where a beam consisting of X-rays is irradiated on the material's surface (i.e. from the outer 1 to 10 nanometers). Electrons are emitted due to the interaction of X-rays photons with atoms or molecules from the material of interest. These emitted electrons possess a characteristic kinetic energy, which is both a function of their photon energy and their binding energy. The measurement of emitted electrons' kinetic energy is thus achieved for elemental identification, as well as for the determination of atoms' chemical states and binding energies. More precisely, the binding energy depends on the element, the orbital as well as the chemical environment from which the electron has been emitted. Apart from hydrogen, XPS is thus able to identify all elements with detection limits typically in the 0.1 to 1.0 atomic percent level. However, the detection limits can be substantially influenced by the elemental matrix containing the materials to be analysed, as the detection limit can be lowered below 0.01 at.% for heavy elements in a light element matrix, or increased over 10 at.% for light elements in a heavy matrix [24]. Additionally, XPS analysis can be realized within the bulk of a material via depth profiling, where the material is etched away by an ion beam.

Elemental composition of the ZnO thin films deposited by ALD was studied by X-ray photoelectron spectroscopy (XPS) to assess their purity and check the presence of eventual contaminants. The O:Zn stoichiometry of the ZnO thin films was investigated as well. An Axis Ultra DLD (Kratos Analytical Ltd., UK) equipped with a monochromatic Al K_{α} X-ray source ($E = 1486.6$ eV) operating at 150 W was used. XPS spectra were collected at a normal take-off angle (90°) with a spot size of 110 μm . Depth profiling

was carried out with an Ar^+ ion beam operating at an accelerating voltage of 2 kV and an emission current of $100 \mu\text{A}$ (etched area = $3 \text{ mm} \times 3 \text{ mm}$).

2.3.7. Four-point probe

The four-point probe technique is used to measure the average resistance of a thin film. It makes use of four equally spaced (with a distance s), collinear probes, where a current source is applied in the two outer probes and the resulting voltage drop is measured in the two inner probes, as illustrated by Fig. 2.17.:

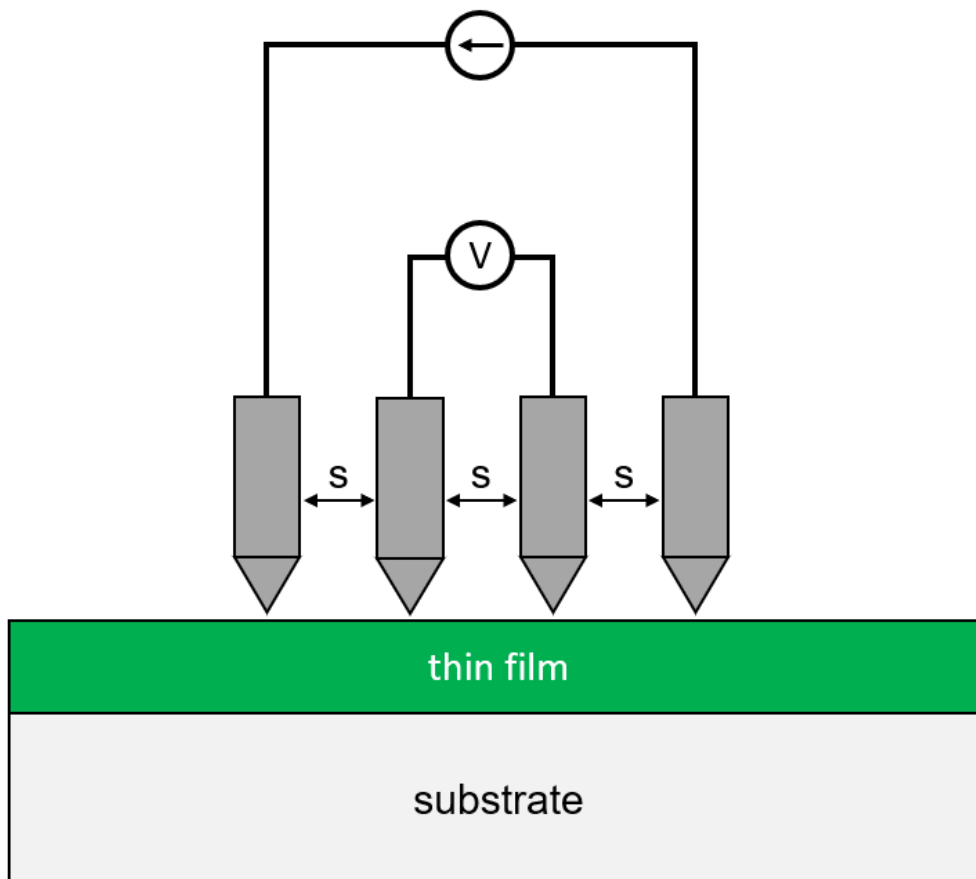


Figure 2.17. Schematic diagram of a four-point probe circuit.

One of the main advantages of the four-point probe measurements is to eliminate the contact and wire resistances from the performed measurements. The determination of the sheet resistance is based on the measurement of the four-point resistance R_{4p} .

The latter one is calculated by applying the same value of current I with opposite signs, and measuring the resulting positive and negative voltage drops, named V_+ and V_- , respectively, via:

$$R_{4p} = \frac{V_+ - V_-}{2 \cdot I} \quad (2.2)$$

The calculation of the sheet resistance R_{sh} and the resistivity ρ depend on the geometry of the sample in use. If the thickness t of the thin film to be measured is inferior to 40% of the probe interspacing s ($t/s < 0,4$), and if the sample lateral size d is superior to forty times the probe interspacing ($d/s > 40$), the following relations can be used [25]:

$$R_{sh} = \frac{\pi}{\ln(2)} \cdot R_{4p} \approx 4,532 \cdot R_{4p} \quad (2.3)$$

$$\rho = R_{sh} \cdot t \quad (2.4)$$

The resistivity of the ZnO thin films was measured by the four-point probe technique on glass substrates using a source meter (2400 Series SourceMeter, Keithley Instruments) coupled with a cylindrical four-point probe head and a probe station (Jandel Multiheight Probe Station, Jandel Engineering).

2.3.8. Current-voltage measurements (I-V)

The sensors' characteristics have been represented and investigated by performing current-voltage (I-V) measurements. They are used to allow for a better visualisation of the device's behaviour as well as to determine intrinsic material parameters by fitting the obtained characteristics by physical models. Typically, a set of bias voltage values are applied over a defined range, each measurement point being separated with a pre-defined step value. The resulting current is then plotted as a function of the applied voltage. (I-V) curves are often represented as a semi-logarithmic plot, to account for the non-linear characteristics of a given device, e.g. in the presence of Schottky

junctions. Particular attention should be given to the measurement's integration time and its sweep speed, as they can have a significant influence on the charge carriers' capture and re-emission dynamics. Additionally, hysteresis curves have been performed to investigate the sensors' characteristics dependence between the forward and backward sweep.

Within the frame of this work, a DC bias voltage was supplied by an electrometer (6517B Electrometer/High Resistance Meter, Keithley Instruments) controlled by software (Labber, Lab Control Software Scandinavia AB) and connected to probe holders to obtain (I-V) curves. The interest in the use of an electrometer lies in the improved measurement's accuracy below the nanoAmpere range, due to the high resistivity of the sensors' electrical characteristics. The sensors were contacted with tungsten probes, while the probe holders were controlled via a probe station (PM8, Cascade Microtech). (I-V) curves were performed to specifically address accurate current measurements of the electrical properties of the thin film material. The resistance was evaluated by contacting ZnO thin films deposited on 1x1 cm² pieces of glass substrates with tungsten probes via a probe station (PM8, Cascade Microtech), while maintaining a constant lateral spacing of 1 mm between the probes, resulting in ohmic W/ZnO/W junctions. A DC bias voltage was supplied by an electrometer (6517B Electrometer/High Resistance Meter, Keithley Instruments) controlled by software (Labber, Lab Control Software Scandinavia AB) and connected to the probe holders to obtain I(V) curves. The bias voltage was thus swept over a defined tension range and the resulting current was measured by the electrometer.

2.3.9. Capacitance/conductance-voltage (C-V/G-V) and capacitance/conductance-frequency (C-f/G-f) measurements

Similar to (I-V) measurements, the sensors' capacitance-voltage (C-V) characteristics have been investigated and fitted by physical models for the determination of intrinsic material parameters. These measurements were performed with an impedance analyser (E4990A Impedance Analyzer, Keysight), where the voltage was swept linearly using defined frequencies for each measurement. A constant AC modulation with an amplitude of 500 mV was superimposed onto a DC bias voltage swept over

the defined tension range. The AC modulation is used for lock-in detection of the signal response of the device under test. Additionally, capacitance-frequency (C-f) have been performed, by varying the bias frequency f with a logarithmic sweep using defined bias voltage values for each measurement. The devices were contacted with tungsten probes via a probe station (PM8, Cascade Microtech) either completely in the dark, or under a microscope light (EasyLED Ringlights, SCHOTT) incident to the measured devices. The open and short calibration of the impedance analyser is a crucial step, realized prior to the measurements to remove the contribution of the cables and connections related to the device. The method described hereby can be further extended for the measurement of conductance-voltage (G-V) and conductance-frequency (G-f) measurements, by replacing the measured capacitance by the conductance of the device.

2.3.10. Electromechanical transduction

The electromechanical transducing characteristics of the developed piezotronic strain microsensors were investigated by integrating the sensors into the nose of an AFM (Nanonics MultiView 4000, Nanonics Imaging, Israel). Upon downward displacement of the head, the polymeric sensors' cantilevers were bent upwards, leading to the generation of a compressive strain in the clamped area of the sensors, where the platinum metal electrodes and the ZnO thin films are located. That mechanical strain triggers the piezotronic effect, inducing the creation of piezoelectric polarization charges at the Pt-ZnO interfaces, subsequently modulating the sensors' electrical characteristics. Our devices showed electromechanical transducing with the current response being modulated by different controlled compressive strains under a defined AC bias voltage. The specific electromechanical bench developed for the integration and testing of the piezotronic sensors, as well the corresponding transducing results are reported and detailed in Chapter 4 and 5.

2.3.11. Noise analysis

Noise is commonly described as an unwanted disturbance in an electrical signal. Several different sources of noise are prone to appear in electronic devices and are

associated with different physical processes. Three main sources of noise are typically identified within a diode junction, defined as the Johnson-Nyquist noise, the shot noise and the Flicker noise [26,27]:

- The Johnson-Nyquist noise, or thermal noise, depends on the temperature T , on the Boltzmann constant k_B and on the series resistance R_S of the semiconductor as:

$$S_{\text{Johnson-Nyquist}} = \frac{4k_B T}{R_S} \quad (2.5)$$

It is an unavoidable source of noise in most electronic devices, associated with random thermal motions of electrons flowing through the series resistance of a semiconductor. The Johnson-Nyquist noise is thus not frequency nor bias dependant for majority carriers' devices and results in a constant background noise in the whole frequency domain.

- The shot noise depends on the electron charge q , the diode current I_{diode} and the saturation current I_S , as:

$$S_{\text{Shot}} = 2q(I_{\text{diode}} + 2I_S) \quad (2.6)$$

The shot noise is defined as a randomly fluctuating noise current related to the movement of charge carriers in semiconductors [28]. It is particularly marked in devices presenting potential barriers (i.e. p-n or Schottky junctions) as the charge carriers must accumulate energy to overcome these barriers. As the shot noise is directly proportional to the DC current flowing through the diode, it will thus increase with a corresponding increase of the applied bias voltage.

- The Flicker noise, or $1/f$ noise, depends on the current I , the frequency f , and on other parameters being device-dependent constants (A , β , γ) [29], as:

$$S_{\text{Flicker}} = \frac{AI^\beta}{f^\gamma} \quad (2.7)$$

The exact origin and rational of the Flicker noise is still not precisely understood. It is generally related to low frequency movements of charges at the diode's junction interface states. As the electrons can randomly be trapped or released from the interface trap states, a fluctuation of the surface potential is observed in diode junctions which then leads to a variation in the charge carrier mobility [27]. The Flicker noise is proportional to the current and inversely proportional to the frequency, i.e. is it prominent for low applied frequencies and increases as the applied bias voltage is increased.

Noise measurements were performed using the Fast Fourier Transform (FFT) of the oscilloscope (WaveSurfer 3024, Teledyne LeCroy). A small Faraday cage was designed and mounted on the AFM nose to shield the sensors against the surrounding electromagnetic noises. Reference metal film resistors of known values (100 k Ω , 1 M Ω and 10 M Ω) were used to ensure that the experimental values of the noise spectral density background measured without any bias voltage corresponded to the expected theoretical value of the Johnson-Nyquist white noise density [30]. The corresponding noise analysis applied to the piezotronic strain sensors is described in Chapter 4, while further details concerning the experimental protocol for the extraction of the noise spectral density values are available in the Appendix C.

References - Chapter 2

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3. ZnO thin films elaboration by thermal atomic layer deposition

This chapter is focused on the deposition and on the control of ZnO thin films structural, chemical and electrical properties by thermal atomic layer deposition (ALD). The first section of this chapter aims at reporting and discussing relevant ZnO material properties used within the frame of this study, with a particular emphasis on the structural and piezoelectric properties of this material. The ALD deposition parameters leading to the obtention and optimization of the semiconducting thin film for a Schottky junction are thus detailed, followed by the characterization of the obtained ZnO thin films. The last section of this chapter is dedicated to the introduction of molecular oxygen pulsing within the ALD cycle performed, whose impact in terms of structural and electrical properties will be detailed.

3.1. ZnO general properties

ZnO is a II-VI compound semiconductor whose thermodynamically stable phase at ambient conditions is the hexagonal wurtzite symmetry. A typical hexagonal wurtzite ZnO crystal structure is represented in Fig. 3.1(a). This structure is characterized by three lattice parameters a , b , c , as well as three angular parameters α , β , γ (where $a = b$, $\alpha = \beta = 90^\circ$ and $\gamma = 120^\circ$). The lattice parameter a is defined as the edge length of the basal plane hexagon, while the lattice parameter c corresponds to the unit cell height perpendicular to this plane. Their values are typically ranging from 3.24 Å to 3.25 Å for the lattice parameter a , while the lattice parameter c is ranging from 5.20 Å

to 5.21 Å [1]. It should be noted that these values can be increased or decreased by the impact of stress, temperature, as well as by the variation of the charge carrier density in the semiconductor. The crystal structure is composed of two interpenetrating hexagonal close-packed sublattices, separated by a defined distance along the c-axis which depends on the ratio between the lattice parameters c and a [2]. A sublattice is constituted by four atoms per unit cell, where each group II atom (i.e. Zn) is tetrahedrally bonded to four group VI atoms (i.e. O), and vice-versa.

The Zn-O bond exhibits a substantial degree of polarity, due to the strong electronegativity of oxygen. The equivalent ionic crystal structure is thus composed of Zn^{2+} cations and O^{2-} anions. The appearance of the piezoelectric effect is linked with the non-centrosymmetric nature of the ZnO wurtzite crystal structure, leading to the generation of electric dipole moments, as illustrated in Fig. 3.1(b). By convention, the c-axis direction is fixed assuming that the positive direction goes from the cations to the anions. In a steady-state configuration (i.e. no strain applied to the crystal structure), the center between the positive cations and negative anions coincide with each other, resulting in a cancellation of the dipole moments on a macroscopic scale for symmetric crystal structures. However, due to intrinsic asymmetry of the bonding in the equilibrium ZnO wurtzite crystal structure, a net dipole moment is generated along the c-axis, inducing a spontaneous polarization. This spontaneous polarization P_{SP} has to be differentiated from the piezoelectric polarization P_{PE} induced by a mechanical strain. As shown in Fig. 3.1(b), the application of either a tensile or compressive strain along the c-axis of the ZnO is leading to a deformation of the wurtzite crystal structure, thus modifying the distance between the center of the cations and anions. Consequently, a dipole moment is generated along the c-axis, corresponding to the piezoelectric polarization. The spontaneous and piezoelectric polarization are parallel when a tensile strain is applied (i.e. both negative along the c-axis) and antiparallel when a compressive strain is applied (i.e. positive for the piezoelectric polarization and negative for the spontaneous polarization along the c-axis). Nonetheless, the magnitude of the piezoelectric polarization is larger than the spontaneous polarization in wurtzite crystal structures [3]. In the configuration described by Fig. 3.1(b), both the strain and the piezoelectric polarization are respectively applied and induced along the c-axis, which corresponds to a contribution

of the piezoelectric coefficient e_{33} . Nonetheless, the strain can also be applied on the plane of the wurtzite structure, this configuration being described by Fig. 3.1(c). If a material is stretched (compressed) in its planar direction, it will consequently be subject to a compressive (tensile) strain along the c -axis direction, which corresponds to a contribution of the piezoelectric coefficient e_{31} . This leads to an inversion of the sign of the piezoelectric polarization, which is well described by the opposite signs between e_{31} and e_{33} .

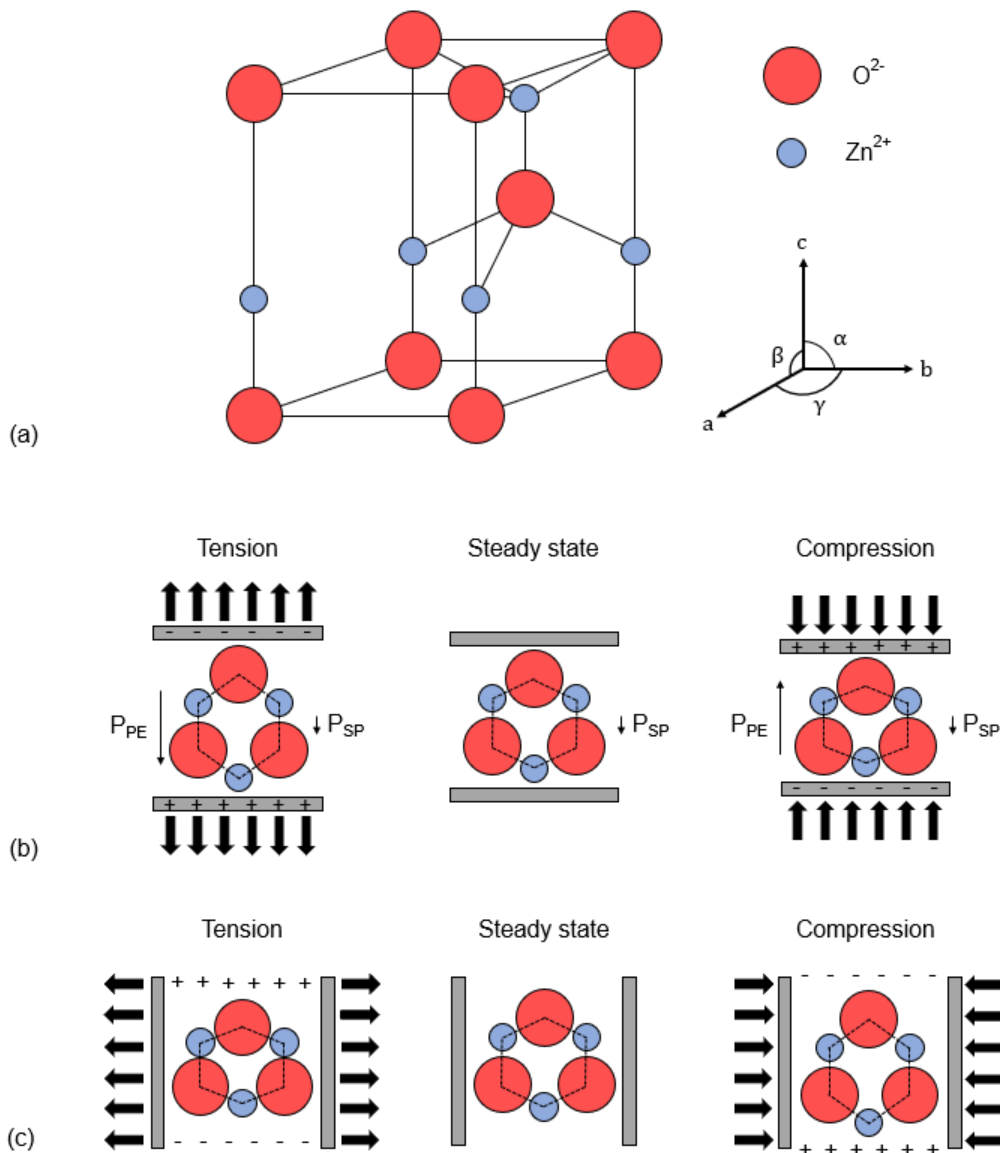


Figure 3.1. (a) Atomic representation of the hexagonal wurtzite ZnO crystal structure. (b) Schematic representation of the impact of the application of a compressive or tensile strain exerted along the c -axis on the ZnO crystal structure. (c) Schematic representation of the impact of the application of a compressive or tensile strain exerted along the basal plane on the ZnO crystal structure. Adapted from [4].

Reportedly, the piezoelectric strain coefficient values for ZnO wurtzite crystal structures are typically in the range of -0.33 to -0.66 $\text{C}\cdot\text{m}^{-2}$ for e_{31} , 0.92 to 1.56 $\text{C}\cdot\text{m}^{-2}$ for e_{33} and -0.35 to -0.59 $\text{C}\cdot\text{m}^{-2}$ for e_{15} [2,5], while the spontaneous polarization for such structures is given as -0.057 $\text{C}\cdot\text{m}^{-2}$ [3,6]. The corresponding ZnO piezoelectric stress coefficient values are reported as -5×10^{-12} $\text{C}\cdot\text{N}^{-1}$ for d_{31} , 12×10^{-12} $\text{C}\cdot\text{N}^{-1}$ for d_{33} , and -10×10^{-12} $\text{C}\cdot\text{N}^{-1}$ for d_{15} [5], respectively. These values are among the highest reported for piezoelectric constants when compared to other tetrahedrally bonded wurtzite semiconductors such as InN and GaN, with the notable exception of AlN matching and sometimes presenting higher e_{33} values [3,7] with an insulating behaviour for a large bandgap of 6.2 eV. These properties lead to a large electromechanical coupling, which is especially suitable for sensing applications in MEMS.

Furthermore, ZnO is a direct wide band gap semiconductor ($E_g \sim 3.3$ eV [8] at 300 K) with large exciton binding energy (~ 60 meV) exhibiting transparency in the visible wavelength range, thus making it a great prospect for optoelectronics applications. The attractiveness of ZnO over other wurtzite semiconductors is further reinforced by its abundance compared with the limited availability of Ga and In [9], its amenability to wet chemical etching [10] as well as its biocompatibility and biosafety [11]. All these reasons motivated our choice for using ZnO as the semiconducting material within the frame of this work.

3.2. Optimization of Schottky behaviour by ALD

ZnO can be readily deposited in thin film form by a wide range of deposition techniques, the most common ones including magnetron sputtering, pulsed laser deposition (PLD), metal-organic chemical vapour deposition (MOCVD) and molecular beam epitaxy (MBE) [1,12]. As the need for ZnO thin films of high crystalline quality grown at low temperatures is increasingly important for their integration on organic substrates for flexible electronics, the range of available techniques is considerably restricted. Within this scope, atomic layer deposition (ALD) appears as an ideal technique to match these criteria. It is well known that the ALD processing is the only one to deposit highly

conformal and uniform thin layers (from the atomic scale to hundreds of nanometers thick) of inorganic materials on large scale (until 10 inches wafer) even at low temperature growth (from room temperature to 300 °C) compatible with the coating of fragile flexible polymeric substrates.

The ALD growth of ZnO was first demonstrated in 1985 by Tammenmaa et al. via the use of zinc acetate and water as precursors [13], where a high temperature above 280 °C was needed for the reaction to occur. Throughout the years, more reactive precursors have been developed, diethylzinc (DEZ) and water (H₂O) being by far the most commonly used precursors in the recent years. The exothermic nature of the reaction between DEZ and water allows the deposition of ZnO thin films even at very low temperatures (from room temperature up to 600 °C [14]). Additionally, the doping of ZnO thin films by ALD with various elements has been developed [15], where the layer-by-layer method of deposition allows for a fine tuning of the doping composition. The conventional ALD process involving the sequential pulsing of precursors, where the surface chemistry is driven by thermal energy is referred as thermal ALD. Another approach consists in using plasma-activated reactant species, referred as plasma-enhanced ALD (PEALD) [16]. Oxygen or water are used in plasma form, leading to a higher stoichiometry linked with the higher reactivity of the plasma source [14].

Nonetheless, only a few works relate about the use of ALD to deposit ZnO in order to obtain Schottky junctions [17–22], **but none of them detailed a post-processing to obtain a strain sensor as we propose for the first time in this thesis work**. The critical control of the ZnO privileged crystalline orientation for such polycrystalline layer to maintain high piezoelectric properties, as well as the control of the resistivity, the carrier concentration and mobility to get a Schottky diode junction are highly challenging. The previously reported works have a common feature [17–22], as low deposition temperatures appear as a viable way to obtain a Schottky junction with a high work function metal. Most notably, E. Guziewicz et al. [17] showed the formation of a Schottky junction between Ag metal electrodes and ZnO thin film deposited by ALD at 100 °C, while reporting a value of 10^{17} cm^{-3} for the electron concentration and $17 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ for the electron mobility. In the same report, they stated that the electron concentration and the electron mobility dedicated to Schottky junctions should be

inferior to the values of $2 \times 10^{17} \text{ cm}^{-3}$ and $10 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$, respectively [17,23], thus providing useful guidelines for subsequent material processing.

From the semiconductor side, the electron concentration is the key parameter to control in order to obtain a Schottky behaviour. If the electron concentration value is too high, the size of the depletion region is reduced, and electrons are able to tunnel through the barrier via field emission, resulting in an Ohmic behaviour of the M-S (Metal-Semiconductor) junction. The electron mobility in semiconductors is particularly important as it influences the frequency bandwidth or time response of a given device. As reported by D. K. Schroder [24], the carrier velocity is proportional to the mobility for low applied electric fields. Thus, a material presenting a high carrier mobility will have a high frequency response. Additionally, semiconductors with higher mobilities have higher currents values and charge capacitances more rapidly, which results as well in a higher frequency response [24]. The electron mobility is thus a key parameter for applicative areas, as high electron mobilities allow devices' operation at higher frequencies.

The control of the deposition temperature to values below $100 \text{ }^\circ\text{C}$ is the principal way for affecting the electron concentration, which ensures optimal conditions for the apparition of a favoured Schottky behaviour. More details concerning the origin of the variation of this parameter against the temperature together with the variation of the electron mobility and the resistivity of the ZnO thin films are given in the following section. Within this scope, the deposition of ZnO by ALD in this work has been realized at low temperatures (from $60 \text{ }^\circ\text{C}$ to $100 \text{ }^\circ\text{C}$) to ensure the formation of a Schottky junction at the interface with high work function platinum metal electrodes. The low temperature deposition of this thin film is also mandatory to make feasible the processing of the Schottky junction on organic substrates for plastic MEMS devices as we will describe in chapters 4 and 5.

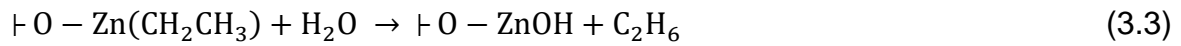
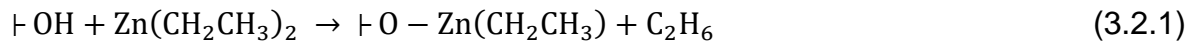
3.3. Characterization of ZnO thin films grown by thermal ALD at low temperatures

3.3.1. ZnO deposition by ALD

As previously mentioned, the most common ALD cycle used for the deposition of ZnO thin films involves the sequential pulsing of diethylzinc (DEZ) and deionized water. A schematic representation of the performed ALD cycle using these precursors is provided in Fig. 3.2. They follow the net reaction:



The assumed half-reactions occurring during the growth mechanism are the following [25]:



Where “┆” is representing the substrate’s surface. It is worth mentioning that the ZnO growth by ALD involves the presence of hydroxyl (┆OH) groups at the surface of the substrate to initiate the first reaction within the ALD cycle. The realization of a plasma treatment prior to the ALD deposition greatly contributes to increase the surface energy and wettability by the introduction of hydroxyl moieties at the substrate’s surface to facilitate the ALD nucleation [26]. The ALD window for such a process is typically located between 110 °C and 170 °C, with corresponding GPC (Growth Per Cycle) values between 1.8 Å/cycle and 2.0 Å/cycle [14].

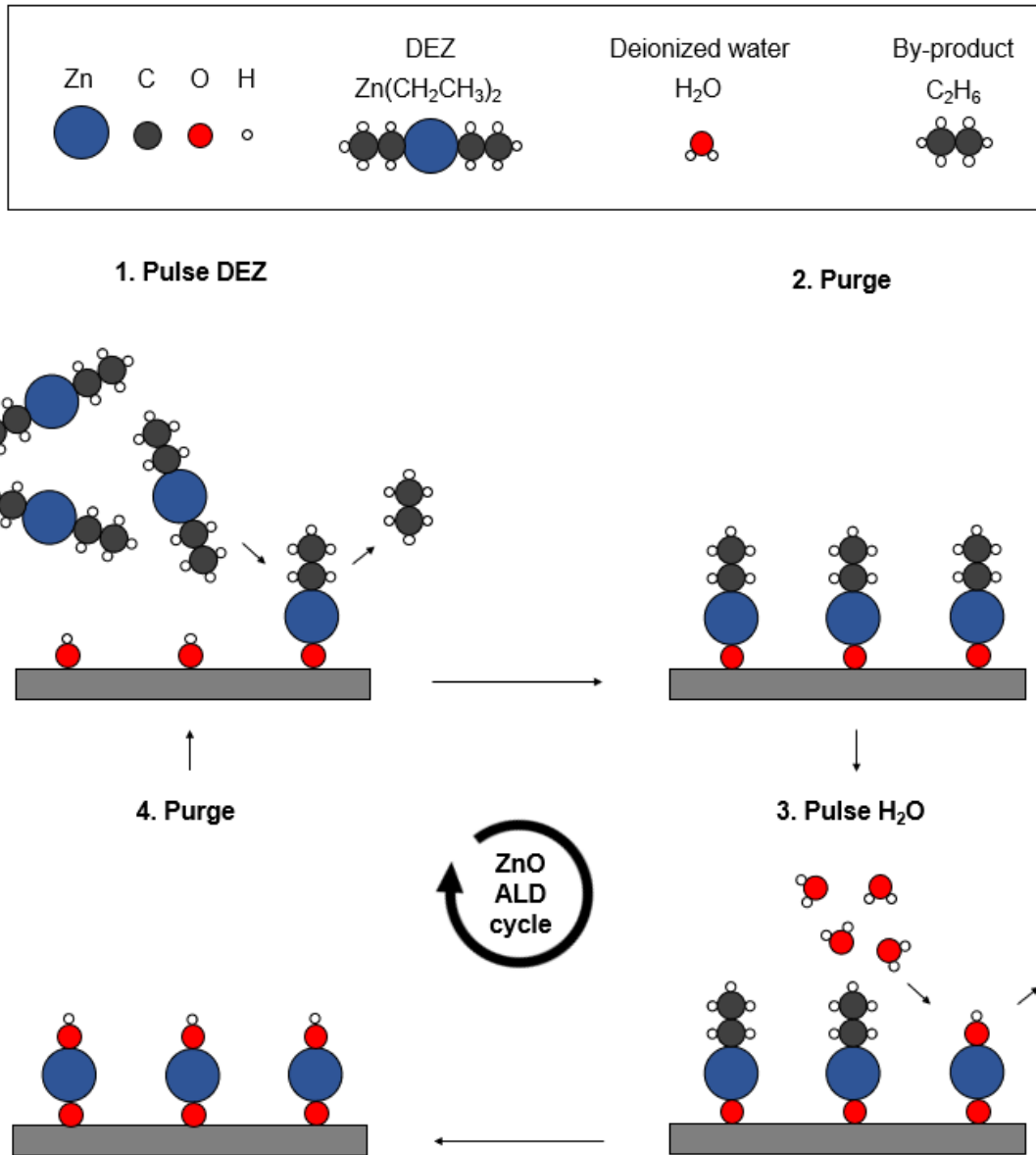


Figure 3.2. Schematic representation of the ALD cycle for ZnO thin films deposition using DEZ and deionized water as precursors.

3.3.2. Experimental part

The ZnO thin films were synthesized using precursors of diethylzinc [DEZ, $Zn(C_2H_5)_2$] (Strem Chemicals, Inc., France) and deionized (DI) MilliQ water (resistivity of 18.2 M Ω .cm at 25 °C), in a commercial ALD reactor (TFS-200, Beneq, Finland) with a thermal configuration. On the one hand, the supporting surfaces for the ZnO thin film deposition consisted of 1x1 cm² pieces of pristine single crystal Si(100) wafer (grade Monitor, Siebert GmbH, Germany), some of them coated with a 200 nm thick Platinum

(Pt) layer (deposited by Electron Beam Metal Evaporation) for comparative thicknesses and structural measurements with the polymeric substrates. On the other hand, 75 μm thick polyimide films (Kapton $\text{\textcircled{R}}$ HN, Dupont) were used for the subsequent processing of piezotronic strain microsensors. The substrates were cleaned in acetone, isopropanol and DI water, followed by dehydration for 30 min at 200 $^{\circ}\text{C}$ (ramp: 150 $^{\circ}\text{C}/\text{h}$) prior to the ALD growth of ZnO films. Before being introduced into the ALD reactor, an additional plasma cleaning (Plasma Therm 790 RIE, 50 W, 5 minutes, in Ar: O_2 gases environment at 60 mTorr) was performed on the substrates. Alphagaz 2 Argon gas was used for the purging steps during the ALD process, with a global purity $\geq 99.9999\%$ mol and less than 0.5 H_2O ppm.mol impurity. The ZnO thin films were elaborated at a substrate temperature varying between 60 $^{\circ}\text{C}$ and 100 $^{\circ}\text{C}$, based on the following sequence of four steps: DEZ pulse (0.1 s), Ar purge (6 s), DI water pulse (0.1 s), and Ar purge (6 s). Thermocouples located inside the ALD reaction chamber are controlling and monitoring the reactor and substrate temperatures to the desired value. The depositions were performed under a constant pressure of 2 mbar, controlled by pressure gauges. A number of loops between 1000 and 2000 was set based on the growth rate of the created ZnO thin films at the different temperatures, in order for the ZnO thin films to obtain a thickness ranging between 150 nm for the structural characterization and 300 nm for the piezotronic strain sensors. A higher thickness of the ZnO thin films contributes to an increased electrical stability response of the Schottky junctions by limiting the apparition of memristive phenomena [27].

3.3.3. Structural and electrical properties of deposited ZnO thin films

The growth rate obtained for temperatures ranging from 60 $^{\circ}\text{C}$ to 120 $^{\circ}\text{C}$, as well as the related cross-sectional micrographs depending on the growth temperature are illustrated on Fig. 3.3 and 3.4, respectively. The GPC values obtained increase as deposition temperatures increases, indicating that the growth of ZnO thin films is outside the ALD temperature window for temperatures below 100 $^{\circ}\text{C}$. This behaviour is typical of low reactivity reactions due to insufficient kinetic energy activation for the ligand exchange reactions, where low temperatures prevent complete reactions from

occurring [28]. However, as the temperature is increased above 100 °C, the GPC is reaching the reported values for the ALD temperature window [14].

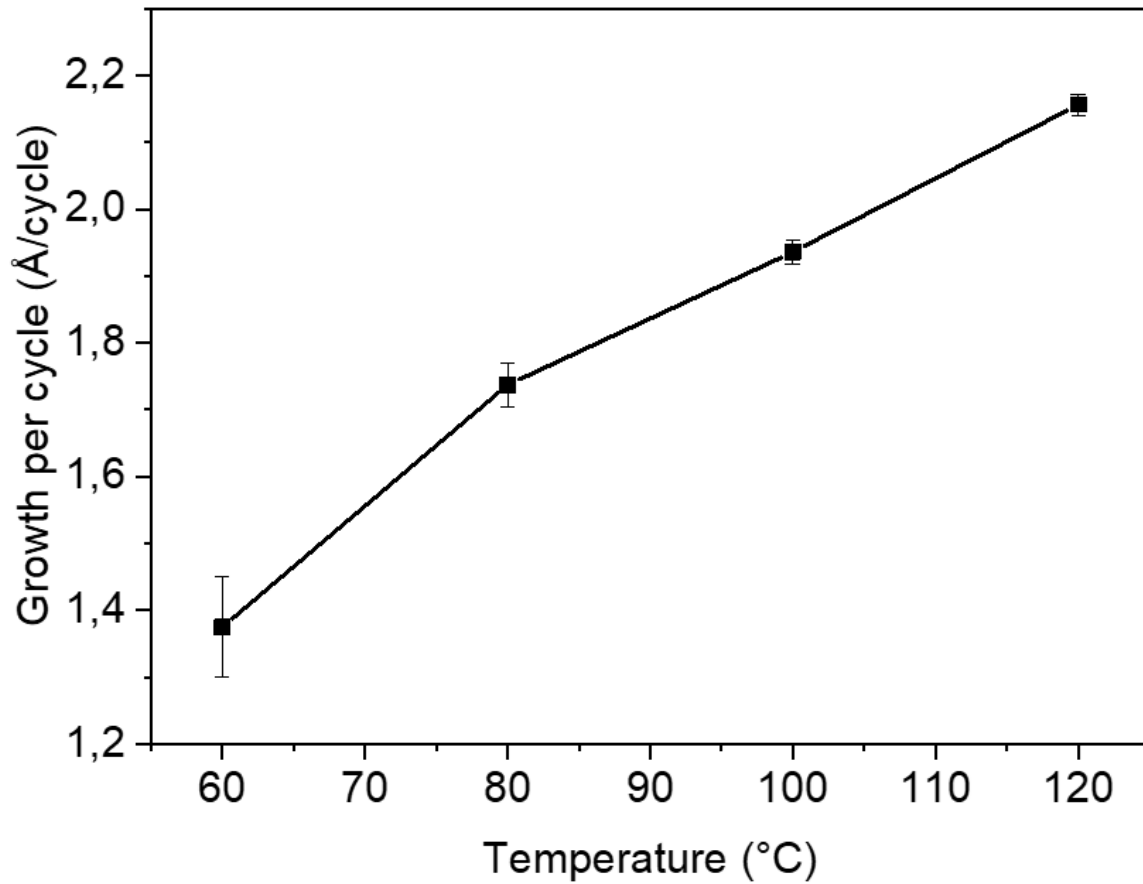


Figure 3.3. Growth rate per cycle ($\text{\AA}/\text{cycle}$) of ZnO thin films by ALD for different deposition temperatures.

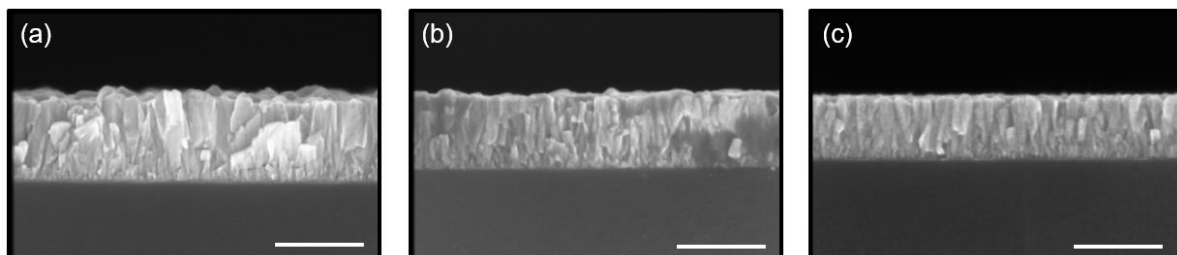


Figure 3.4. SEM cross-sectional images of ZnO thin films grown on Si substrates at (a) 100 °C, (b) 80 °C and (c) 60 °C. Each ZnO thin film was obtained with 1000 ALD loops. The scale bar corresponds to 200 nm.

The SEM top view images of ZnO thin films grown by ALD on reference Si substrates with the associated grazing incident x-ray diffraction (GI-XRD) at a deposition temperature of (a) 100 °C, (b) 80 °C and (c) 60 °C are presented on Fig. 3.5.

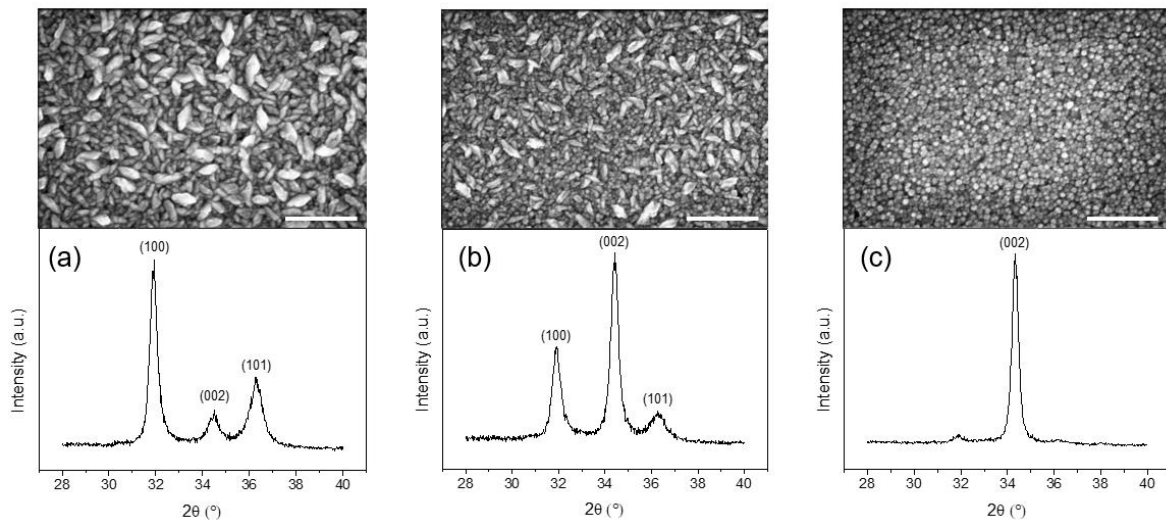


Figure 3.5. SEM top view images and associated GI-XRD diffraction patterns ($\omega=0.3^\circ$) of ZnO thin films grown on Si substrates at a deposition temperature of (a) 100 °C, (b) 80 °C and (c) 60 °C. The obtained ZnO thin films were deposited with the same number of ALD loops (1000). The scale bar corresponds to 300 nm.

The ZnO thin films deposited are polycrystalline. At a temperature of 100 °C, a different distribution of grain orientations can be observed, split between the (100), (002) and (101) crystalline orientations. This is further confirmed by SEM top view images showing a distribution of wedge-like shaped crystallites parallel to the substrate and of fine columnar crystallites perpendicular to the substrate at this temperature. However, in comparison to these results obtained at 100 °C, a transition occurs as the deposition temperature decreases, with a strong increase of the diffraction peak intensity corresponding to the (002) crystalline orientation at deposition temperatures of 80 °C and 60 °C. This is consistent with the appearance of fine columnar crystallites considerably increasing as deposition temperatures decrease. Obtaining a privileged (002) crystalline orientation perpendicular to the substrate, along the c-axis, is especially important for piezoelectric applications in order to maximize the collective piezoelectric participation of ZnO grains with similar piezoelectric strain coefficient value and orientation [29–31]. Nonetheless, additional XRD measurements in a θ - 2θ configuration shall be performed to assess the preferential crystalline orientation of the obtained ZnO thin films as a function of the deposition temperature.

Similar observations can be applied to the growth of ZnO thin films on the sensors' substrates, polyimide and platinum, as can be observed in Fig. 3.6 and 3.7, respectively.

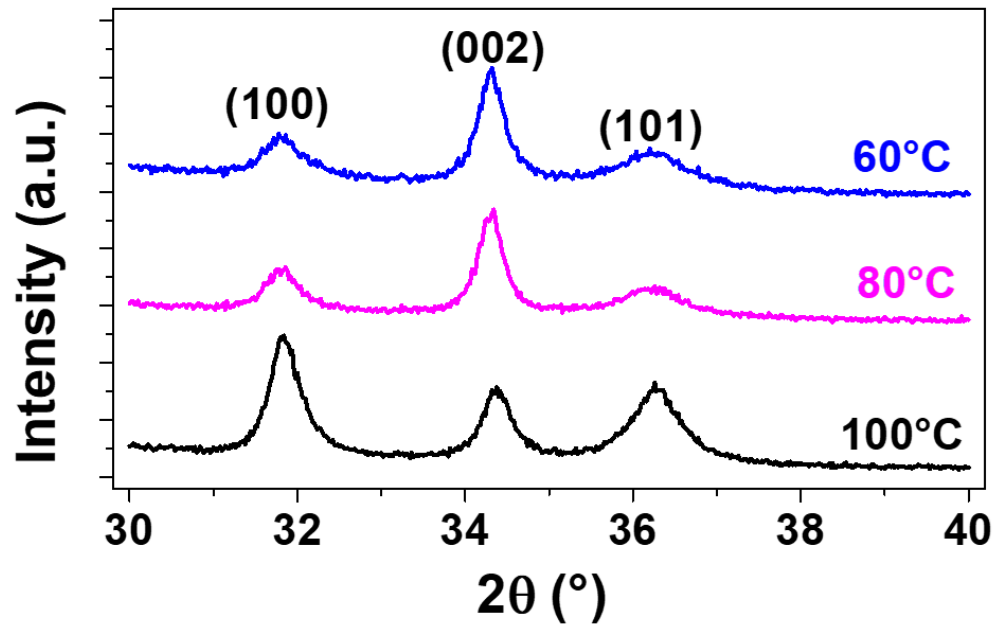


Figure 3.6. GI-XRD diffraction patterns ($\omega=0.3^\circ$) of ZnO thin films grown on top of 75 μm thick polyimide substrates at 100 $^\circ\text{C}$, 80 $^\circ\text{C}$ and 60 $^\circ\text{C}$.

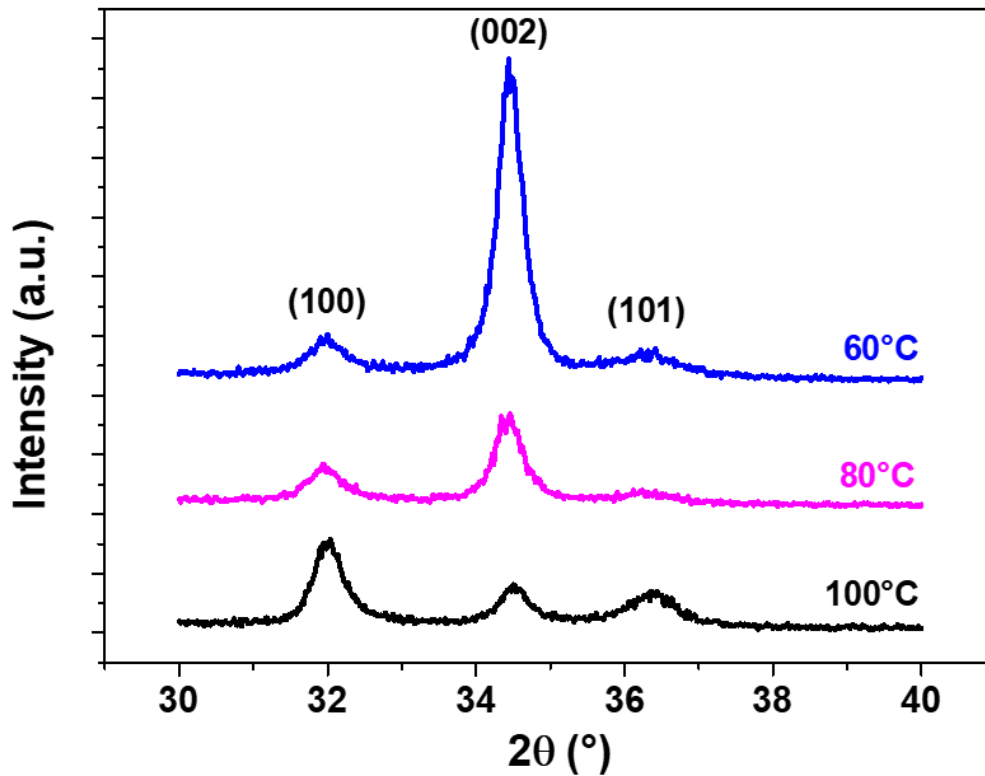


Figure 3.7. GI-XRD diffraction patterns ($\omega=0.3^\circ$) of ZnO thin films grown on Si substrates coated with a 200 nm thick Pt layer at 100 °C, 80 °C and 60 °C.

Furthermore, the conformality of the ALD technique is demonstrated in Fig. 3.8, where a ZnO layer is deposited on a polyimide substrate as well as on the top of Pt electrodes. An encapsulation layer of SU8 resist is deposited on top to protect the ZnO/Pt junction against the environmental conditions and to maintain the electrical performance.

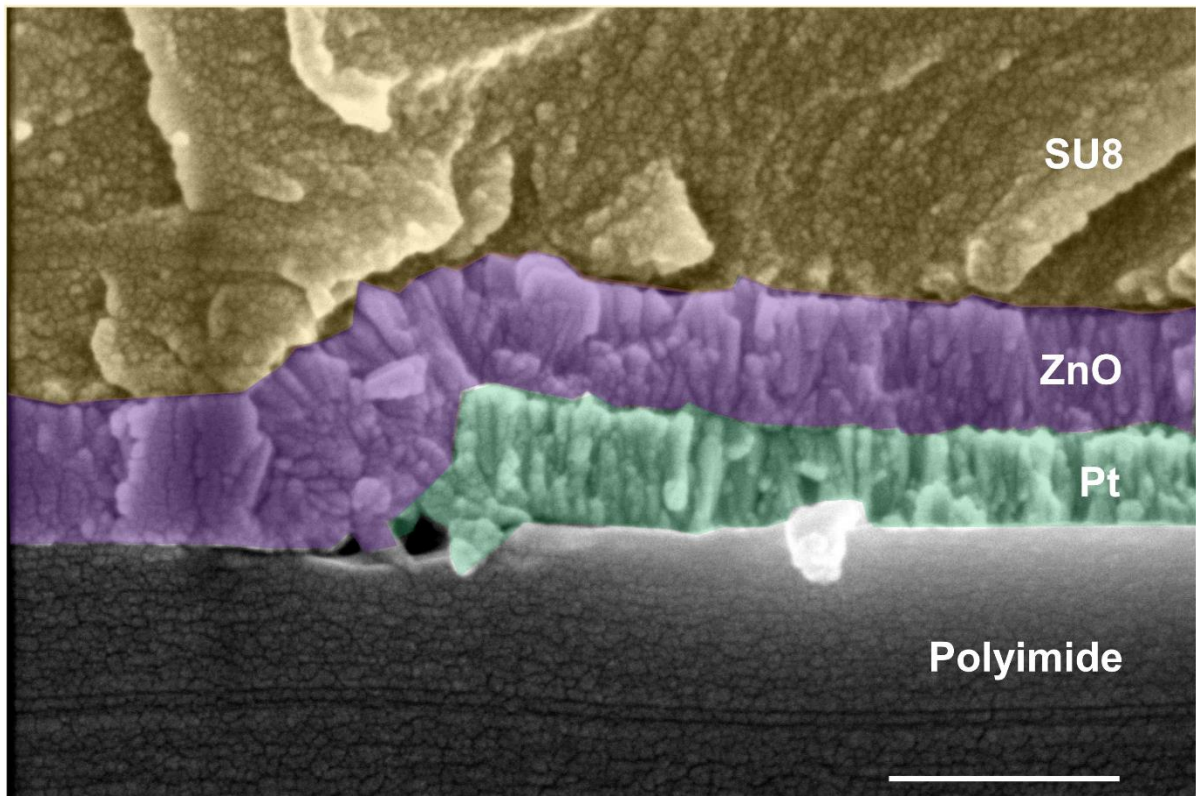


Figure 3.8. Cross-section showing the conformality of the ZnO thin film deposited by ALD on the polyimide substrate and the platinum metal electrodes. A SU8 resist top layer is deposited to protect the ZnO/Pt junction. The scale bar represents 500 nm.

The apparition of the (002) crystalline orientation below 100 °C shows the strong dependence between the crystallinity and the deposition temperature while using ALD as a deposition technique. Similar results were reported in the literature [28,32,33] for low deposition temperatures with a thermal ALD configuration. A. Di Mauro et al. [33] showed a strong increase of the diffraction peak intensity corresponding to the (002) orientation for increasing thicknesses between 9 nm and 42 nm, for ZnO thin films deposited at 80 °C. These results thus suggest that ZnO crystallites with random orientations are grown within a defined thickness range (~ 20 nm) during the nucleation. Within this scope, transmission electron microscopy (TEM) investigations were performed to further assess the respective impact of the nucleation and the subsequent growth on the crystallinity of the ZnO thin films deposited by ALD at low temperatures. The samples in study consisted of ~ 300 nm thick polycrystalline ZnO thin films deposited by ALD at 80 °C on ~ 200 nm thick Pt substrates. The obtained

cross-sectional micrographs at different areas and magnifications of the ZnO/Pt interface are shown in Fig. 3.9, 3.10 and 3.11.

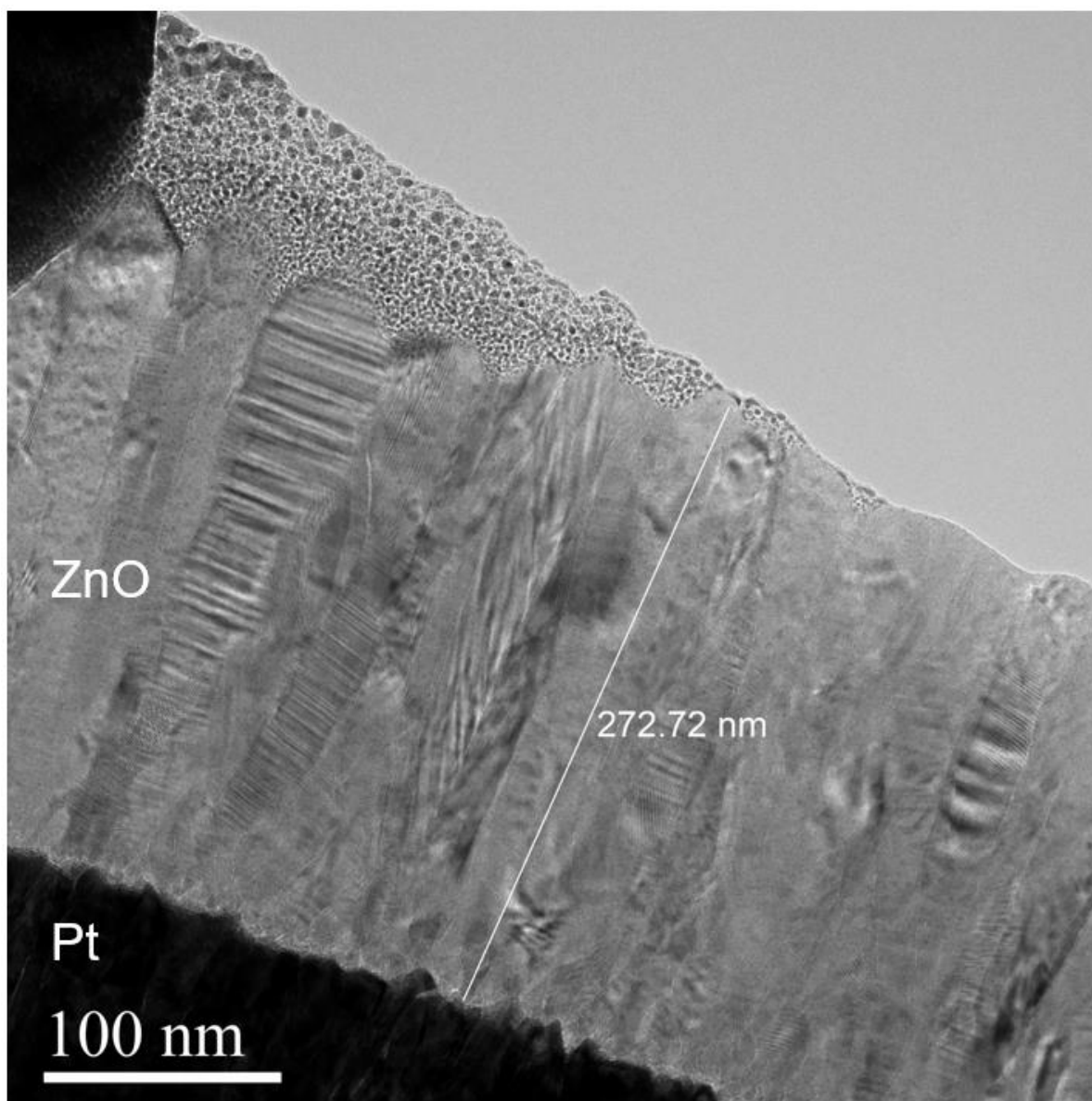


Figure 3.9. TEM Bright Field (BF) micrograph of the ALD-grown ZnO thin film at 80 °C.

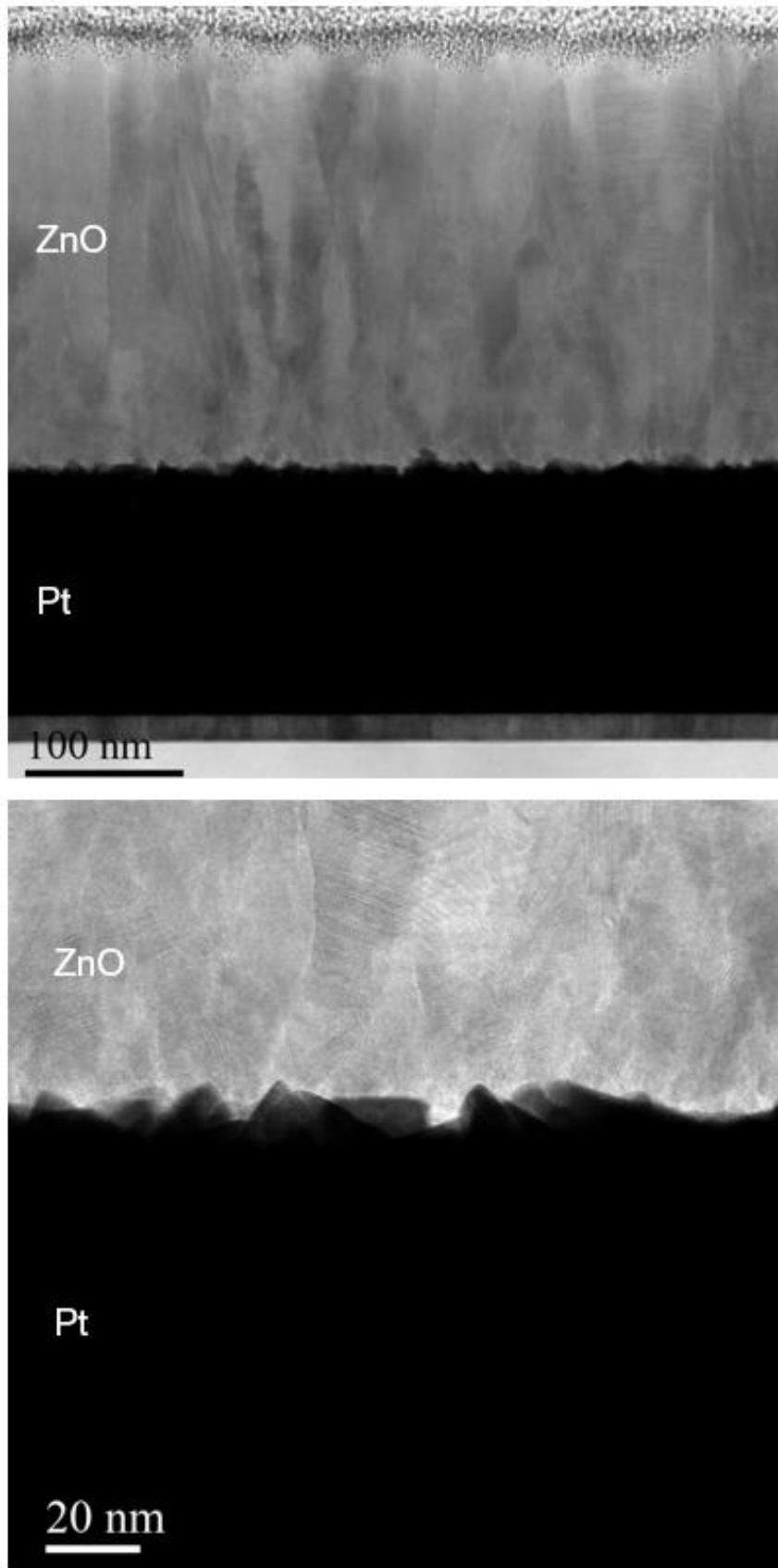


Figure 3.10. Scanning transmission electron microscopy (STEM) BF micrographs of the ZnO/Pt interface.

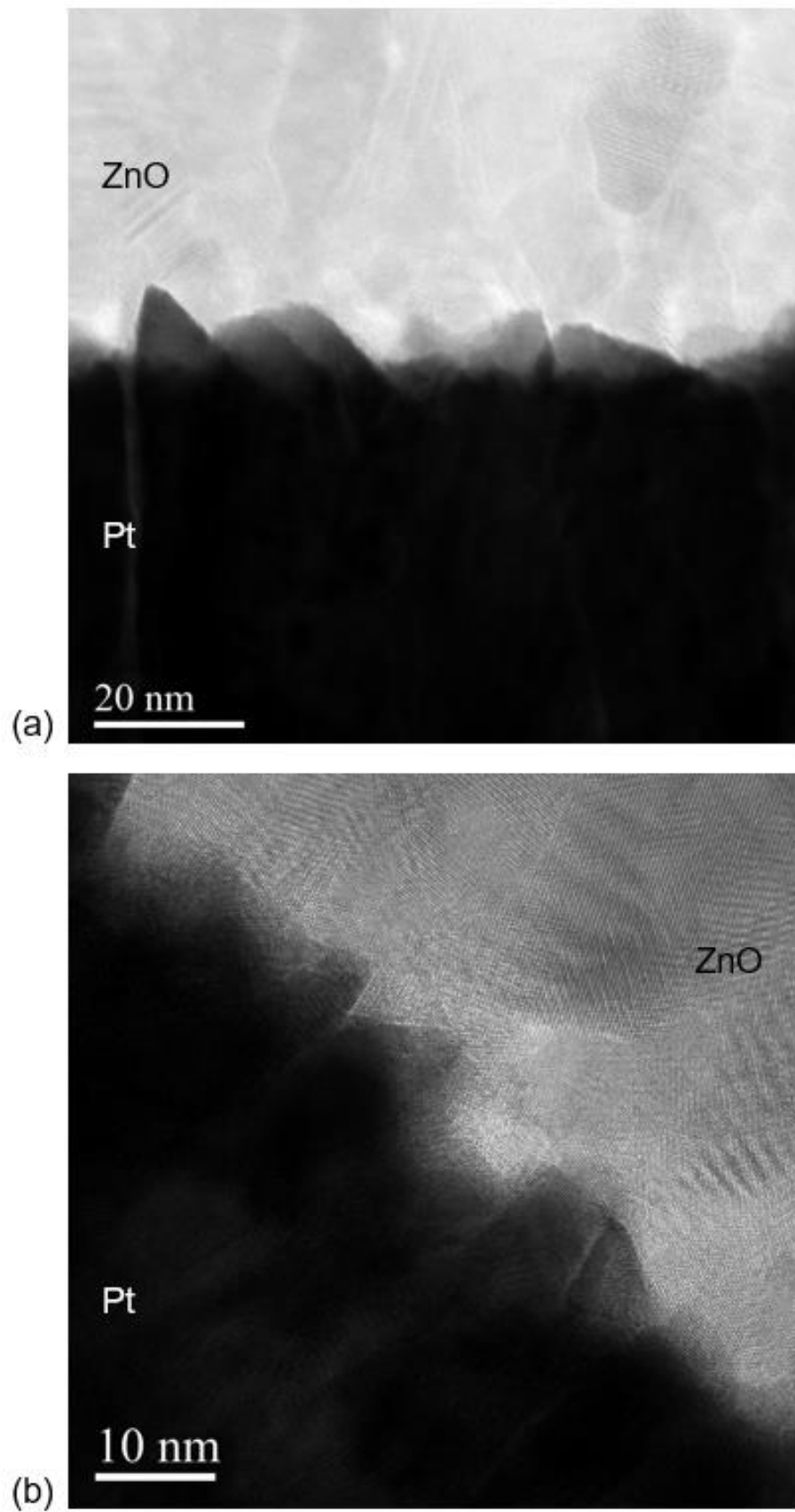
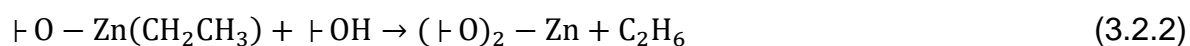


Figure 3.11. (a) STEM BF micrograph and (b) High-resolution TEM (HRTEM) micrograph of the ZnO/Pt interface.

As expected from Fig. 3.9, the columnar growth of the ZnO thin film with the (002) crystalline orientation perpendicular to the Pt substrate can be observed. Nonetheless, as the magnification is increased towards the ZnO/Pt interface in Fig. 3.10 and 3.11, a substantial reduction in the ZnO crystallite size can be seen within the first 10 nm to 20 nm close to the Pt substrate. The micrographs in Fig. 3.11 clearly show that several ZnO crystallites with random crystalline orientations are grown during the first stages of nucleation by ALD, which further confirms the above-mentioned statement.

Furthermore, the use of plasma-enhanced ALD (PEALD) using DEZ and oxygen plasma as precursors seems to suppress the dominance of the (002) orientation for temperatures below 100 °C [34,35]. Nonetheless, to the best of our knowledge, the mechanism concerning the (002) plane growth at low temperatures by thermal ALD has not yet been well understood.

A more detailed explanation can be provided by considering a departure from the ideal half-reactions presented in the section 3.3.1. Following the initial DEZ pulse, the monoethyl zinc (MEZ) containing an ethyl ligand may further react with the hydroxyl groups on the surface [36–38], as:



This additional reaction leads to the formation of a bare zinc on the substrate's surface, linked with two oxygen originating from hydroxyl sites. Concomitantly, MEZ originating from the initial reaction (3.2.1) remains as well on the surface. Weckman et al. [36,37] stated that the bare zinc atoms are able to subsequently adsorb water while a fraction of the ethyl ligands persists on the surface after the water pulse has ended. They suggested that the incomplete elimination of the ethyl ligands is linked with the presence of a kinetic barrier which depends on the temperature. Consequently, the fraction of persisting ethyl ligands would be decreased with an increase in the deposition temperature. This would result in an increase of the number of reactive surface sites for both polar and nonpolar orientation surfaces of the ZnO, leading to the increase of the growth rate in the (001), (101) and the (002) orientations with increasing temperatures. In a similar study, Cai et al. [28] reported that each DEZ

molecule reacted with nearly 1.5 H-OH surface sites for every growth temperature in study (i.e. 80 °C, 100 °C, 120 °C, 150 °C, 200 °C and 250 °C), except for the temperature of 30 °C where 2 H-OH sites were available per Zn site. These results suggest that the occurrence of the reactions (3.2.1) and (3.2.2) are equally shared for these temperatures, except at 30 °C where the growth is predominantly originating from the formation of bare zinc, and where most of the ethyl ligands would not react with the water pulse. Additionally, Malm et al. [32] reported in ZnO thin films grown in similar conditions an increasing hydrogen content from 2.0 at.% at a growth temperature of 120 °C to 4.5 at.% at 70 °C, with a sharp increase to 11 at.% at 40 °C. They observed a similar behaviour for the carbon content which increased from 0.25 at. % at 70 °C to 1.1 at. % at 40 °C. These increases in both the hydrogen and carbon content could thus be linked with the increase in the persisting ethyl ligands at lower temperatures. Moreover, based on the calculations of Fujimura et al. [39], the (002) crystalline orientation appears as the growth direction possessing the lowest surface free energy, it is thus more thermodynamically favourable at lower temperatures. As the energy activation is limited for low temperatures, this may explain the dominance of the (002) plane for deposition temperatures below 100 °C, as the fastest-growing direction would determine the preferred crystallographic orientation of the ZnO thin films.

Additionally, the internal strains of the ZnO thin film induced during the ALD growth process are correlated to crystallinity changes and shifting of the lattice parameters. As introduced in the introduction paragraph “ZnO general properties”, the piezoelectric properties are linked with the non-centrosymmetric nature of the ZnO wurtzite crystal structure, leading to the generation of electric dipole moments. The lattice parameters a and c , characteristics of the hexagonal wurtzite structure of the polycrystalline ZnO thin films, were calculated using Bragg’s law:

$$\lambda = 2 \cdot d_{hkl} \cdot \sin\theta \quad (3.4)$$

With λ the X-ray wavelength (1.5406 Å for Cu $K\alpha$ radiation), d_{hkl} the distance between planes using Miller indices h , k and l and θ the glancing angle.

When applied to a hexagonal structure, the plane spacing equation combined with Bragg's law yields:

$$\frac{1}{d_{hkl}^2} = \frac{4}{3} \cdot \left(\frac{h^2 + h \cdot k + k^2}{a^2} \right) + \frac{l^2}{c^2} = \frac{4 \cdot \sin^2 \theta}{\lambda^2} \quad (3.5)$$

The lattice constants a and c can thus be calculated by equations (3.6) and (3.7), according respectively to the (100) and (002) diffraction planes:

$$a = \frac{\lambda}{\sqrt{3} \cdot \sin \theta} \quad (3.6)$$

$$c = \frac{\lambda}{\sin \theta} \quad (3.7)$$

The internal strain ε_i along the c -axis was then determined by:

$$\varepsilon_i = \frac{c - c_0}{c_0} \quad (3.8)$$

The ZnO reference (JCPDS-36-1451) has been used for the lattice parameter c_0 value of 5.211 Å.

The measurements were carried out for ZnO deposition temperatures of 100 °C, 80 °C and 60 °C, on Si samples coated with a 100 nm layer of Pt. The platinum (111) peak, located at constant value of $2\theta = 40,2^\circ$, was used as a reference to track the shift of the ZnO (002) peak. The corresponding diffraction patterns are presented in Fig. 3.12.

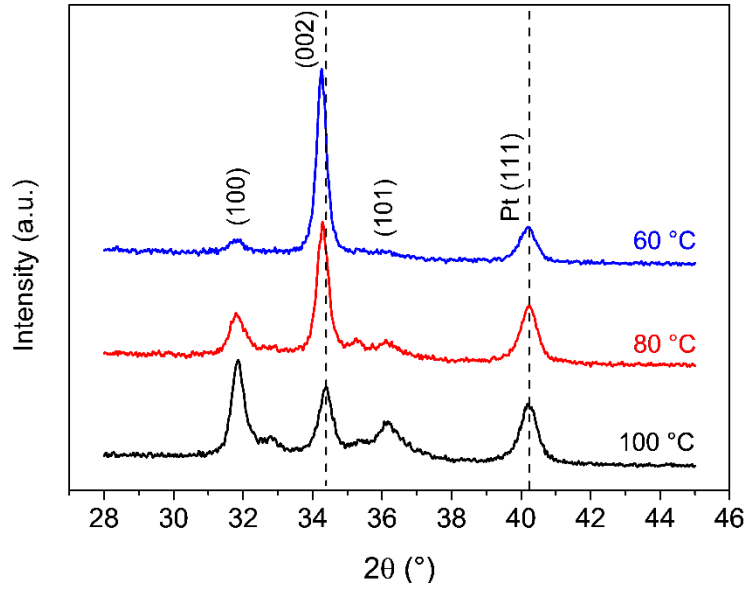


Figure 3.12. GI-XRD diffraction pattern ($\omega = 0.6^\circ$) of ZnO thin films with different growing temperatures, deposited on Si samples coated with a 100 nm layer of Pt. The black dashed vertical line highlights the shift of the (002) peak.

The calculated values of the lattice parameters and the internal strain for different deposition temperatures are summarized in Table 3.1 below:

Deposition temperature (°C)	Thickness (nm)	2θ (100) (°)	2θ (002) (°)	a (Å)	c (Å)	ϵ_i (%)
100	115.2	31.86	34.38	3.241	5.213	0.035
80	99.8	31.85	34.29	3.242	5.226	0.289
60	105.6	31.84	34.26	3.243	5.231	0.375

Table 3.1. Lattice parameters and internal strain calculations for different deposition temperatures.

Interestingly, the (002) peak values of ZnO are significantly shifting to higher 2θ values as the deposition temperature is increasing. This leads to an increase of the lattice parameter c of the hexagonal structure for decreasing deposition temperatures when compared to steady state reference values, which suggests that the ZnO thin films are subject to an increasing tensile strain state along the c-axis as the temperature is decreasing. These results are consistent with the ones reported by T. Nguyen et al. [8], where ZnO thin films deposited in similar conditions are experiencing an increasing compressive strain state along the c-axis for increasing deposition temperatures

between 100 °C and 200 °C. The presence of internal strain along the c-axis induces the generation of piezoelectric polarization charges within the ZnO thin films, thus leading to a deviation in the steady state current values and the sensor transducing properties for different deposition temperatures.

The internal chemistry of the ZnO thin film with the different levels of oxidation of its atoms and the stoichiometry of these ones has an impact on the electronics properties and the control of the semiconducting properties necessary to set a Schottky junction. The XPS survey spectrum, shown in Fig. 3.13, corresponds to the bulk of a ZnO thin film deposited by ALD at 80 °C.

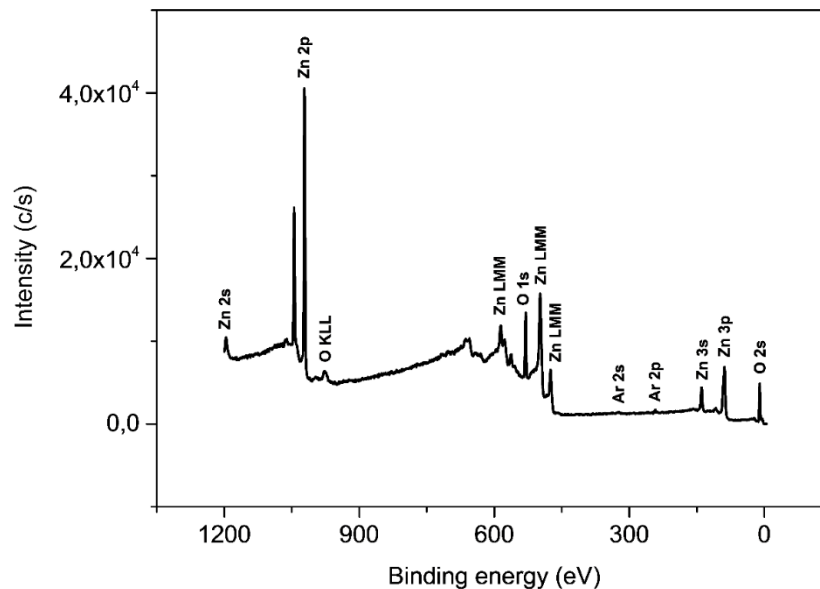


Figure 3.13. XPS survey spectrum of a ZnO thin film deposited by ALD at 80 °C, obtained in the bulk of the thin film after Ar⁺ etching on the top surface.

Apart from the Ar 2s and Ar 2p peaks, related to the implantation of Ar⁺ ions due to the use of an Ar⁺ ion beam for depth profiling, all other peaks are related to Zn and O chemical elements, which confirms the high quality of the created ZnO thin films with negligible levels of contaminants as carbon originating from remaining ligands of the DEZ precursor. The evolution of the O:Zn atomic ratio obtained by XPS depth profiling for ZnO thin films deposited in these conditions is displayed in Fig. 3.14.

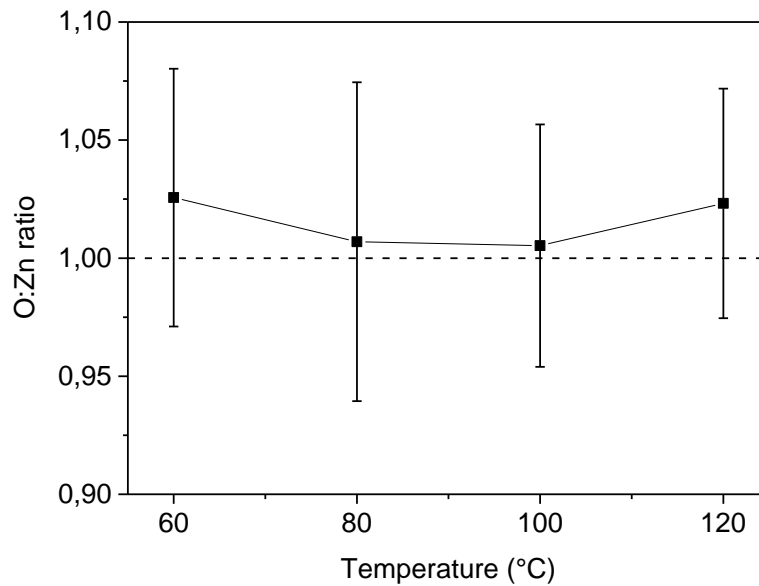


Figure 3.14. Evolution of the O:Zn atomic ratio obtained by XPS depth profiling for the ZnO thin films by ALD for different deposition temperatures.

The O:Zn ratio is close to unity for every temperature studied between 60 °C and 120 °C. That ratio is expected to decrease when the temperature is increased to values higher than 150 °C [8,17]. The deposition of ZnO thin films by ALD at low temperatures thus leads to a privileged stoichiometric growth, where the formation of ZnO defects, more precisely oxygen vacancies and zinc interstitials, is considerably reduced. This reduction in the defects in turn contributes to decrease the intrinsic n-type carrier concentration of the ZnO thin films, within the aim of reaching appropriate values for a Schottky barrier formation. This modulation of the electron concentration with the deposition temperature, linked with the amount of defects, has a direct impact on the material's electrical parameters. Reportedly, decreasing electron concentrations values in ZnO thin films are typically accompanied by an increase in the electrical resistivity and a decrease in the electron mobility values [14,16,35].

In this study, we aimed to find the appropriate balance between these different electrical parameters in order to control the Schottky barrier. The resistivity of the ZnO thin films created was measured by the conventional four-points probe method on glass substrates [40]. This method eliminates the lead and contact resistance, which is an advantage for measurements at low-resistance values. However, it leads to inaccurate measurements for higher contact resistance values than 1 kΩ [41], which

is linked to the very low source current value in the order of nanoAmperes used. The resulting voltage measurements are thus more sensitive to noise and present unstable values, also due to the slow decay of the charges [42]. To overcome the limit of detectable resistivity values by the four-point probe method, (I-V) curves were performed with an electrometer by a two-points probe on ZnO thin films deposited on glass substrates at 60 °C, 80 °C and 100 °C. The resistance was thus evaluated by extracting the slope of the obtained linear (I-V) curves. The resistivity (by four-points probe) and resistance (by (I-V)) values obtained as a function of the deposition temperature are presented in Fig. 3.15.

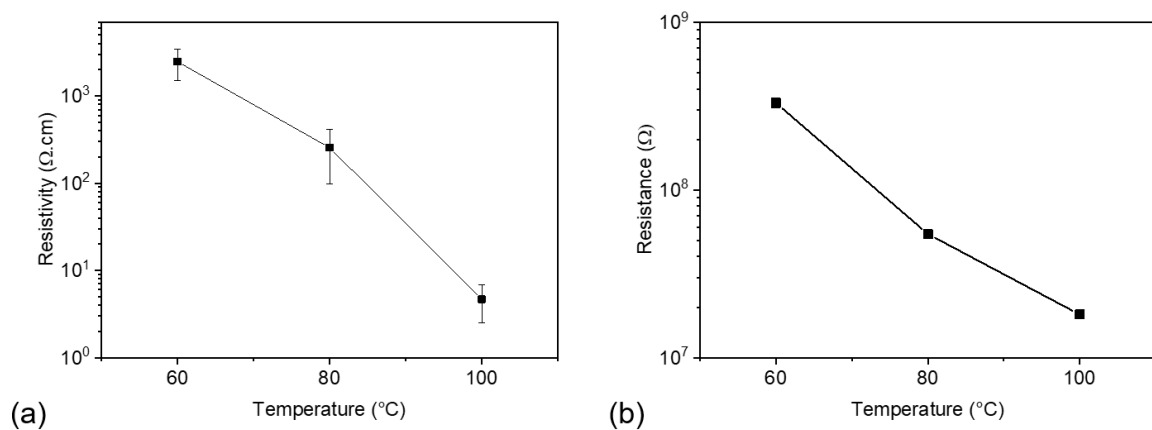


Figure 3.15. (a) Evolution of the resistivity as a function of the deposition temperature for 150 nm thick ZnO thin films deposited at 60 °C, 80 °C and 100 °C on glass substrates, measured by the four-points probe method; (b) Evolution of the resistance as a function of the deposition temperature for 150 nm thick ZnO thin films deposited at 60 °C, 80 °C and 100 °C on glass substrates, measured by the two-points probe method by the means of (I-V) with an electrometer. The ZnO films were contacted with tungsten probes with a constant lateral spacing of 1 mm, resulting in ohmic W/ZnO/W junctions.

Both the resistivity, estimated by the four-points probe method, and the resistance of ZnO thin films, calculated by the two-points probe method, increase from average values of 4.7 Ω.cm and 18 MΩ, respectively, at 100 °C, to 255.3 Ω.cm and 55 MΩ at 80 °C, reaching 2473.4 Ω.cm and 330 MΩ at 60 °C. These results confirm the increase of the resistivity and resistance for lower deposition temperatures by ALD. This last statement is well-reported and documented in the literature [8,43,44]. Additionally, Hall effect measurements (Ecopia HMS-3000) were performed to extract the electron concentration and the electron mobility of the ZnO thin film samples on glass substrates, which consists of the most important and direct technique used for polycrystalline thin films. At 100 °C, the electron concentration was estimated at an

average value of $8 \times 10^{16} \text{ cm}^{-3}$, with an average mobility of $9 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$. These values consistently decreased for measurements taken at lower deposition temperatures. However, due to the high resistivity of the ZnO thin films, the resulting Hall voltage was inaccurate and yielded inconsistent values for the electron concentration and the electron mobility, as reported by F. Werner for low mobility polycrystalline thin films [45]. In a recent study, E. Przewdziecka et al. [46] showed that both the electron concentration and mobility were reduced at lower ALD deposition temperatures. They stated that the electron mobility of ZnO thin films grown by ALD at low temperatures was dominated by grain-boundary scattering for low electron concentrations (i.e. between 10^{15} cm^{-3} and 10^{17} cm^{-3}). E. Guziewicz et al. [17] reported an electron concentration value of 10^{17} cm^{-3} together with a mobility of $17 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ for polycrystalline ZnO thin films deposited by ALD at $100 \text{ }^\circ\text{C}$ with similar precursors, with a further decrease of the electron concentration value in the 10^{16} cm^{-3} range at a deposition temperature of $80 \text{ }^\circ\text{C}$. Similarly, S. Kwon et al. [44] reported a decrease of both the electron concentration and the electron mobility from $1.56 \times 10^{17} \text{ cm}^{-3}$ and $56.43 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$ at $110 \text{ }^\circ\text{C}$ to $1.76 \times 10^{14} \text{ cm}^{-3}$ and $6.435 \text{ cm}^2 \cdot \text{V}^{-1} \cdot \text{s}^{-1}$, respectively, at $70 \text{ }^\circ\text{C}$.

The above-mentioned results further confirm that low temperature ALD depositions lead to electron concentration values of the ZnO thin films being well appropriated for Schottky junctions. However, decreasing the deposition temperature below $80 \text{ }^\circ\text{C}$ leads to a substantial decrease of the mobility, which might be detrimental for further device's application at high frequencies. In order to circumvent the measurement inaccuracy linked with higher resistivities, the electron concentration is determined via a fitting of the sensors' electrical characteristics, provided in Chapter 4.

3.4. Impact of the introduction of molecular oxygen

In the prior art, S.H.K. Park et al. [47] in 2004 proposed the use of molecular oxygen gas pulsing during the ALD sequence to control a main (002) crystalline orientation of the ZnO polycrystalline film. In the prior art, T. Nguyen et al. [8] in 2020 proposed a systematic study of the role of both the molecular oxygen gas pulsing time and the

growth temperature to modulate the privileged crystalline orientation and the electrical properties of the ZnO polycrystalline film made by ALD.

The semiconducting thin layer made by ALD represents a crucial stage to modulate the series resistance of the diode junction, but also the mobility and the density of the free carriers, as well as the resistivity inside the material by an interplay between the crystalline structure and the Zn:O stoichiometry. For a given temperature of growth on top of the polymer surface, we introduced the use of molecular oxygen gas pulsing in the ALD processing to control these electronic parameters.

In the conventional process, the deposition cycle consists of a diethylzinc (DEZ) pulse followed by a pulse of deionized water, while using argon as an inert purging gas. The variant of the process presented in this section consists in the introduction of a molecular oxygen gas pulse in between the DEZ and the deionized water pulses. The purging time of the molecular oxygen gas pulse has been set to 20 s to avoid any potential parasitic CVD reaction inside the ALD reactor. Particular attention has been given concerning the purity of the molecular oxygen gas used. Alphagaz 2 Oxygen has been used with a global purity ≥ 99.9995 % mol and $\text{H}_2\text{O} \leq 0,5$ ppm.mol. The oxygen gas carrying line has been filtered with a cartridge to avoid any unwanted reaction between moisture contamination and DEZ.

The incorporation of molecular oxygen within the ALD process is leading to a preferred (002) crystalline orientation with fine columnar crystallites at a temperature of 100 °C and above, as observed on Fig. 3.16.

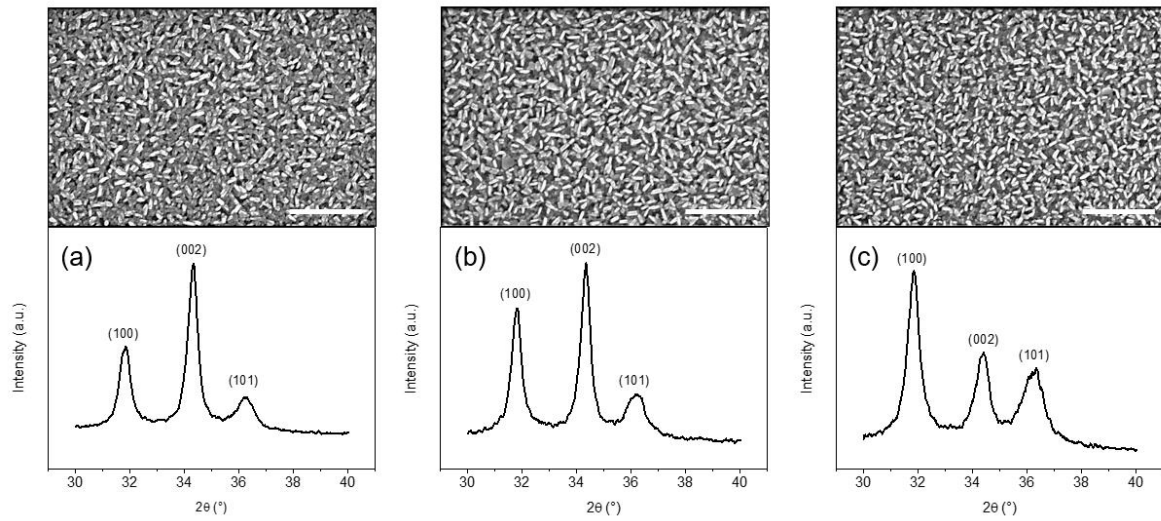


Figure 3.16. SEM top view images and associated GI-XRD diffraction patterns ($\omega=0.3^\circ$) of ZnO thin films grown on Si substrates in the presence of molecular oxygen, at a deposition temperature of (a) 100 °C, (b) 80 °C and (c) 60 °C. The obtained ZnO thin films were deposited with the same number of ALD loops (1000). The scale bar corresponds to 300 nm.

A transition is occurring below 100 °C, where a different distribution of grain orientations can be observed, shared between the (100), (002) and (101) crystalline orientations. This is further confirmed by SEM top view images showing a distribution of wedge-like shaped crystallites parallel to the substrate and of fine columnar crystallites perpendicular to the substrate.

A substantial increase of the resistivity for the ZnO thin films deposited with oxygen gas can be noticed from Fig. 3.17, which is attributed to the decrease in the concentration of oxygen vacancies [8].

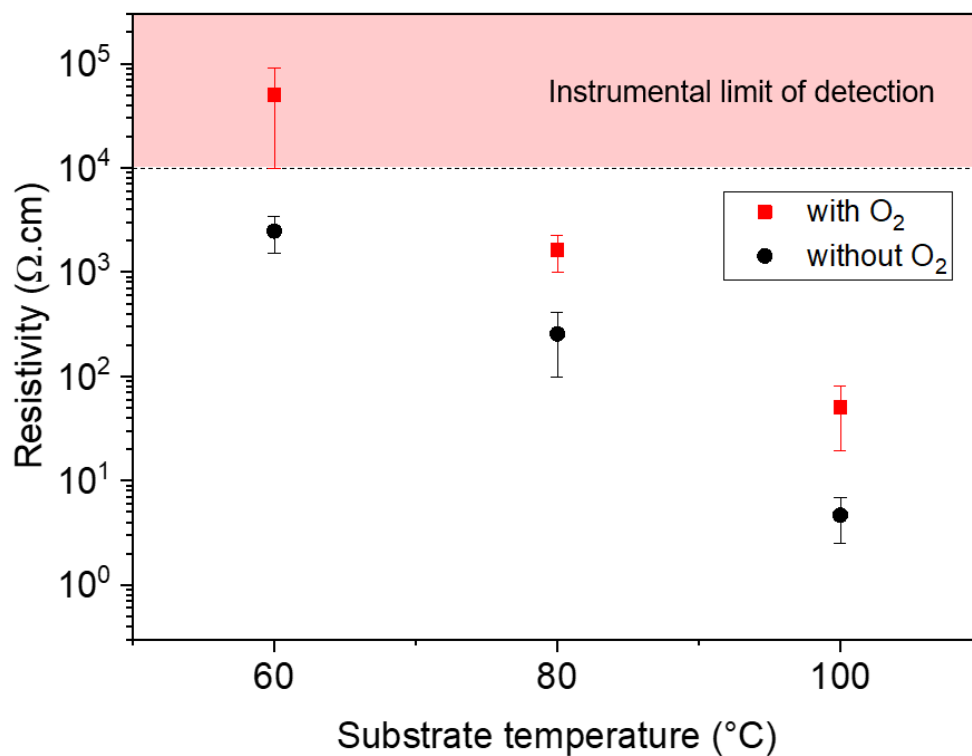


Figure 3.17. Resistivity (4-points probe) of ZnO thin films grown with and without molecular oxygen pulsing on glass substrates, for ALD deposition temperatures between 60 °C and 100 °C.

This is correlated with the O:Zn ratio monitoring on Fig. 3.18 for ZnO thin films deposited using oxygen gas pulsing during growth with ratio superior to those of ZnO thin films processed without oxygen gas (cf. Fig. 3.14).

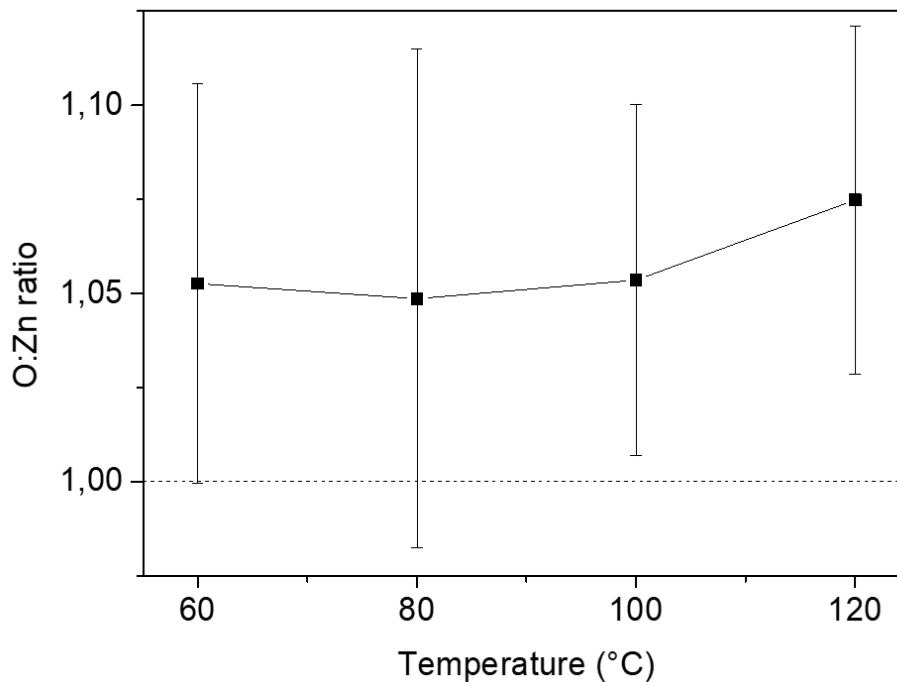


Figure 3.18. Evolution of the O:Zn atomic ratio obtained by XPS depth profiling for the deposited ZnO thin films using oxygen gas pulsing during growth by ALD for different deposition temperatures.

Concerning piezoelectric-based applications as for piezotronic strain sensors, ZnO thin films are required to present a preferred (002) crystalline orientation together with a high resistivity or low leakage current to ensure the highest output voltages. This alternative ALD process thus allows to tune the structural and electrical characteristics of the deposited ZnO thin films by incorporating molecular oxygen gas pulsing during the ALD loops, with properties adapted for piezoelectric applications on a different temperature range, i.e. for temperatures above 100 °C.

3.5. Conclusion

In this chapter we described the optimized experimental parameters of deposition for controlling the ZnO thin films structural, chemical and electrical properties by thermal atomic layer deposition (ALD). This work allows to get reproducible processes to get the mandatory control of the Schottky barrier and the related piezotronics junction to obtain a highly sensitive strain sensor on a polymeric substrate as we will described in the next chapters 4 and 5.

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4. Polymeric cantilevered piezotronic strain sensors

This chapter is focused on the analysis of the polymeric cantilevered piezotronic strain sensors. The first section of this chapter aims at describing the sensors' design and the different microfabrication steps performed by means of maskless photolithography, as well as the main issues faced during their processing. The electrical properties of the sensors are then thoroughly detailed, by first identifying the main conduction mechanism in the metal-semiconductor-metal (M-S-M) junctions. Crucial material's parameters are extracted by fitting the sensors' electrical characteristics. Additionally, we report on the evidence of negative capacitance phenomena and capacitance modulation by the application of light and mechanical strain. The last section is focused on the integration and testing of the piezotronic strain sensors, where the electromechanical transducing properties of the sensors are reported and discussed. The noise analysis of the piezotronic sensors is subsequently detailed.

A part of these results have been published in the peer-reviewed journals *Sensor and Actuators A* [1] and *Sensors* [2].

4.1. Microfabrication

4.1.1. Design

The piezotronic strain sensors consist of Pt/ZnO/Pt Schottky junctions, integrated at the clamped area of millimetre-sized polyimide cantilevers. Schottky junctions were made by ALD deposition of 300 nm ZnO thin films on top of 200 nm Pt interdigitated

electrodes (IDE). A general top view representation with the corresponding sensors' dimensions is provided in Fig. 4.1, alongside with a detailed view of the sensitive area (i.e. where the zinc oxide pad surrounds the interdigitated metal electrodes to create Schottky interfaces). An encapsulation layer of SU8 resist is deposited on top to protect the ZnO/Pt junction against the environmental conditions and to maintain their long-term electrical performance.

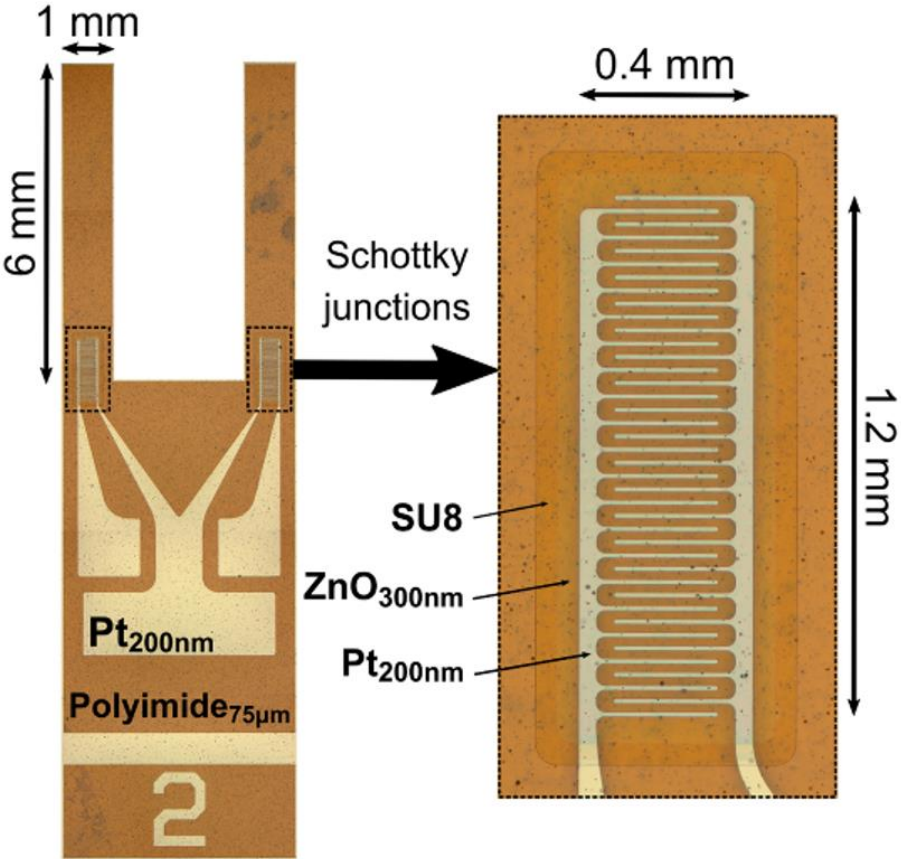


Figure 4.1. Top view representation of a piezotronic strain microsensors. The black dashed line box details the area of the interdigitated electrodes surrounded by the ZnO pad.

A single cantilever might be influenced by several parameters in his direct environment, such as vibrations and thermal drift. Within this scope, two polyimide cantilevers were processed and are localized at the right and left-hand side of the sensor for the obtention of differential measurements. Recording difference signals with respect to a reference cantilever allows to effectively remove such disturbances [3], leading to an increase of the signal-to-noise ratio (SNR) and the resulting sensitivity of the piezotronic sensors.

Another motivation linked with the use of polyimide cantilevers lies in the lower Young's modulus of polymeric materials in the order of 2 to 4 GPa, typically two orders of magnitude lower than for conventional silicon-based materials, which contributes to reduce their stiffness and increase their sensitivity [4]. The dimensioning of the cantilevers is another critical aspect as their stiffness must remain inferior to approximately 10 N.m^{-1} , which represent realistic mechanical performances comparable with strain induced in AFM (Atomic Force Microscopy) cantilevers [5,6]. The stiffness k of a cantilever, also named spring constant, can be denoted as follows:

$$k = \frac{3 \cdot Y \cdot I_{\text{cantilever}}}{L^3} \quad (4.1)$$

Where Y is the Young's modulus of the cantilever, L is the length of the cantilever and $I_{\text{cantilever}}$ is the moment of inertia of the cantilever cross-section.

For a rectangular cantilever beam, the moment of inertia $I_{\text{cantilever}}$ can be expressed as [7]:

$$I_{\text{cantilever}} = \frac{w \cdot t^3}{12} \quad (4.2)$$

With w and t being the width of the cantilever and its thickness, respectively.

Consequently, the stiffness of a rectangular cantilever is expressed accordingly as:

$$k = \frac{Y \cdot w \cdot t^3}{4 \cdot L^3} \quad (4.3)$$

With the corresponding numerical values linked with the polyimide cantilevers properties ($Y = 3 \text{ GPa}$) and dimensions detailed on Fig. 4.1 with a body thickness of $75 \mu\text{m}$, the numerical application yields:

$$k = \frac{(3 \times 10^9) \cdot (1 \times 10^{-3}) \cdot ((75 \times 10^{-6})^3)}{4 \cdot ((6 \times 10^{-3})^3)} = 1.46 \text{ N.m}^{-1}$$

This results in an appropriate stiffness value for the polyimide cantilevers, adapted for AFM scanning probe applications in contact mode such as force spectroscopy or imaging [8].

Moreover, the strain ε generated in the clamped area of the cantilevers was calculated using the following equation [9]:

$$\varepsilon = \frac{3}{2} \cdot \frac{(t - t_s)(2L - L_s)}{L^3} \cdot d \quad (4.4)$$

With t and L having the same meaning as before, t_s being the sensor thickness, L_s the sensor length, and d the deflection imposed on the cantilever relative to the contact point (at length L). It is worth noting that the calculated strain ε is inversely proportional to the cube of the length L at the contact point of the cantilever end. Consequently, the strain ε generated in the clamped area of the cantilevers has been calculated with equation 4.4 derived from Stoney equation as a function of deflections values ranging between 1 nm and 1 cm, for three different contacts points at lengths L of the cantilever (2 mm, 4 mm and 6 mm, the latter value corresponding to the tip end of the polyimide cantilever). The resulting values are presented in Fig. 4.2, using t_s as 2 μm and L_s as 860 μm from the sensing area detailed in Fig. 4.1.

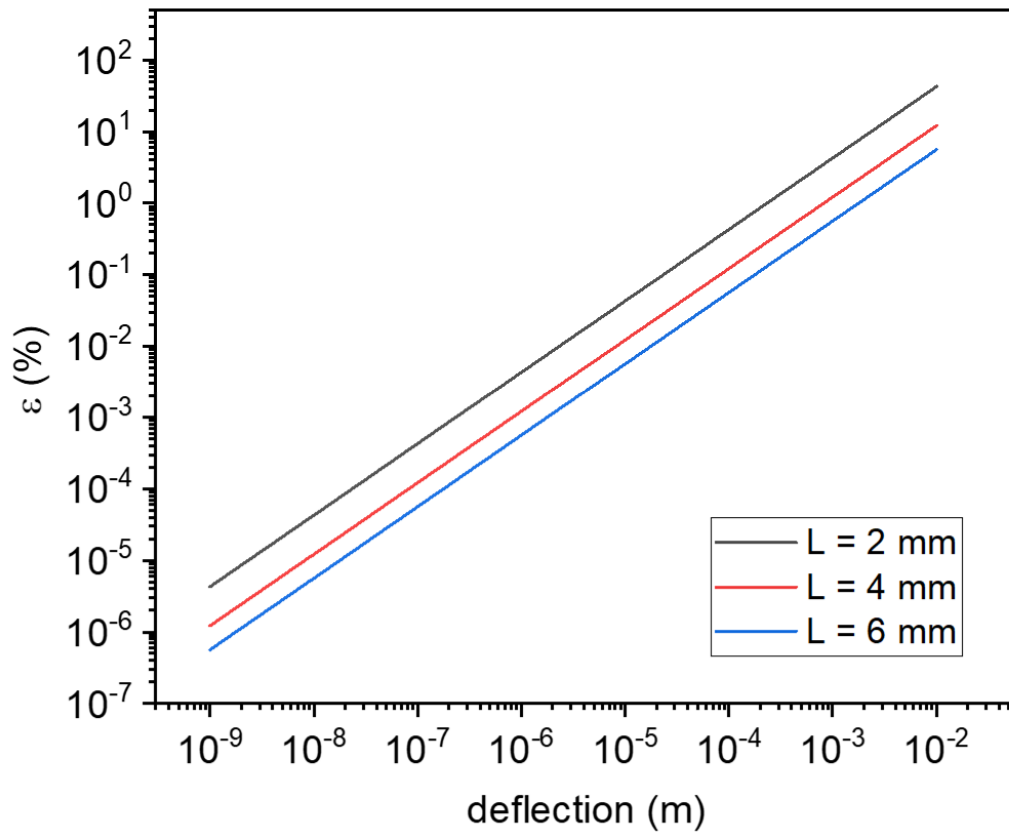


Figure 4.2. Log-log plot of the calculated strain ε generated in the clamped area of the cantilevers as a function of deflections values ranging between 1 nm and 1 cm, for three different contacts points at lengths L (2 mm, 4 mm and 6 mm) of the cantilever.

Furthermore, as mentioned earlier, the platinum metal electrodes are organized as two interdigitated sets, used to increase the number of parallelized sensing elements and maximize the size of the Schottky contact interface, which leads to the creation of several metal-semiconductor (M-S) back-to-back Schottky diodes within the area defined by the ZnO pad. The equivalent circuit model involving the interdigitated electrodes is presented in Fig. 4.3.

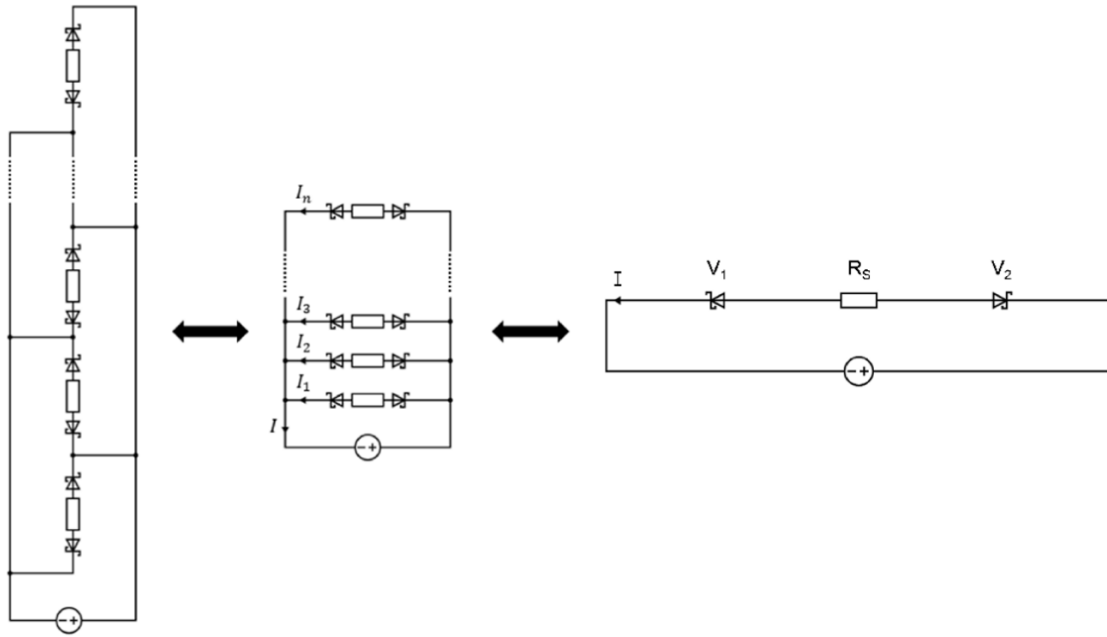


Figure 4.3. Equivalent circuit model of the metal-semiconductor-metal structure with interdigitated electrodes.

The total current I of the device corresponds to the sum of each individual back-to-back Schottky diode current, following the equation:

$$I = I_1 + I_2 + I_3 + \dots + I_n = \sum_{i=1}^n I_i \quad (4.5)$$

Where n corresponds to the number of back-to-back Schottky diodes created by the two sets of interdigitated platinum electrodes within the area defined by the ZnO pad. Since all the sets of back-to-back diodes were processed in a similar way during the same processing stages, the current flowing out of every metal-semiconductor-metal (M-S-M) structure is considered to be equal ($I_1 = I_2 = I_3 = \dots = I_n$).

The equivalent circuit model can thus be represented by a single back-to-back Schottky diode corresponding to the sum of every M-S-M diode. This is linked to the use of the same planar metal bottom electrode layer, as well as to the uniformity the ZnO coating and reproducibility of its electrical properties by the mean of the ALD process. The electrical properties of this equivalent circuit model will be detailed within the next section. The dimensioning of the IDE is particularly important as several geometrical parameters can be modified and influence the resulting number of parallelized sensing elements as well as the Schottky contact area with the ZnO thin

film. A generic interdigitated electrodes planar structure is illustrated in Fig. 4.4, together with the main geometrical parameters defining such kind of structure.

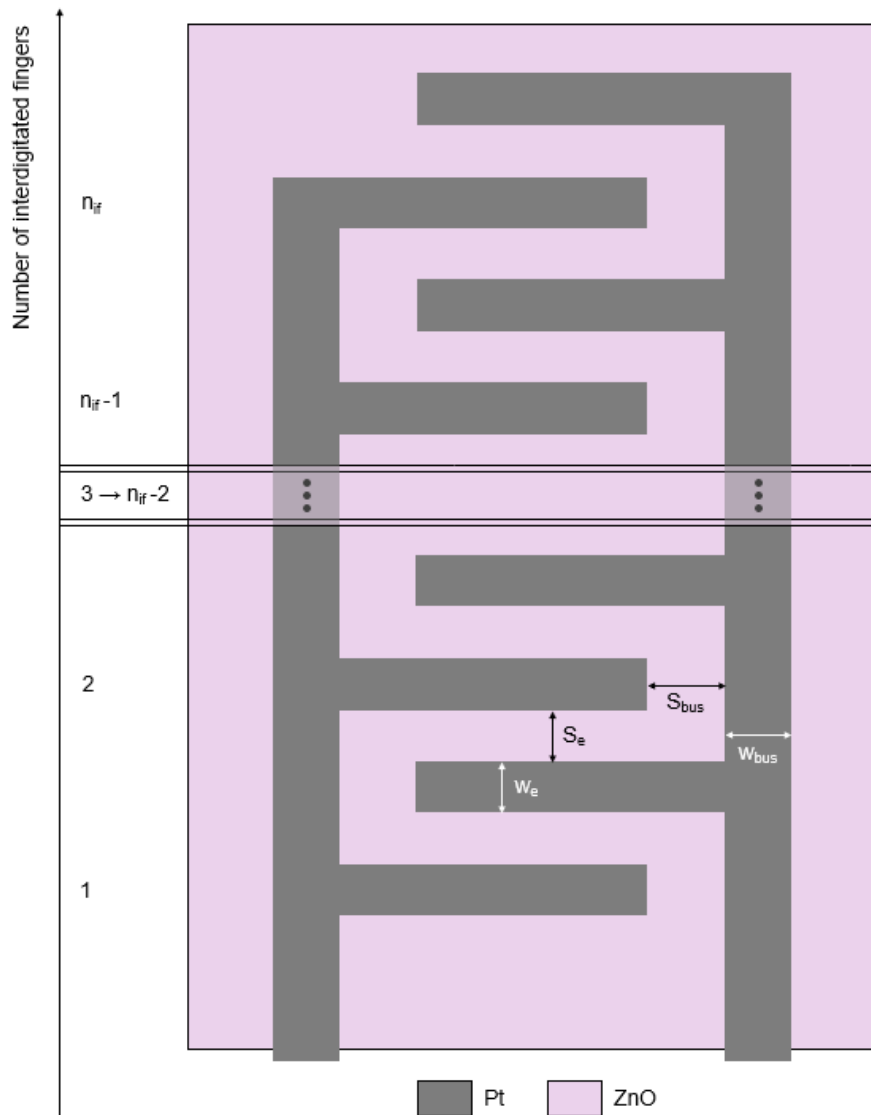


Figure 4.4. Top-view representation of a generic interdigitated (IDE) planar structure.

Where w_{bus} is the IDE bus width, S_{bus} is the IDE finger-bus spacing, w_e is the finger width, S_e is the IDE inter-finger spacing and n_{if} is defined as the total number of interdigitated fingers on a single set. Within this scope, four different IDE layouts have been designed, their respective parameters being reported in Table 4.1:

Geometrical parameters \ Reference design	"1"	"2"	"3"	"4"
w_{bus} [μm]	40	40	40	40
S_{bus} [μm]	40	40	40	20
w_e [μm]	10	10	10	5
S_e [μm]	10	20	30	5
n_{if}	30	20	15	59

Table 4.1. Geometrical parameters defining the different IDE structures.

The main difference in these designs arise from the inter-finger spacing S_e , thus impacting the total number of interdigitated fingers n_{if} , which allows for a modulation of the Schottky contact interface and the number of parallelized sensing elements. The corresponding impact on the sensors' electrical properties is reported within the next section.

Furthermore, the placement of the sensitive area (i.e. the Pt IDE and the patterned ZnO and SU8 layers) was localized where the polyimide cantilever is clamped to the sensor to maximize the stress/strain concentration, as previously shown in Fig. 4.1. To further confirm this statement, numerical simulations were performed with COMSOL software. A 2D model was used, representing a longitudinal cross-section of the whole structure, consisting of the sensitive area, the polyimide cantilever and the printed circuit board (PCB) upon which the piezotronic sensor is stucked for further integration. A general view of the computational domain is depicted in Fig. 4.5(a), together with an enclosed view on the sensitive area in Fig. 4.5(b), with the corresponding dimensions used within the simulation.

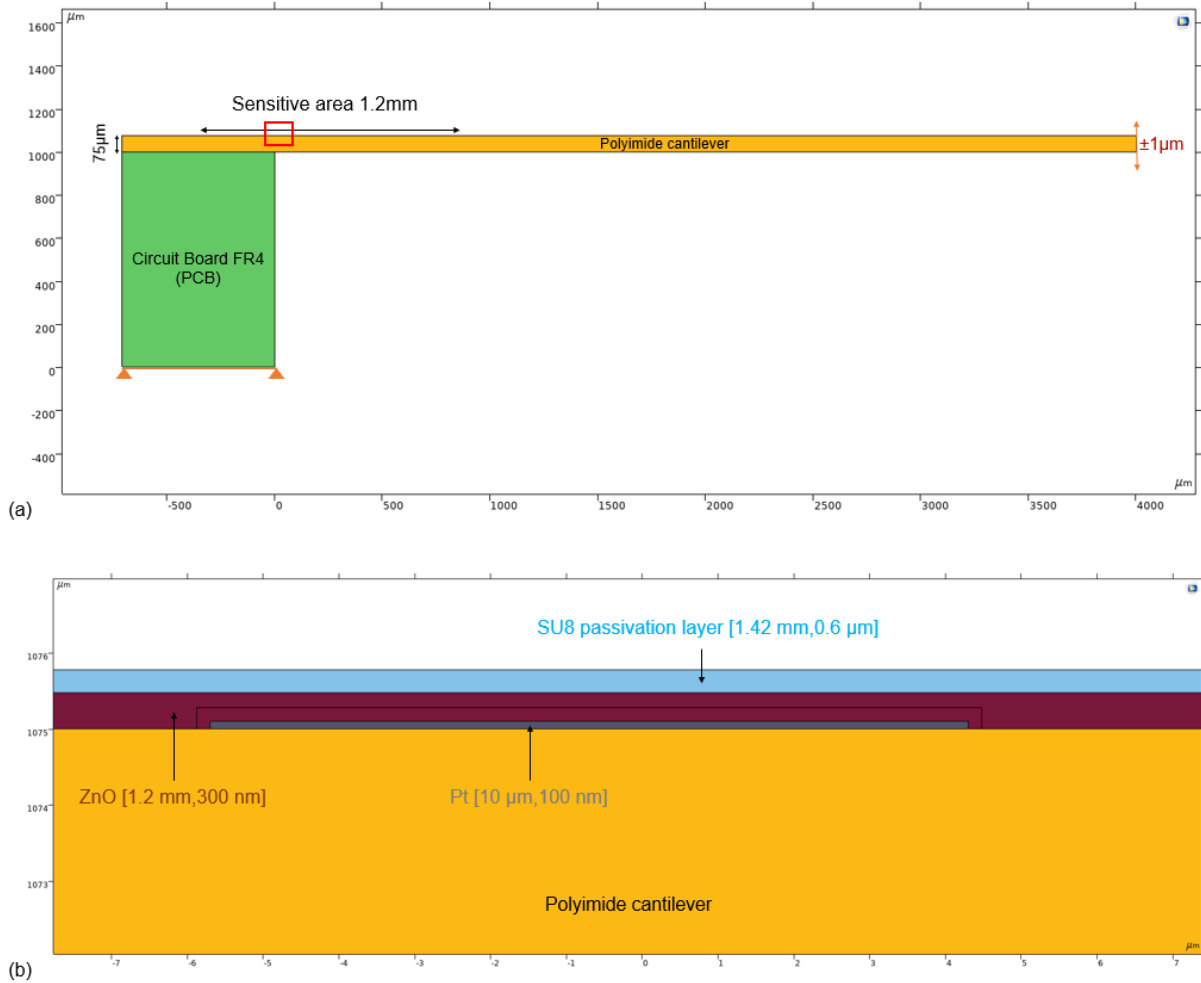


Figure 4.5. 2D Computational domain of the structure's longitudinal cross-section. (a) General view of the structure with corresponding materials and dimensions used within the simulation. The outlined red box localized on the polyimide cantilever corresponds to the area represented in the enclosed view below. (b) Enclosed view on the sensitive area consisting of a Pt metal electrode and a ZnO pad encapsulated on the SU-8 passivation layer.

The resulting volume-stretching rate inside the ZnO layer at the area where the polyimide cantilever is clamped to the sensor is represented on Fig. 4.6. The volume-stretching rate, represented on the z-axis, was numerically simulated as a function of both the cantilever's tip displacement between $-1\mu\text{m}$ and $1\mu\text{m}$, represented on the x-axis, and the distance along the ZnO layer on the y-axis.

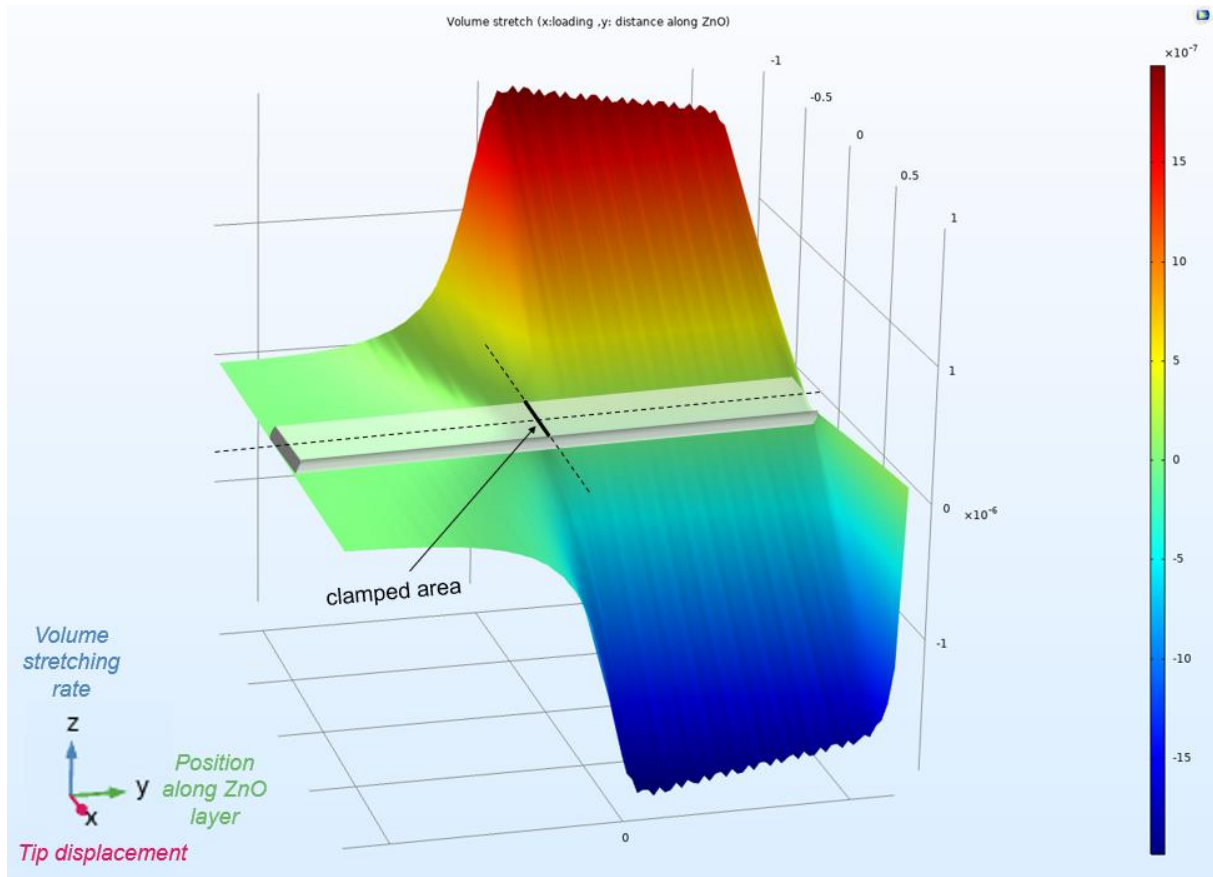


Figure 4.6. Surface map showing the volume-stretching rate (z-axis) picked up over a line cut spanning the ZnO layer (y-axis) against the tip displacement (x-axis). An illustration of the cantilever with the localization of its clamped area along the y-axis was added to the surface map for a better understanding of the graph.

It can be observed from Fig. 4.6 that the ZnO layer is not affected by the mechanical deformation on the clamped area of the sensor. However, the volume-stretching rate abruptly increases to its maximum value after reaching the limit of the clamped area (set as the reference “0” value along the y-axis). From that point, the volume-stretching rate then decreases slightly as the distance along the cantilever is increased (i.e. as the distance from the clamped area is increased). These numerical simulations thus clearly demonstrate that the strain reaches its maximum value at the area where the polyimide cantilever is clamped to the sensor. Nonetheless, as the polyimide cantilevers are released by manual dicing with the help of a precision scalpel blade, manual operation could induce mechanical damage to the ZnO layer and the Pt metal electrodes, especially around the clamped area of the polyimide cantilevers. To avoid a rupture of the electrical continuity on the thin Pt stripes leading to the interdigitated

structure, the sensitive area was thus slightly displaced towards the cantilever chip body by a distance of ~ 0.4 mm.

4.1.2. Process flow

The microfabrication process flow of the sensors on the flexible polyimide substrate with interdigitated electrodes is illustrated in Fig. 4.7. The different processing steps are further detailed within Appendix A, with the corresponding experimental parameters employed and specific guidelines to follow.

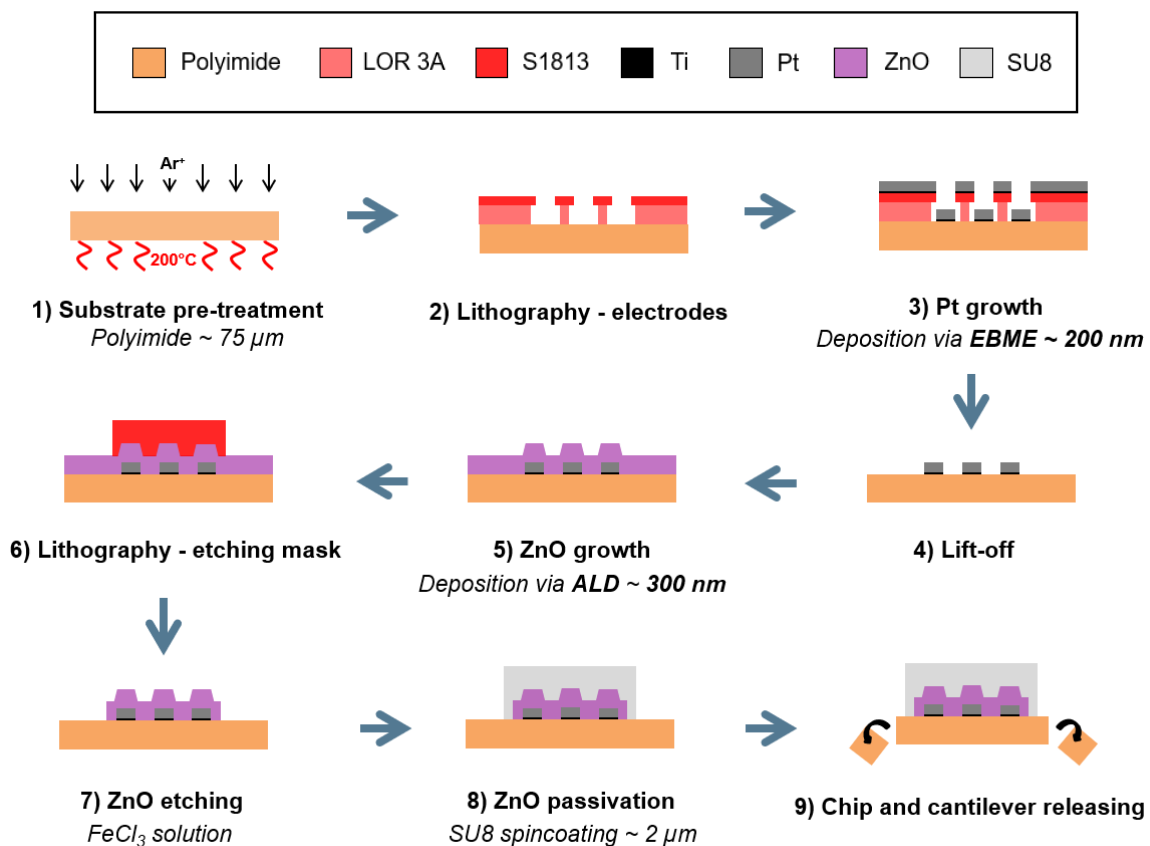


Figure 4.7. Microfabrication process flow of the piezotronic strain microsensors including the deposition of the ZnO layer by ALD.

4.1.3. Troubleshooting

The micro processing of composite structures stacking organic and inorganic materials with different mechanical and thermal behaviours represent a major challenge to

realise a functional device. This section aims at reporting some specific issues faced during the different microfabrication processing steps and detailing the solutions adopted, if any. More specifically, the mitigation of cracks propagation due to thermal shocks is detailed within Appendix A.

- Choice of the metal electrodes

Several metals can be readily used to form a Schottky junction with n-type ZnO thin films. To ensure the formation of a Schottky junction at the interface with the ALD-deposited ZnO thin films, a high work function metal was thus targeted. Within this scope, the most frequently used metals with n-type ZnO to form Schottky junctions include Pt, Ir, Pd, Au and Ag [10]. Nonetheless, it should be noted that a wide energy range is observed experimentally concerning the Schottky barrier height between the same metal and ZnO, depending on the surface preparation and the presence of interface states. The use of Ag as a metal electrode was not pursued due its oxidation in air. Ag is a metal which oxidizes easily and where the resulting Schottky barrier height depends on the degree of oxidation, leading to a lack of reproducibility and a drift of the electrical properties over time [10].

Furthermore, prior to the microfabrication processing of interdigitated electrodes, the electrical properties of local metal-ZnO junctions were tested with a simple experimental configuration. As detailed in the previous chapter, the electron concentration is the key factor to control the Schottky interface at the M-S interface; the most influent parameter on this concentration being the ALD deposition temperature. The objective of these measurements was thus not to extract the materials parameters from the (I-V) characteristics, as the Pt/ZnO/Pt interfaces integrated in the piezotronic sensors result in a complex structure consisting of back-to-back Schottky junctions. Rather, the aim was to assess the presence of a Schottky behaviour on the interfaces between the ALD-grown ZnO thin films at different temperatures, together with Pt and Au metal electrodes. More precisely, these experiments consisted in the deposition of Au or Pt bottom electrodes (100 nm) by EBME on a polyimide substrate, followed by the ZnO thin-films (150 nm) deposition by ALD at temperatures of 100°C, 80°C and 60 °C. Au or Pt top electrodes (100 nm) were

then deposited by EBME using a shadow mask of TLM (Transmission Line Method) electrodes array. Dry etching was subsequently performed by RIE on the ZnO layer locally protected by a hard mask to reveal and access the bottom electrode for subsequent electrical characterization. The metal-ZnO junctions were locally contacted with tungsten (W) tips via a probe station and connected to an electrometer to characterize the resulting W/ZnO/Au and W/ZnO/Pt junctions in the top and bottom configurations, with the positive bias applied on the Pt or Au metal electrode, as illustrated by Fig. 4.8.

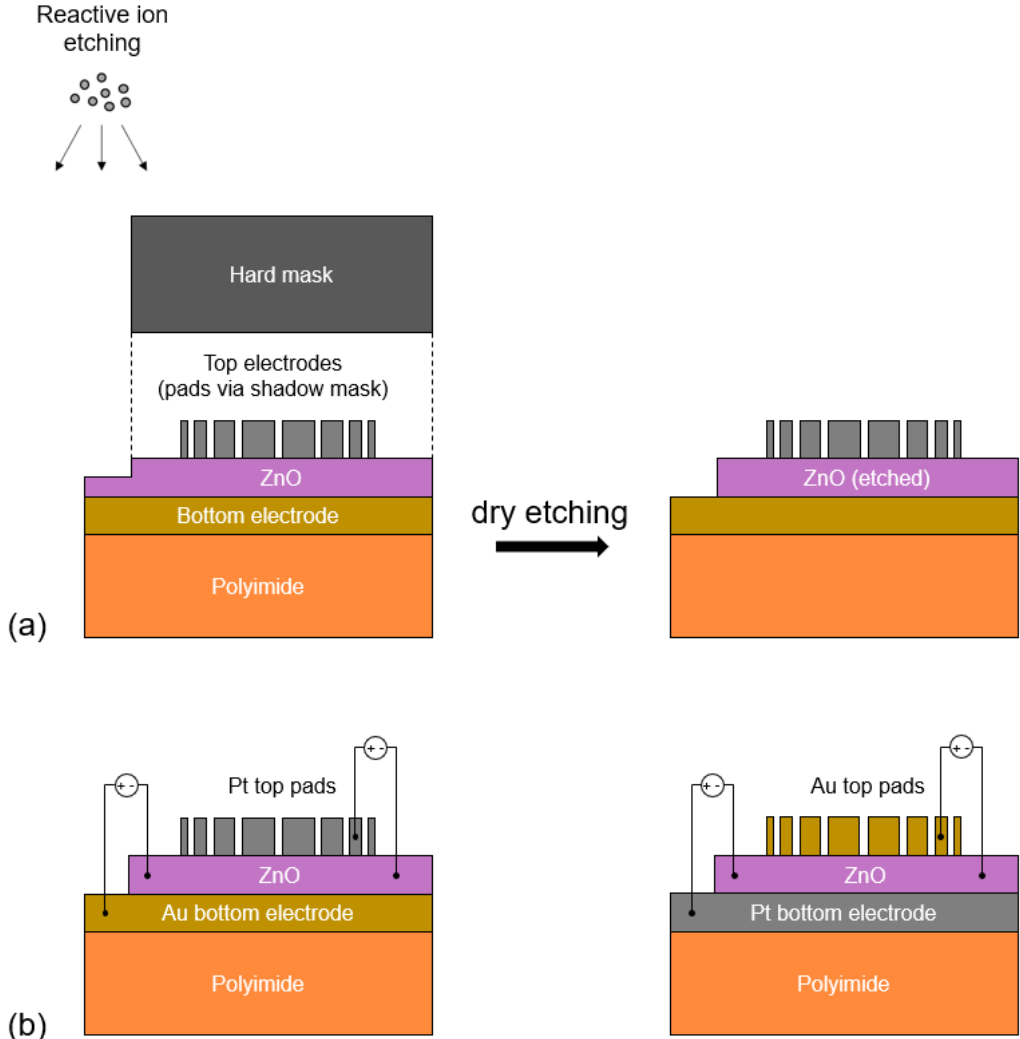


Figure 4.8. Experimental multi-layer stack used to probe the electrical behaviour of Au and Pt with ALD-deposited ZnO thin films. (a) Illustration of the experimental multi-layer stack with the dry etching step performed on the ZnO layer to reveal the bottom electrode. (b) Illustration of the two experimental configurations tested with Pt and Au metal electrodes as bottom or top electrodes, with the corresponding electrical connections performed with W tips.

According to the thermionic emission theory by Schottky [11], the current I flowing through a metal/semiconductor junction under a forward bias V can be written as:

$$I = A \cdot A^* \cdot T^2 \cdot e^{\left(\frac{-q \cdot \phi_B}{k_B \cdot T}\right)} \cdot \left[e^{\left(\frac{q \cdot (V - I \cdot R_S)}{\eta \cdot k_B \cdot T}\right)} - 1 \right] \quad (4.6)$$

Where ϕ_B is the Schottky barrier height, A the Schottky contact area, A^* the Richardson constant [12], q the elementary charge, T the temperature, k_B the Boltzmann constant, R_S the series resistance of the semiconductor and η the ideality factor. By assuming that the electron concentration value of the ALD-grown ZnO thin films is adequate for the formation of a Schottky junction, the presence of an exponential dependence between the applied bias voltage V and the resulting current I would thus validate the presence of a Schottky barrier in the locally probed ZnO/metal junctions.

Within this scope, the (I-V) characteristics of W/ZnO/Pt junctions (with Pt as a bottom electrode) for a 150 nm thick ZnO thin film deposited by ALD at 80 °C are displayed in Fig. 4.9(a). The curve exhibits typical diode characteristics, with a non-linear (I-V) behaviour for the forward bias and low current values for the reverse bias. Additionally, the semilogarithmic (I-V) characteristics of forwardly biased W/ZnO/Pt junctions (with Pt as a bottom electrode) for 150 nm thick ZnO thin films deposited by ALD at 100 °C, 80 °C and 60 °C are displayed in Fig. 4.9(b). As observed, the (I-V) characteristics follow a similar trend but their current values are decreased by approximately one order of magnitude as the ALD deposition temperature is decreased from 100 °C to 80 °C and 60 °C. This decrease in the current values with lower deposition temperatures is linked to the decrease of the free electron concentration, leading to higher resistivities and series resistances values for the ZnO thin films, as detailed in the previous chapter.

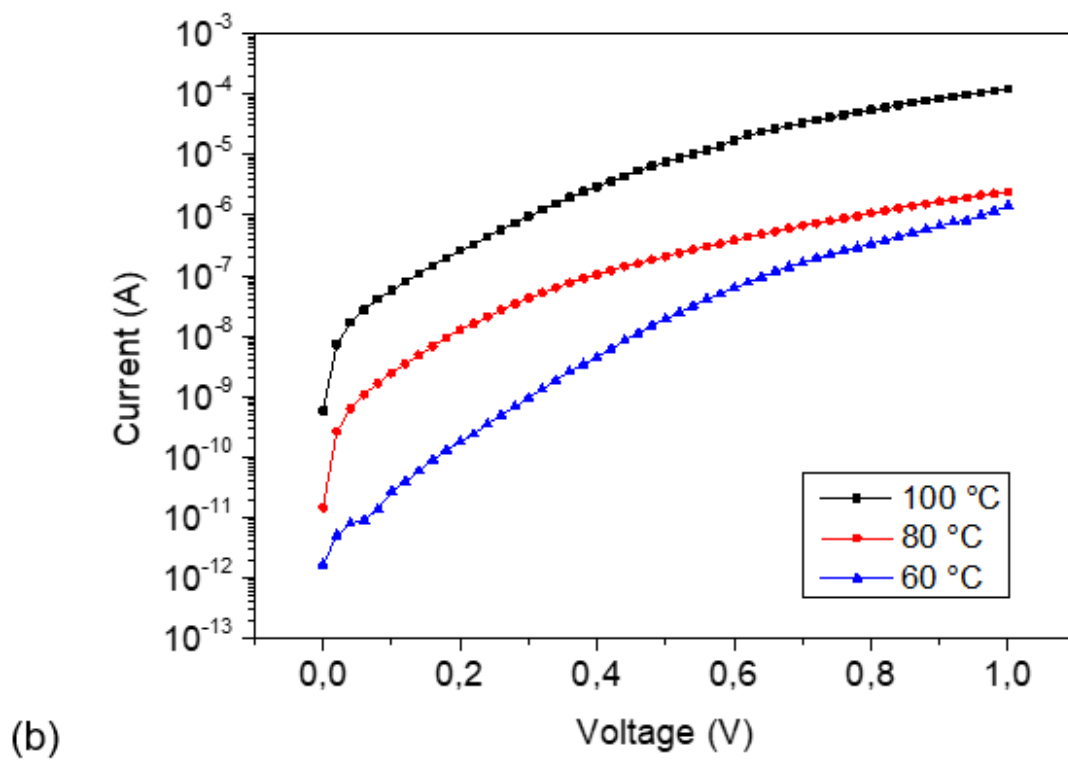
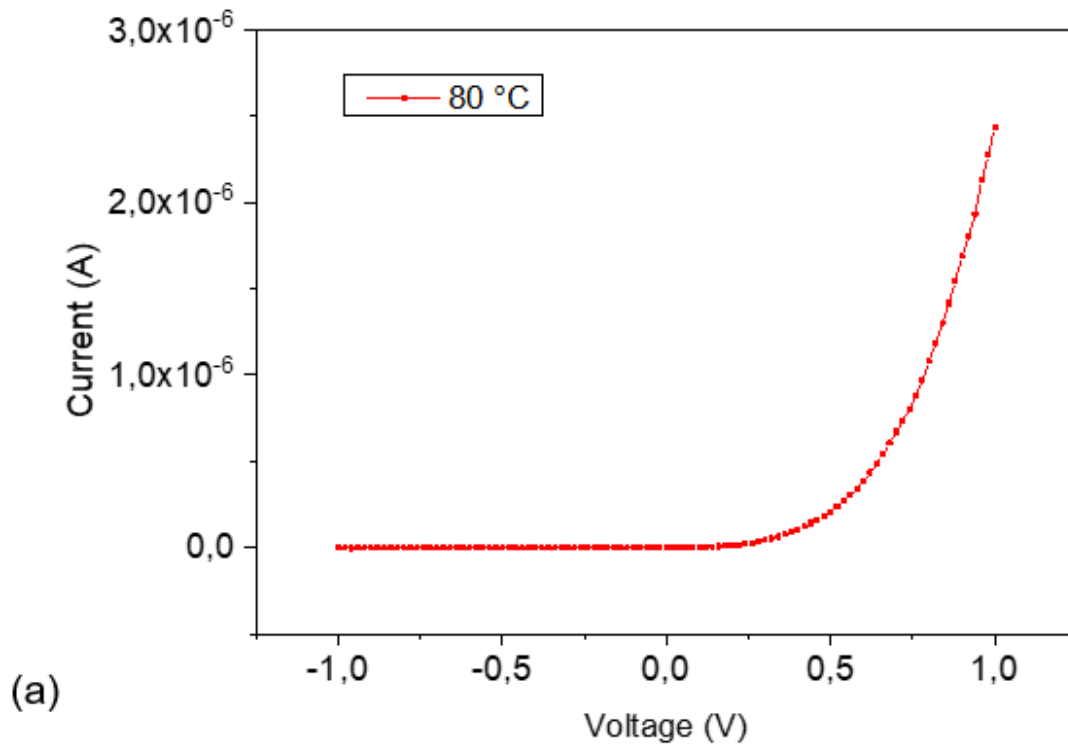


Figure 4.9. (a) (*I-V*) characteristics of a W/ZnO/Pt junction (with Pt as a bottom electrode) for a 150 nm thick ZnO thin film deposited by ALD at 80 °C. (b) Semilogarithmic (*I-V*) characteristics of W/ZnO/Pt junctions (with Pt as a bottom electrode) for ZnO thin films deposited by ALD at 100 °C, 80 °C and 60 °C.

Furthermore, a typical (I-V) curve corresponding to a W/ZnO/Pt junction (with Pt as a bottom electrode) with ALD-grown ZnO at 80 °C is displayed in log-log X-Y scale in Fig. 4.10.

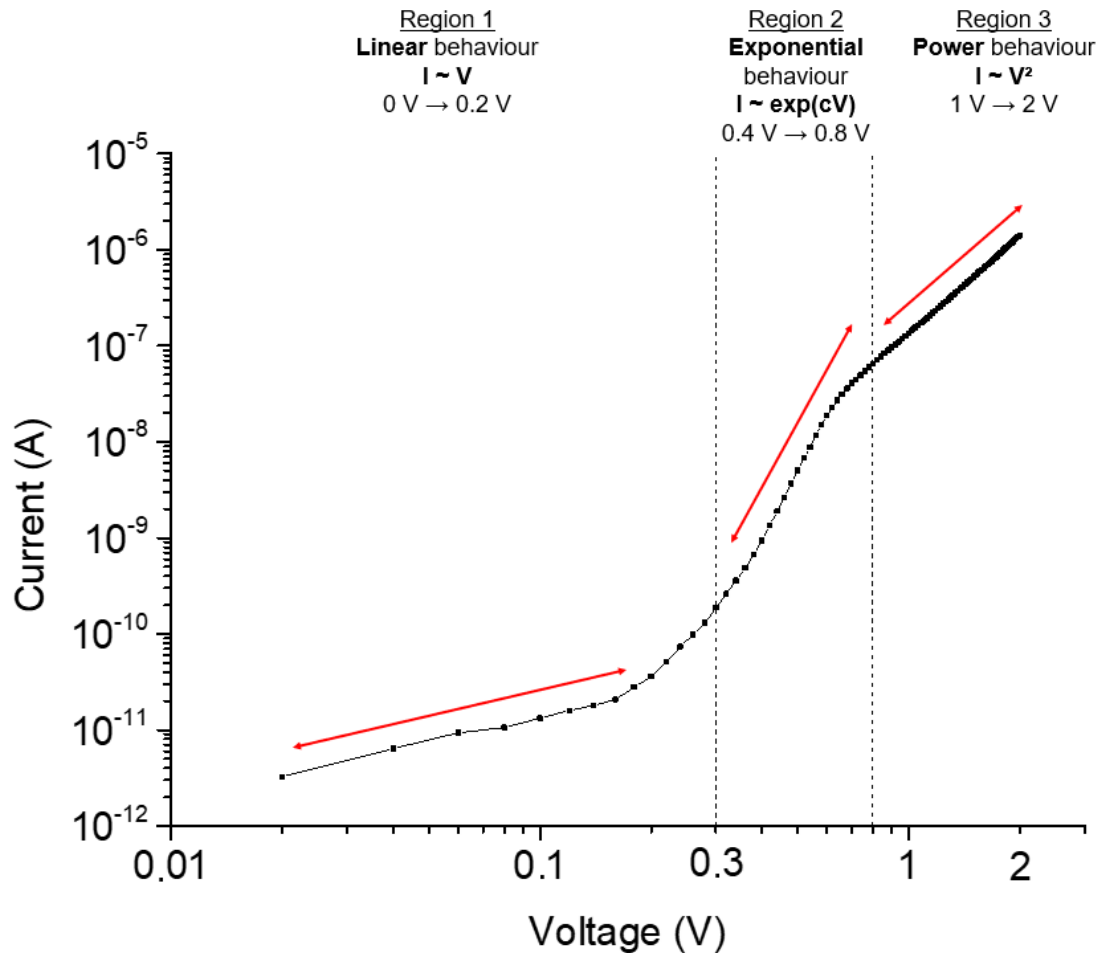


Figure 4.10. Log-log graph showing the presence of three main conduction mechanisms in the (I-V) characteristics of a W/ZnO/Pt junction (with Pt as a bottom electrode) for a 150 nm thick ZnO thin film deposited by ALD at 80 °C.

Three different regions can be identified from the log-log plot, corresponding to three distinct conduction mechanisms. Between 0 V and 0.2 V, the behaviour is linear ($I \sim V$), where the injection of electrons is reduced because of the low applied voltage. Between 0.4 V and 0.8 V, an exponential behaviour can be identified in the (I-V) characteristics ($I \sim \exp(a \cdot V)$, a being an arbitrary constant). This region accurately describes the thermionic emission model presented in equation (4.6) and validates the presence of a Schottky barrier between the locally probed ZnO thin films and the

metals. When the bias voltage is further increased from 1 V up to 2 V, the (I-V) characteristics are following a power law ($I \sim V^n$, with $n \geq 2$). A similar behaviour was reported by Hussain et al. [13]. They attributed this power dependency between the current values and the applied bias voltage to a space-charge limited current transport mechanism, controlled by the presence of traps within the band gap of the ZnO semiconducting material.

Besides, the (I-V) characteristics of the corresponding W/ZnO/Au junctions (with Au as a top electrode) were extremely similar to those obtained for the W/ZnO/Pt junctions (with Pt as a bottom electrode) for every ALD deposition temperature in study. However, interestingly, the inverted experimental configuration, consisting of the local probing of both the W/ZnO/Au junctions with Au as a bottom electrode, as well as the W/ZnO/Pt junctions with Pt as a top electrode, resulted in an ohmic behaviour, with a linear relation between the applied voltage and the measured current, for every ALD deposition temperature in study. This is further illustrated by Fig. 4.11, displaying the (I-V) characteristics for ZnO thin films deposited by ALD at 80 °C for every metal electrode configuration.

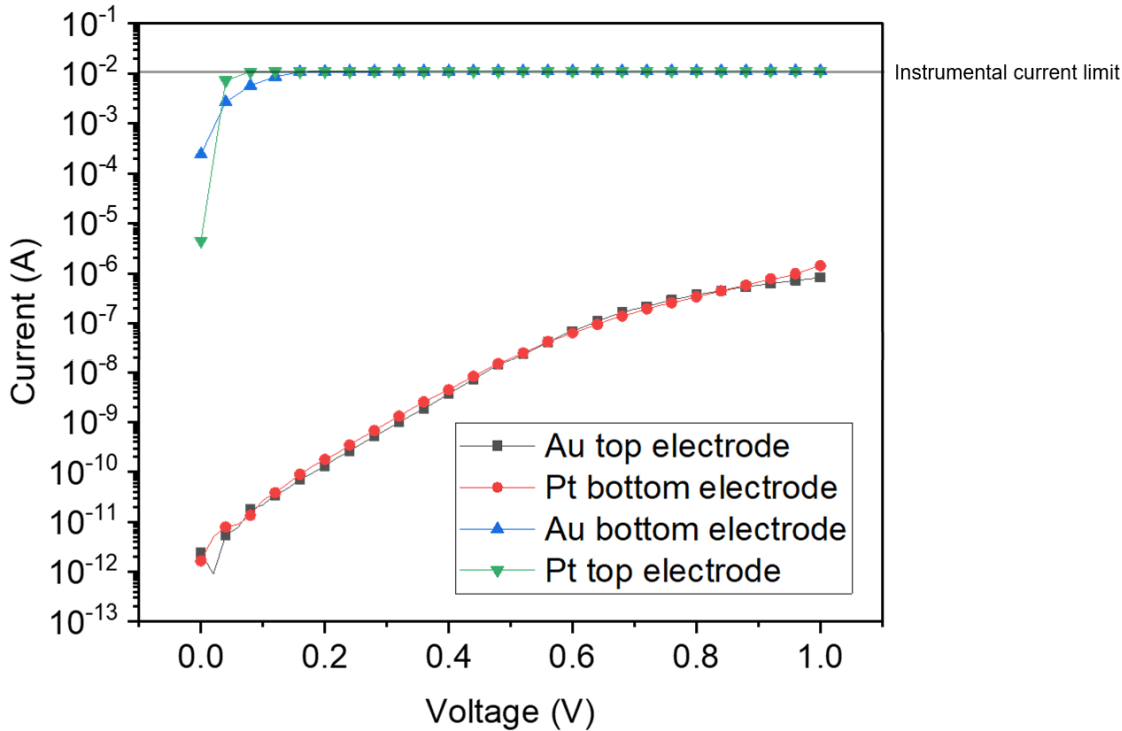


Figure 4.11. Semilogarithmic (I-V) characteristics of W/ZnO/metal junctions for ZnO thin films deposited by ALD at 80 °C, where the metal corresponds to the Pt and Au electrodes in both top and bottom configurations.

As observed from Fig. 4.11, both curves exhibiting non-linear (I-V) characteristics similar as the ones in Fig. 4.9 and Fig. 4.10 correspond to the same experimental configuration (i.e. right of Fig. 4.8(b), with Pt as a bottom electrode and Au as a top electrode), where the ZnO thin films were grown by ALD on Pt metal electrodes. However, the two other curves in Fig. 4.11 presenting linear (I-V) characteristics are exhibiting high current values, quickly reaching the instrumental current limit of 10 mA for applied bias voltage values superior to 100 mV. These linear (I-V) curves correspond to the inverted experimental configuration (i.e. left of Fig. 4.8(b), with Au as a bottom electrode and Pt as a top electrode) where the ZnO thin films were grown by ALD on Au metal electrodes. These results thus highly suggest that the underlying metal substrate might have a determinant impact on the electrical properties of the M-S junctions. A peculiar electrical behaviour corresponding to the ALD growth of ZnO thin films at 130 °C on Au metal electrodes has been reported as well by Ma et al. [14]. They observed a strong increase in the current values (from one up to 2 orders of magnitude) while comparing the (I-V) characteristics of Au/ZnO junctions with other metals (i.e. Ru and TiW). This increase in the current values was explained by the presence of a dominant diffraction peak corresponding to the (103) crystalline orientation of the ZnO thin films at $2\theta \sim 63^\circ$, leading to a strong increase of the electron concentration up to $1 \times 10^{19} \text{ cm}^{-3}$. This statement thus further confirms the strong intercorrelation between the underlying metal substrate, the ZnO crystalline orientation and the resulting M-S junction's electrical properties and deserves further studies.

Moreover, the thermal stability is a critical factor which should be accounted when integrating metal electrodes in device applications. Metals such as Au and Ag have been shown to exhibit a poor thermal stability with ZnO for temperatures higher than 330 K, leading to phenomenon of interdiffusion (i.e. for Au metal electrodes) or delamination (i.e. for Ag metal electrodes) [10,15,16]. Consequently, their use is severely compromised for microfabrication processing, which involves the use of various bakes during the different steps.

Given the above-mentioned considerations, platinum thus appears as a candidate of choice due to its high work function (i.e. typically 5.6 eV [10,17]), leading to some of the highest Schottky barrier height values reported among other metals with n-type ZnO (i.e. typically between 0.7 eV and 1 eV [10]). Moreover, platinum electrodes

present a high thermal stability, as they are generally assumed to remain structurally and chemically inert for temperatures up to 500 °C [18], thus preventing oxidation or interdiffusion from occurring [10]. Moreover, their efficiency has been proven for MEMS applications [19], which highly motivated our choice for their subsequent integration in the piezotronic sensors.

- Top-bottom electrode (TBE) configuration

Another metal electrode configuration has been investigated, where the ZnO thin film is sandwiched between a bottom and a top Pt electrode. The microfabrication process flow of the sensors on the flexible polyimide substrate corresponding to the top-bottom electrode (TBE) configuration is illustrated in Fig. 4.12. The main difference with the IDE configuration in the microfabrication processing arises after the ZnO etching, where another lithography and lift-off steps are performed to deposit the top Pt electrode above the patterned ZnO pad.

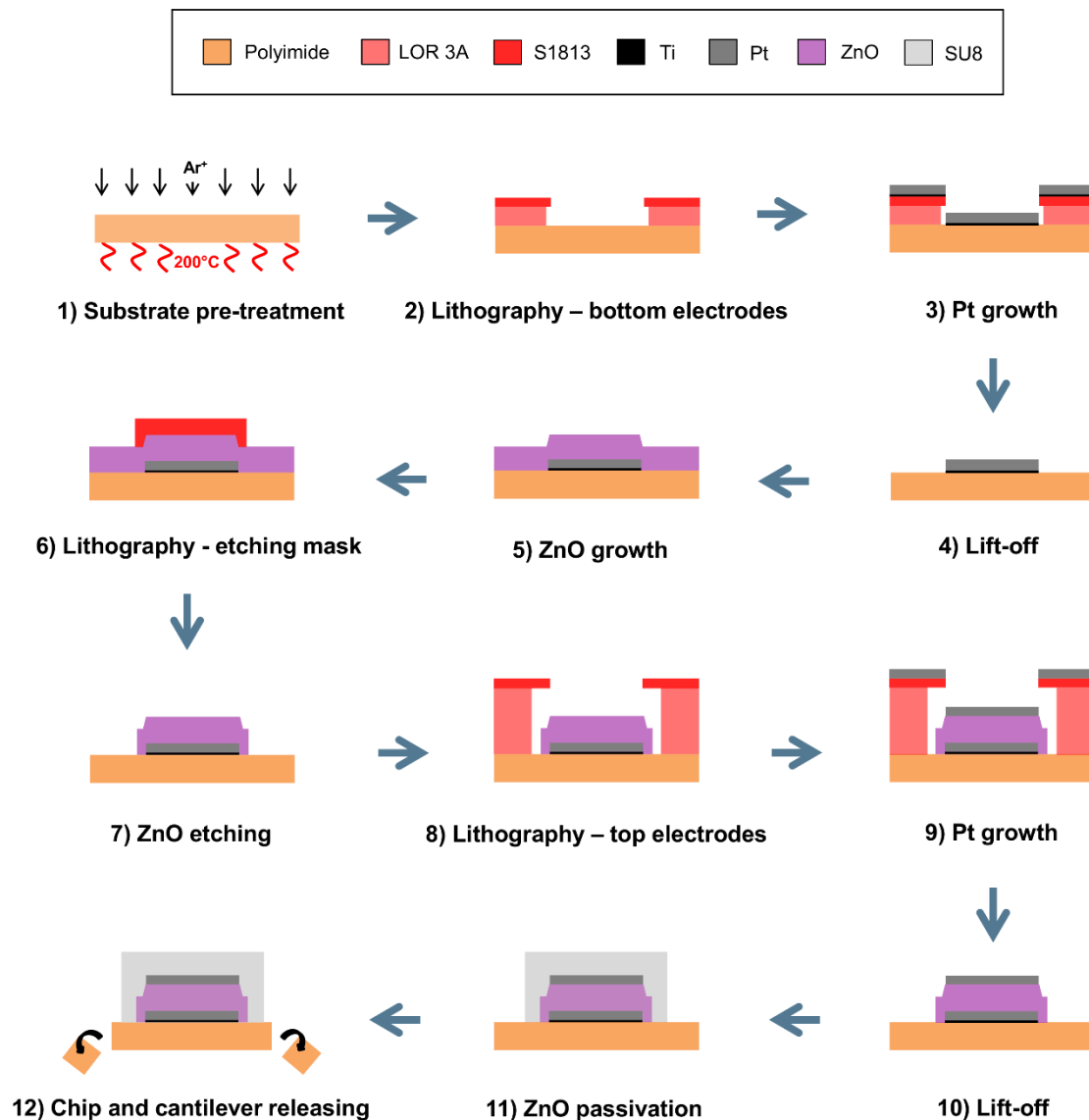


Figure 4.12. Microfabrication process flow corresponding to the top-bottom electrode configuration.

The main operating difference between the IDE and TBE configuration originates from the direction of the electric field \vec{E} , planar to the polyimide structure in the case of the IDE configuration and perpendicular to the polyimide substrate in the case of the TBE configuration, as illustrated in Fig. 4.13(a). When the polyimide cantilever is bent, a strain is exerted on the planar direction, while the piezoelectric polarization is induced perpendicular to the substrate according to the c-axis privileged orientation of ZnO perpendicular to the substrate, meaning that both configurations are actuated by the piezoelectric coefficient e_{31} . However, as the applied electric field via a bias voltage is

respectively perpendicular to the piezoelectric polarization in the IDE configuration, and parallel to the piezoelectric polarization in the TBE configuration, the distribution of the piezoelectric polarization charges should be different at their respective Pt/ZnO Schottky interfaces. As shown in Fig. 4.13(b), piezoelectric polarization charges with a similar sign are created at the Pt/ZnO interfaces in the IDE configuration, which should further result in a symmetry of the strain-actuated (I-V) characteristics. Contrarily, piezoelectric polarization charges with opposite signs are created at the Pt/ZnO interfaces in the TBE configuration, which should result in an asymmetry of the strain-actuated (I-V) characteristics.

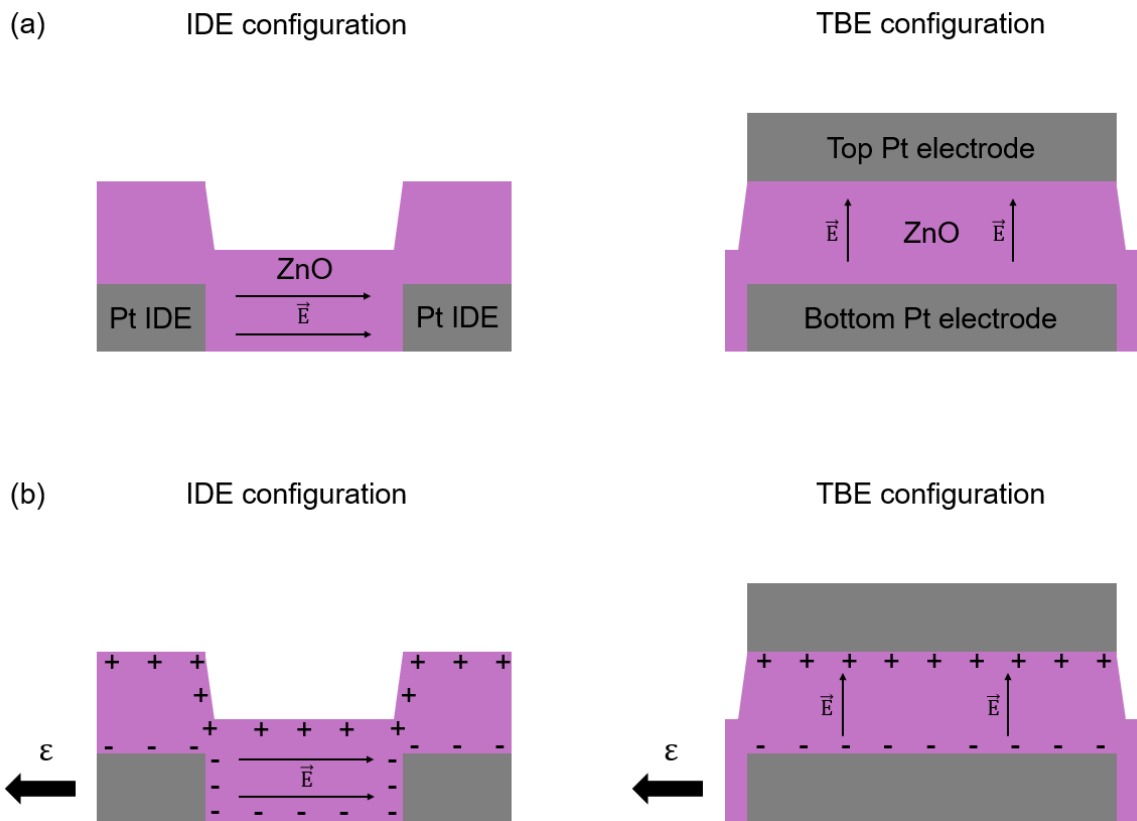


Figure 4.13. Operating difference between the IDE and TBE configuration. (a) Difference in the direction of the applied electric field for both configurations. (b) Strain-induced piezoelectric polarization charges at the Pt/ZnO Schottky interfaces for both configurations.

The sign of the piezoelectric polarization charges indicated at the Pt/ZnO interfaces in Fig. 4.13(b) is based on the convention that the c-axis direction is fixed, assuming that the positive direction goes from the cations to the anions (i.e. from Zn^{2+} to O^{2-}). Based on this assumption, the wurtzite ZnO structure is said to be Zn-polar. The polarity is a

bulk property of the ZnO wurtzite structure, which should not be mistaken with surface terminations. On the opposite, when the cation-anion bond collinear with the c-axis starts with an oxygen atom to a zinc atom, the wurtzite ZnO structure is said to be O-polar, resulting in an inversion of the sign of the piezoelectric charges at the M-S interface compared with the above-mentioned case. The polarity of a given semiconducting material can thus help to anticipate how the strain-induced electrical properties will be modulated at the M-S Schottky interfaces via the piezotronic effect. However, as pointed out recently by V. Consonni et al. [20], the polarity of ZnO nanowires used in the field of piezotronics is very often disregarded despite its importance. Within the frame of this work, knowing the polarity of the semiconducting material is a complex task as the ALD-deposited ZnO thin films are polycrystalline. Moreover, as shown in the previous chapter, the nucleation at the Pt/ZnO interfaces consists of several crystallites randomly oriented in different crystalline orientations. Consequently, the sign of the created piezoelectric polarization charges will be empirically deduced from the strain-modulated (I-V) characteristics of the piezotronic sensors.

Nonetheless, the major problem induced by the TBE configuration arises from the discontinuity of the deposited Pt top electrode, linked with the directionality of the Pt deposition by EBME, as well as by the presence of a step height (~ 500 nm) between the ZnO pad and the polyimide substrate, as shown in Fig. 4.14. The presence of this step height induced a breach of the electrical continuity. Depositions of the top Pt electrode with an oblique angle by EBME and sputtering were tentatively performed to improve the step coverage, but still resulted in an electrical discontinuity, which prevented us from further testing the electrical and transducing properties of this sensor configuration.

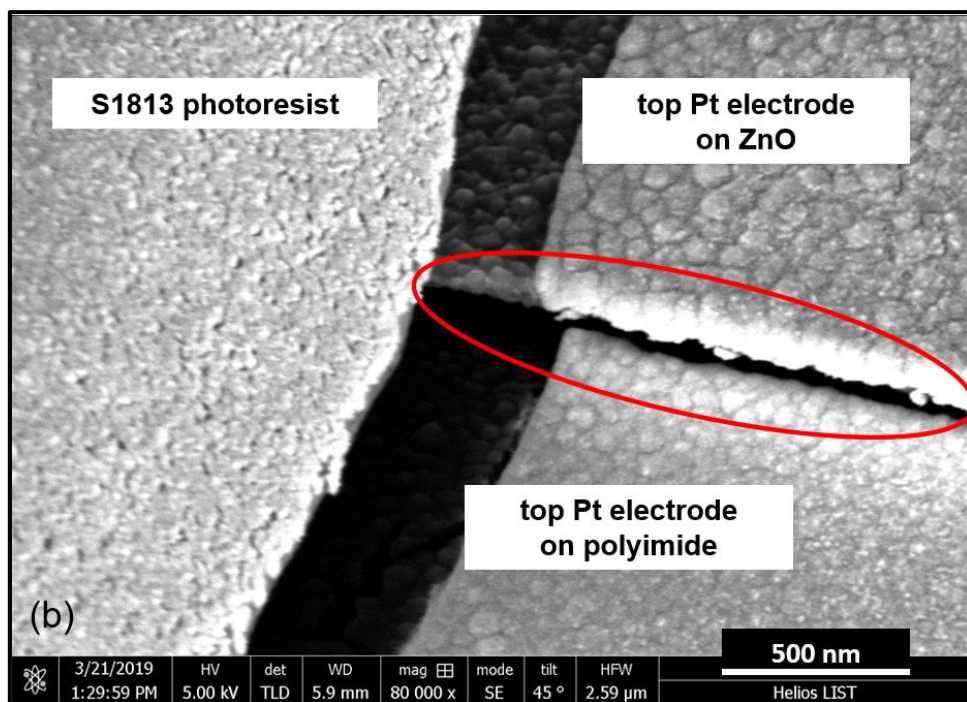
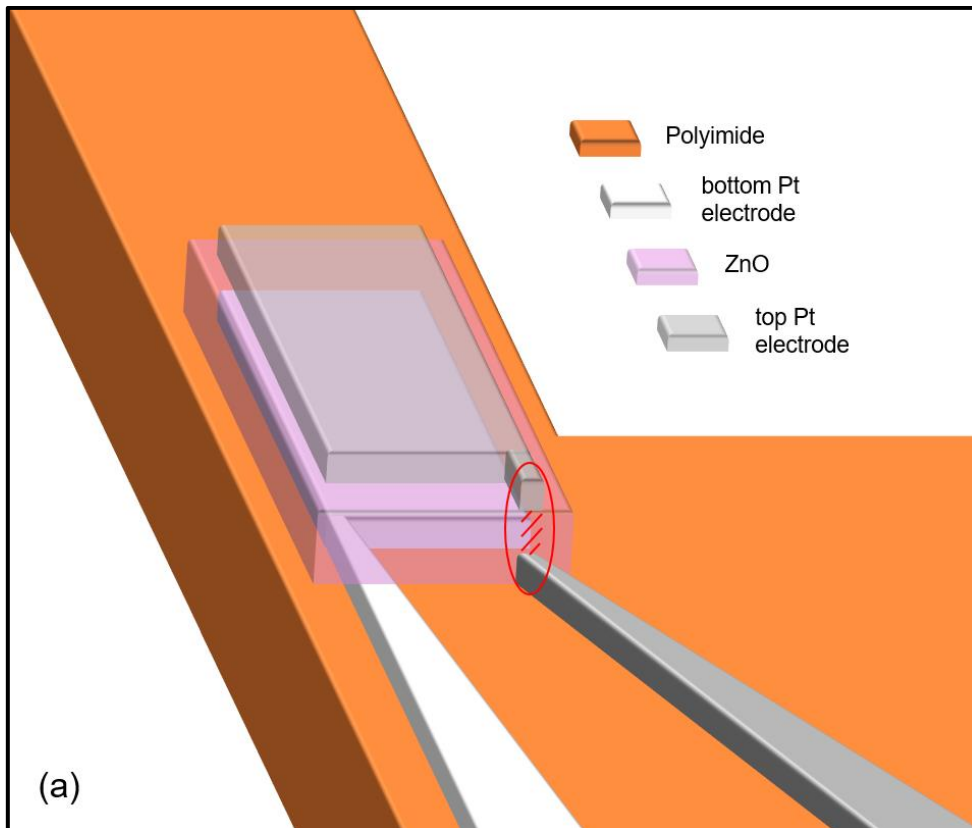


Figure 4.14. (a) Sketch of top-bottom electrode configuration at the sensitive area. Not to scale. (b) SEM picture showing the discontinuity of the top platinum electrode between the ZnO pad and the polyimide substrate. The S1813 photoresist layer is used within the lift-off process.

4.2. Electrical characteristics of the Pt/ZnO/Pt Schottky junctions

4.2.1. Identification and development of the conduction mechanism

Fundamentals of metal-semiconductor contacts were introduced and developed by S.M. Sze and Kwok K. Ng [11] and E.H. Rhoderick and R.H. Williams [21]. The description of the conduction mechanisms occurring in M-S-M structures is a complex function depending on several parameters. Different conduction mechanisms can occur at the M-S Schottky junctions depending on the carrier concentration of the semiconducting material and on the temperature. Additionally, phenomena such as image-force lowering as well as the presence of interface trap states can have a major influence in the electrical properties at the M-S interfaces. As the M-S-M structures consist in two back-to-back Schottky diodes, the classical methods for the extraction of Schottky diode parameters from forward biased M-S junctions cannot be applied [22,23]. M-S-M structures involving Schottky interfaces are now ubiquitous in MEMS and CMOS applications. Several works thus focused on the rationalization of the electrical properties in back-to-back Schottky diodes [24–31], providing various methods for the extraction of the characteristic material's parameters influencing the conduction mechanism. However, some of these methods remain theoretical or can only be applied in specific regions of the (I-V) characteristics. Moreover, the impact of the series resistance and the interface trap states are often neglected in these models. Most importantly, not enough attention has been given on some crucial material's parameters such as the carrier concentration, on the validity of the extracted parameters, as well as on the interplay between the variation of the material's parameters and the resulting electrical properties. Furthermore, it is necessary to precisely define the conduction mechanism to better understand how the strain-induced piezoelectric polarization charges are modulating the (I-V) characteristics of the Pt/ZnO/Pt Schottky junctions integrated in the piezotronic sensors. Conduction mechanisms in the field of piezotronics are commonly described by various models, including the thermionic emission model [32], the thermionic emission-diffusion model [33,34], or the thermionic-field emission model [35,36]. However, most of these works do not provide any justification regarding the choice of the emission model and are not

meticulous in the extraction and the validation of the material's parameters. This section thus aims at precisely characterizing the electrical properties of the Pt/ZnO/Pt Schottky junctions integrated in the piezotronic sensors, through a rigorous identification and description of the conduction model. The M-S-M structures considered in this section consist of interdigitated Pt metal electrodes contacted with ZnO thin films deposited at 80 °C and 60 °C.

As detailed in the section 4.1.1, the platinum metal electrodes are organized as two interdigitated sets, leading to the creation of several metal-semiconductor-metal (M-S-M) Schottky diodes within the area defined by the ZnO pad. The equivalent circuit model consists of two back-to-back Schottky diodes corresponding to the Pt/ZnO interfaces, together with the series resistance of the ZnO thin film, as illustrated in Fig. 4.15.

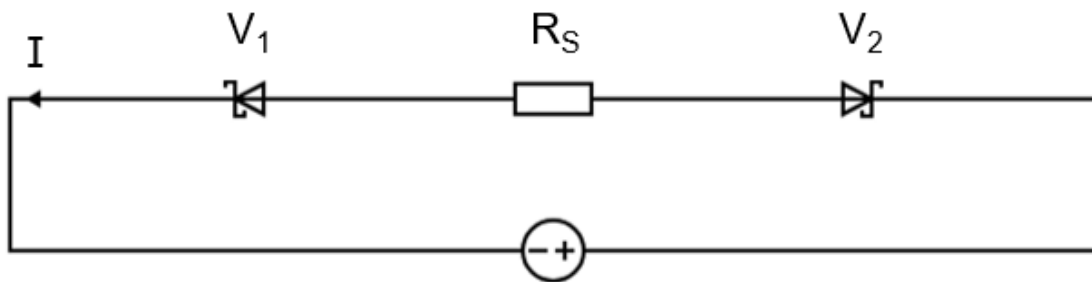


Figure 4.15. Equivalent circuit model of the Pt/ZnO/Pt Schottky junctions.

Where the total current I of the device corresponds to the sum of each individual back-to-back Schottky diode current, as presented in equation (4.5). V_1 and V_2 are the voltage drops occurring at the reverse and forward biased Schottky diodes, respectively, while R_S represents the series resistance in the bulk of the ZnO thin film. When a bias voltage is applied, one of the Schottky diode junctions will necessarily be reversely biased while the other will be forward biased, depending on the sign of the bias voltage. In the following analysis, the reverse and forward biased Schottky junctions together with their respective parameters will be designated as 1 and 2, respectively. By applying Kirchhoff voltage law, in a series circuit, the voltage is the

sum of the voltage drops of each individual component, which yields the following equation when applied to the equivalent circuit model:

$$V = V_1 + V_{\text{ZnO}} + V_2 \quad (4.7)$$

Where V is the applied bias voltage and V_{ZnO} is the voltage drop occurring in the bulk of the ZnO thin film, which can be further expressed as the product of the total current I of the device and the series resistance R_S , as:

$$V = V_1 + I \cdot R_S + V_2 \quad (4.8)$$

Moreover, in a series circuit, the current flowing through each component is equal, in such a way that:

$$I = I_1 = I_{\text{ZnO}} = I_2 \quad (4.9)$$

Where I_1 and I_2 are the current flowing through the reverse and forward biased Schottky diodes, respectively, and I_{ZnO} is the current flowing through the bulk of the ZnO thin film.

The schematic energy band diagram of the Pt/ZnO/Pt Schottky junctions at thermal equilibrium is illustrated in Fig. 4.16.

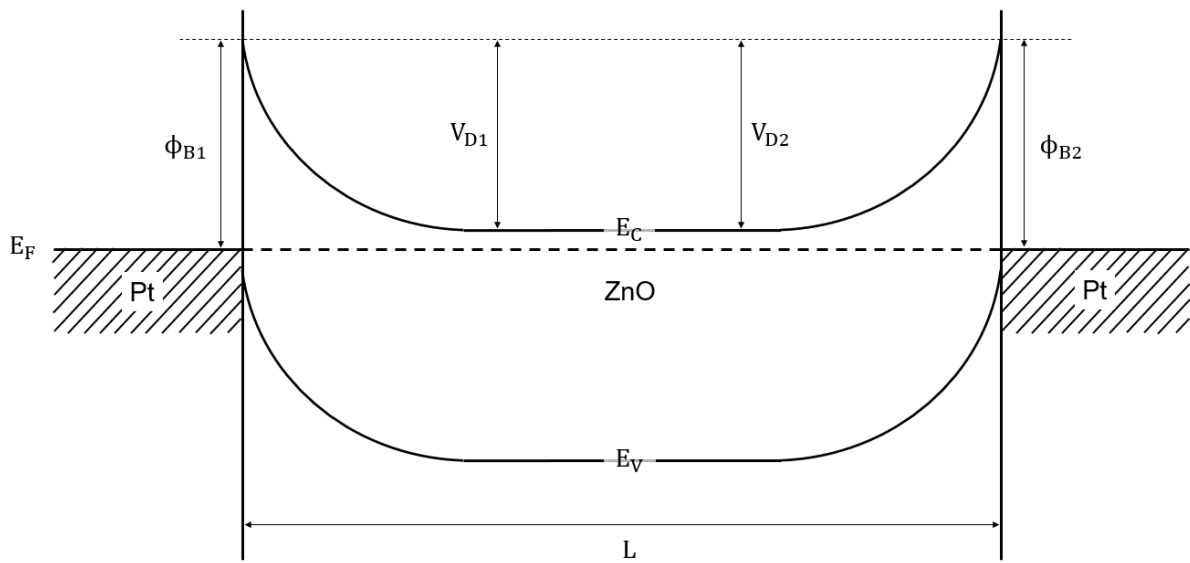


Figure 4.16. Schematic energy band diagram of the Pt/ZnO/Pt structure at thermal equilibrium.

Where E_F , E_C and E_V are the Fermi level of the metal, conduction band of the semiconductor and valence band of the semiconductor, respectively. V_{D1} and V_{D2} are the built-in voltages at contacts 1 and 2, respectively, defined as the distance between the conduction band and the Schottky barrier height at thermal equilibrium. ϕ_{B1} and ϕ_{B2} are the Schottky barrier heights at contacts 1 and 2, respectively. L is the distance separating the two metal electrodes, varying between 5 μm and 30 μm as a function of the IDE design in use (see Table 4.1).

The free carriers transport in the Pt/ZnO/Pt Schottky junctions is dominated by electrons due to the intrinsic n-type nature of the ZnO thin film. When a bias voltage is applied, its total value V is thus shared between the reverse and forward biased Schottky junctions (V_1 and V_2), as well as in the bulk of the ZnO thin film (V_{ZnO}). As the current continuity requirement shown in equation (4.9) states that the electron current across both Schottky barriers and in the bulk of the ZnO thin film must be equal, most of the total bias voltage will thus be injected in the reverse biased Schottky junction. The conduction mechanism will thus be dictated by the reverse biased Schottky junction. However, a low voltage drop is still necessary to bias the forward biased Schottky junction, as well as to take into account in the bulk of the ZnO. Nonetheless, as the reverse biased Schottky junction is characterized by low current values, a high series resistance is required for the resulting voltage drop V_{ZnO} to be meaningful

compared to the applied bias voltage. The series resistance and its resulting voltage drop will thus be assumed to be negligible in the following analysis. Their impact on the electrical properties of the Pt/ZnO/Pt Schottky junctions will be assessed within the following section.

The schematic energy band diagram of the Pt/ZnO/Pt structure under an arbitrary bias voltage is illustrated in Fig. 4.17.

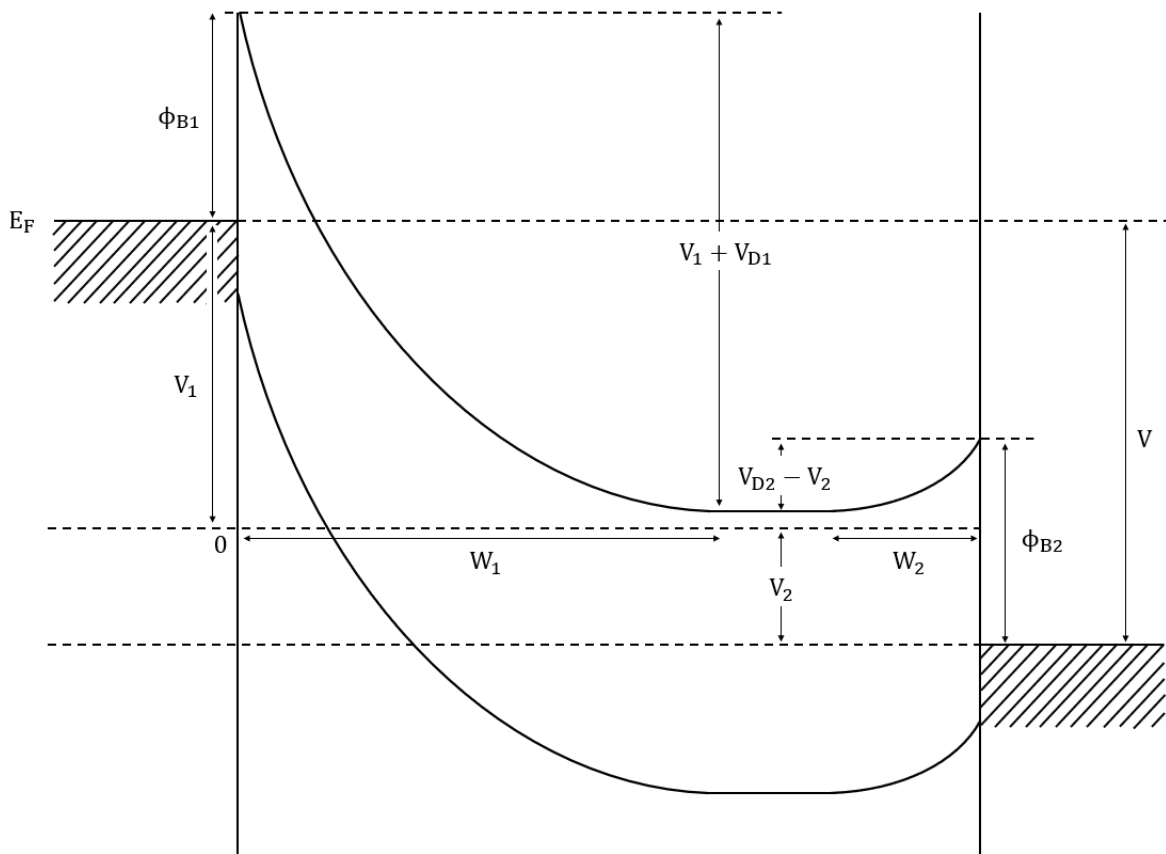


Figure 4.17. Schematic energy band diagram of the Pt/ZnO/Pt structure under bias, where the Schottky barrier denoted as 1 is reverse biased while the Schottky barrier denoted as 2 is forward biased. Adapted from [24].

Where W_1 and W_2 are the depletion widths corresponding to the reverse and forward biased Schottky diodes, respectively, while the other parameters have the same meaning as before. As the voltage drop at the reverse biased Schottky junction is much superior to the voltage drop at the forward biased Schottky junction, its corresponding depletion width W_1 is also much superior than W_2 . These depletion widths are expressed as [24]:

$$W_1 = \sqrt{\left[\frac{2 \cdot \epsilon_S}{q \cdot N_D} \cdot (V_1 + V_{D1}) \right]} \quad (4.10)$$

$$W_2 = \sqrt{\left[\frac{2 \cdot \epsilon_S}{q \cdot N_D} \cdot (V_{D2} - V_2) \right]} \quad (4.11)$$

Where q is the electron charge, ϵ_S is the permittivity of the ZnO thin film and N_D is the electron concentration of the ZnO thin film.

As the conduction mechanism is dictated by the contact 1, we will first focus on the description of the electrical characteristics through the reverse biased Schottky junction. Within this scope, three main conduction mechanisms can typically occur at this interface according to S. M. Sze [11], as illustrated in Fig. 4.18.

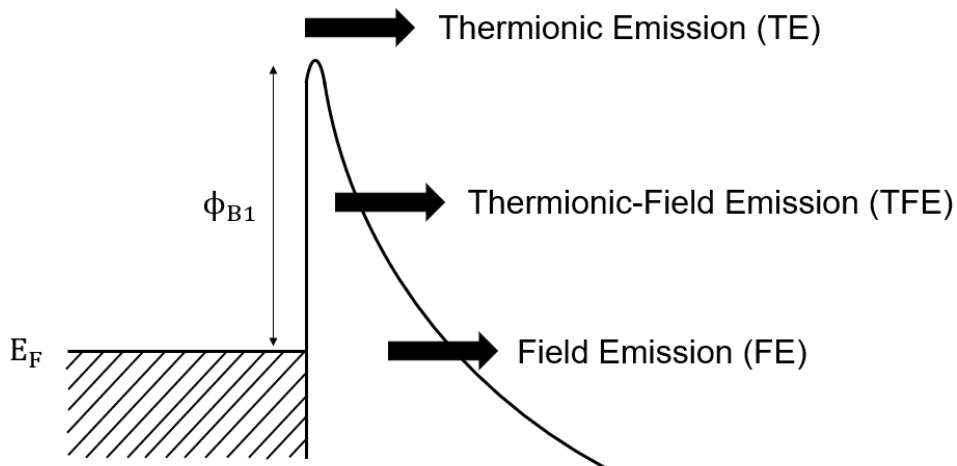


Figure 4.18. Illustration of the three potential conduction mechanisms occurring in a reverse biased Schottky junction. Adapted from S. M. Sze [11].

These conduction mechanisms refer to the thermionic emission (TE) of electrons over the Schottky barrier, field emission (FE) through the Schottky barrier at an energy close to the Fermi level and thermionic-field emission (TFE), occurring at an energy between the thermionic and field emission. More precisely, FE corresponds to a pure tunnelling process, while TFE is associated to tunnelling of thermally excited electrons seeing a thinner barrier when compared to FE [11]. The relative contribution of these conduction

mechanisms on the total current flowing through the reverse biased Schottky junction depends mainly on the electron concentration and on the temperature. In order to assess their respective impact, the thermal energy $k_B T$, characteristic of the thermionic emission, is usually compared to the energy criterion E_{00} , characteristic of field emission, in Joules unit. E_{00} , based on a triangular Schottky barrier height model also proposed by Yu Cao et al. [37] and approximating very well the barrier profile, is defined by S.M. Sze and K. K. Ng as [11]:

$$E_{00} \equiv \frac{q \cdot \hbar}{2} \cdot \sqrt{\frac{N_D}{m^* \cdot \epsilon_s}} \quad (4.12)$$

Where \hbar is the reduced Plank constant and m^* is the effective electron mass for ZnO.

A quantitative comparison of $k_B T$ with E_{00} applied to ZnO parameters at a given temperature thus allows to determine which conduction mechanism will dominate depending on the electron concentration value. The evolution of E_{00} as a function of the electron concentration N_D at 300 K is shown in the Fig. 4.19. The values of E_{00} are compared with $k_B T$, indicated by a straight horizontal line in the log-log representation.

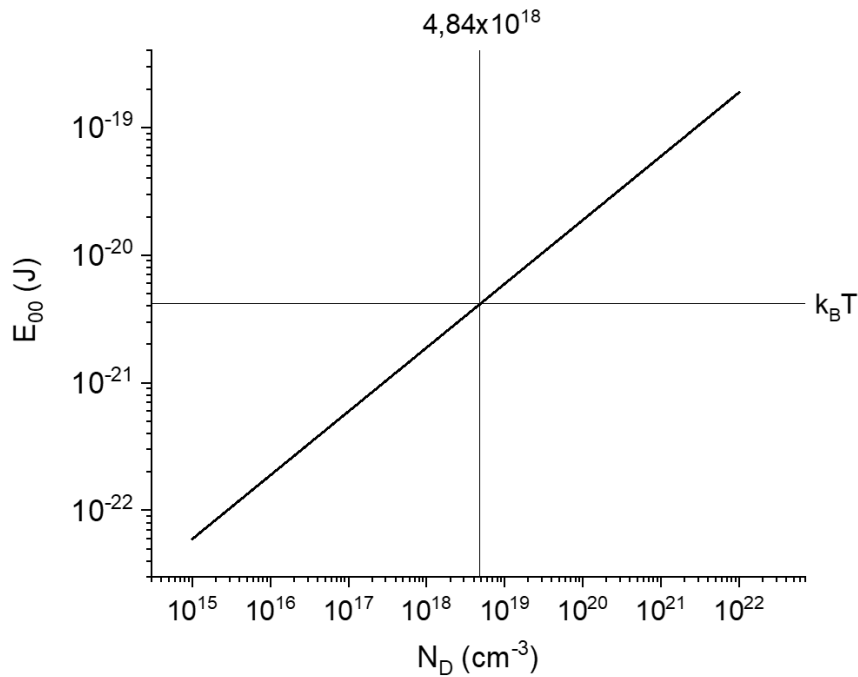


Figure 4.19. Evolution of E_{00} as a function of the electron concentration N_D at a temperature of 300 K in log-log scale. The value of the thermal energy $k_B T$ is indicated by a straight horizontal line. The electron concentration corresponding to $k_B T = E_{00}$ is indicated by a straight vertical line.

For $k_B \cdot T = E_{00}$, the value of the electron concentration can be determined as:

$$N_D \equiv \left(\frac{2 \cdot k \cdot T}{q \cdot \hbar} \right)^2 \cdot m^* \cdot \epsilon_s \quad (4.13)$$

Which yields numerically $N_D \approx 4,84 \times 10^{18} \text{ cm}^{-3}$, this value thus corresponding to the threshold electron concentration value applied to our configuration at 300 K. Consequently, when the electron concentration is inferior to $4,84 \times 10^{18} \text{ cm}^{-3}$, the thermionic emission (TE) of electrons over the Schottky barrier will dominate as a conduction mechanism. Also, when N_D is superior to $4,84 \times 10^{18} \text{ cm}^{-3}$, field emission (FE) with electrons tunnelling through the Schottky barrier will dominate. Finally, when N_D is close to the value of $4,84 \times 10^{18} \text{ cm}^{-3}$, thermionic-field emission (TFE) will be the main conduction mechanism, consisting in a combination of TE and FE.

In the previous chapter, we estimated the electron concentration at a value of $8 \times 10^{16} \text{ cm}^{-3}$ for an ALD deposition temperature of 100 °C. Moreover, electron concentration values reported in the literature for deposition temperatures below 100 °C typically extend between 10^{15} cm^{-3} and 10^{17} cm^{-3} . As the ZnO thin films integrated in the piezotronic sensors were deposited at 80 °C and 60 °C, thermionic emission is thus very likely to be the dominant conduction mechanism within our system.

According to the thermionic emission theory, the reverse current of an ideal Schottky diode at a given temperature should saturate at a constant value, given by the so-called saturation current, as [21]:

$$I_1 = A \cdot A^* \cdot T^2 \cdot \exp\left(-\frac{q \cdot \phi_{B1}}{k_B \cdot T}\right) \quad (4.14)$$

However, as mentioned previously, there are several causes of deviation from this ideal behaviour, leading to an increase of the leakage current through the reverse biased Schottky junction. The increase in the leakage current can be linked with the Schottky barrier dependence on the applied electric field, leading to a lowering of the Schottky barrier height. Within this scope, image-force lowering is commonly attributed to the Schottky barrier lowering to explain the lack of saturation. Image-force lowering

originates from the presence of an image charge (i.e. a positive charge) induced on the metal surface when an electron is located at a distance x from the metal. This image charge is generating an attractive force toward the metal, inducing the generation of a potential energy along the distance x when an external electric field is applied, referred as the image potential energy [11]. The impact of the image-force lowering on the Schottky barrier is illustrated in Fig. 4.20.

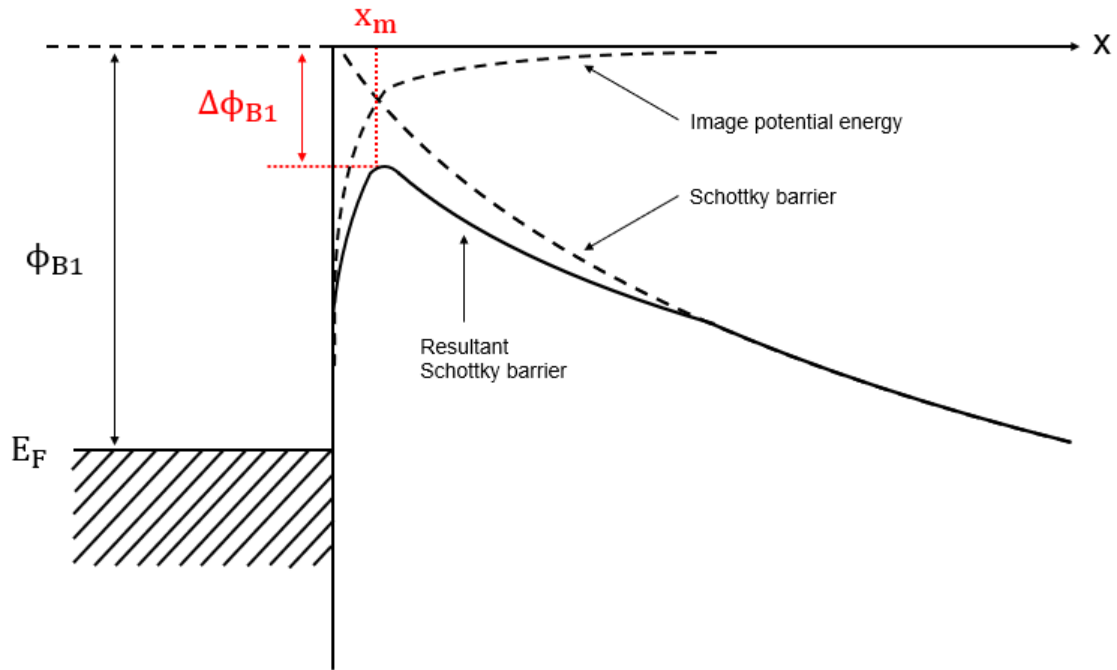


Figure 4.20. Energy band diagram illustrating the impact of the image-force lowering on the Schottky barrier. The horizontal axis corresponds to the distance x . Adapted from [21].

The resulting Schottky barrier height lowering $\Delta\phi_{B1}$ is calculated at the distance x_m , where the maximum electric field E_m occurs.

$\Delta\phi_{B1}$ is expressed as a function of the maximum electric field at the reverse biased Schottky junction E_{m1} , as [11]:

$$\Delta\phi_{B1} = \sqrt{\frac{q \cdot E_{m1}}{4 \cdot \pi \cdot \epsilon_s}} \quad (4.15)$$

Where the maximum electric field E_{m1} is defined by [21]:

$$E_{m1} = \sqrt{\frac{2 \cdot q \cdot N_D}{\epsilon_s} \cdot (V_1 + V_{D1})} \quad (4.16)$$

By combining equations (4.15) and (4.16), $\Delta\phi_{B1}$ can thus be further expressed as:

$$\Delta\phi_{B1} = \left[\frac{q^3 \cdot N_D}{8 \cdot \pi^2 \cdot \epsilon_s^3} \cdot (V_1 + V_{D1}) \right]^{1/4} \quad (4.17)$$

As observed from equation (4.17), the Schottky barrier lowering presents a dependence on both the bias voltage and the electron concentration. Consequently, the Schottky barrier height lowering $\Delta\phi_{B1}$ will be increased with increasing applied bias voltage. Injecting equation (4.17) into equation (4.14) with $\phi_{B1} - \Delta\phi_{B1}$ instead of ϕ_{B1} thus yields:

$$I_1 = A \cdot A^* \cdot T^2 \cdot \exp\left(-\frac{q \cdot \phi_{B1}}{k_B \cdot T}\right) \cdot \exp\left(\frac{q \cdot \Delta\phi_{B1}}{k_B \cdot T}\right) \quad (4.18)$$

Nonetheless, we observed empirically that the simulated (I-V) characteristics with equation (4.18), using various parameters values for ϕ_{B1} and N_D , led to current values way inferior to the experimentally obtained (I-V) characteristics of the piezotronic sensors. Image-force lowering alone thus cannot explain the lack of saturation at the reverse biased Pt/ZnO Schottky junction within our devices.

Consequently, we considered another cause of increased leakage current through the reverse biased Schottky junction, linked with interface effects. More precisely, the presence of either an interfacial layer or interface trap states at the Pt/ZnO Schottky junction leads to a dependence of the Schottky barrier height on the electric field, which thus decreases with increasing applied bias voltage [21]. This effect can be formalised as an empirical field dependence, leading to an additional reduction in the Schottky barrier height $\Delta\phi_{B1}'$, expressed as [38]:

$$\Delta\phi_{B1}' \approx \alpha \cdot E_{m1} \quad (4.19)$$

This phenomenon is often referred as the static lowering, where α , the intrinsic barrier lowering coefficient, is a parameter determined empirically, in units of meters [21,38]. Its value is typically reported within the range of 1 nm up to 5 nm [21]. The physical interpretation of the static lowering applied to our system will be discussed within the next section. The image-force correction $\Delta\phi_{B1}$ on the Schottky barrier height is proportional to $E_{m1}^{1/2}$, while the static lowering correction $\Delta\phi_{B1}'$ is linearly proportional to E_{m1} . Consequently, the barrier lowering generated by the phenomenon of static lowering is considerably greater than the image-force lowering. By adding the static lowering contribution to the Schottky barrier height, the conduction mechanism results in the following equation:

$$I_1 = A \cdot A^* \cdot T^2 \cdot \exp\left(-\frac{q \cdot \phi_{B1}}{k_B \cdot T}\right) \cdot \exp\left(\frac{q \cdot (\Delta\phi_{B1} + \Delta\phi_{B1}')}{k_B \cdot T}\right) \quad (4.20)$$

Which is equivalent to:

$$I_1 = A \cdot A^* \cdot T^2 \cdot \exp\left(-\frac{q \cdot \phi_{B1}}{k_B \cdot T}\right) \cdot \exp\left(\frac{q \cdot \left(\sqrt{\frac{q \cdot E_{m1}}{4 \cdot \pi \cdot \epsilon_s}} + \alpha_1 \cdot E_{m1}\right)}{k_B \cdot T}\right) \quad (4.21)$$

Finally, a correction for low applied bias voltage shall be implemented in the conduction mechanism of the reverse biased Schottky junction, corresponding to $1 - \exp\left(-\frac{q \cdot V_1}{k_B \cdot T}\right)$, ensuring that the current is zero when no bias voltage is applied [11,38]. The equation describing the conduction mechanism through the reverse biased Schottky junction finally results in:

$$I_1 = A \cdot A^* \cdot T^2 \cdot \exp\left(-\frac{q \cdot \phi_{B1}}{k_B \cdot T}\right) \cdot \exp\left(\frac{q \cdot (\Delta\phi_{B1} + \Delta\phi_{B1}')}{k_B \cdot T}\right) \cdot \left[1 - \exp\left(-\frac{q \cdot V_1}{k_B \cdot T}\right)\right] \quad (4.22)$$

The main difference in the conduction mechanism of the forward biased Schottky junction is obviously arising from the exponential dependence of its current I_2 on the voltage drop V_2 . Additionally, both the effects of the image-force lowering and the static lowering are occurring as well on the forward biased Schottky junction and should be

taken into account. By analogy, the conduction mechanism through the forwardly biased diode junction, whose parameters are denoted as 2, is described by:

$$I_2 = A \cdot A^* \cdot T^2 \cdot \exp\left(-\frac{q \cdot \phi_{B2}}{k_B \cdot T}\right) \cdot \exp\left(\frac{q \cdot (\Delta\phi_{B2} + \Delta\phi_{B2}')}{k_B \cdot T}\right) \cdot \left[\exp\left(\frac{q \cdot V_2}{k_B \cdot T}\right) - 1\right] \quad (4.23)$$

Where:

$$E_{m2} = \sqrt{\frac{2 \cdot q \cdot N_D}{\epsilon_s} \cdot (V_{D2} - V_2)} \quad (4.24)$$

The image-force lowering and the static lowering are adapted from equations (4.15) and (4.19), as:

$$\Delta\phi_{B2} = \sqrt{\frac{q \cdot E_{m2}}{4 \cdot \pi \cdot \epsilon_s}}$$

And:

$$\Delta\phi_{B2}' \approx \alpha \cdot E_{m2}$$

The Pt/ZnO/Pt contacts consist of a symmetrical structure in our IDE configuration, where both Schottky junctions are contacted with Pt metal electrodes and were processed following similar deposition and microfabrication steps. Consequently, the Schottky barrier heights of both contacts as well as their intrinsic barrier lowering coefficients are assumed to be equal ($\phi_{B1} = \phi_{B2} = \phi_B$ and $\alpha_1 = \alpha_2 = \alpha$). Moreover, the built-in voltage at both contacts is assumed to be equal as well ($V_{D1} = V_{D2} = V_D$). As the conduction mechanism is dictated by the reverse biased Schottky junction, the experimental (I-V) should be fitted using equation (4.22), using the voltage drop value V_1 . As only the total applied bias voltage V is known as an input parameter, this also implies the determination of the voltage drop V_2 at the forward biased junction. Furthermore, several parameters used in the described conduction mechanisms in equations (4.22) and (4.23) remain unknown, i.e. the Schottky contact area A , the Schottky barrier height ϕ_B , the electron concentration N_D , the built-in voltage V_D , as

well as the intrinsic barrier lowering coefficient α . Due to the multiplicity of these variables, no analytical solution can be extracted from the developed conduction mechanisms, a numerical solution thus has to be implemented to fit the experimental (I-V) characteristics. The development of this numerical solution is detailed in the following section.

4.2.2. Determination of experimental material parameters and fitting of the experimental (I-V) curves

In order to fit the experimental (I-V) characteristics, a numerical solution was implemented by a non-linear curve fitting, based on an Orthogonal Distance Regression iteration algorithm via the software Origin [39]. Nonetheless, it is extremely advisable to minimize the number of unknown variables and parameters in the system of equations, in order to facilitate and improve the resulting fitting of the curves. Several parameters were thus estimated or determined experimentally by various methods, detailed within this section.

4.2.2.1. Estimation of the Schottky contact area

The Schottky contact area A is defined as the cross-sectional surface corresponding to the area in contact between the metal and the semiconductor, i.e. the Pt IDE and the ZnO thin film. A precise estimation of this value is thus important for the fitting as it is linearly proportional to the resulting current. However, as the interdigitated Pt electrodes are defined within both the length and the width of the polyimide cantilever, a simple longitudinal cross-section is not sufficient to accurately represent the Schottky contact area of the Pt/ZnO/Pt structures. Moreover, the distribution of the electric field should be considered at the relevant Pt/ZnO interfaces for a better estimation of the Schottky contact area. Within this scope, numerical simulations were performed using the “current flow” module of FEMM software [40]. Two different 2D models were implemented, with a longitudinal cross-section and a top view of the Pt/ZnO interfaces, while using the geometrical parameters from the experimental device with the IDE structure corresponding to the design denoted as “2” (see Table 4.1). The

computations were performed by using the electrical conductivity of the ZnO thin films deposited at 80 °C (taken as the inverse of the resistivity, i.e. $0.392 \text{ S}\cdot\text{m}^{-1}$) with a relative electrical permittivity of 8.59 [41]. Considering the Pt metal electrodes, we used an electrical conductivity of $9.43 \times 10^6 \text{ S}\cdot\text{m}^{-1}$. In both models, a Pt electrode was set to a fixed bias voltage value of 1 V while the other Pt electrode was grounded. The computational domains and the resulting distribution of the electric field strength in the ZnO layer corresponding to the cross-sectional and top view models are depicted in Fig. 4.21 and Fig. 4.22, respectively.

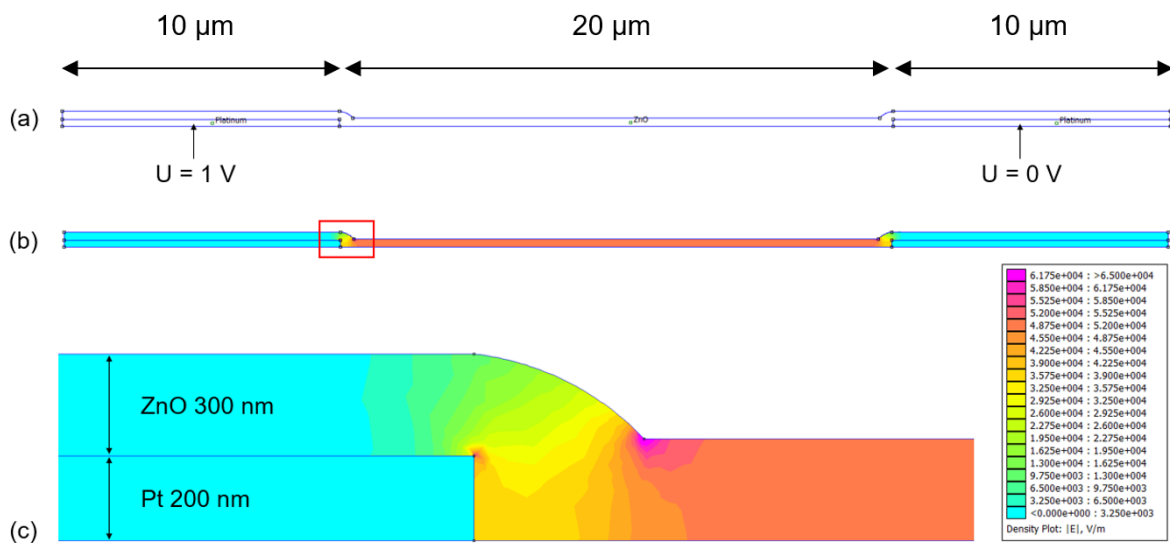


Figure 4.21. (a) 2D Computational domain of the structure's longitudinal cross-section. (b) Resulting distribution of the electric field strength in the ZnO layer. The outlined red box corresponds to the area represented in the enclosed view below. (c) Enclosed view showing the distribution of the electric field strength in the ZnO layer at a Pt/ZnO interface.

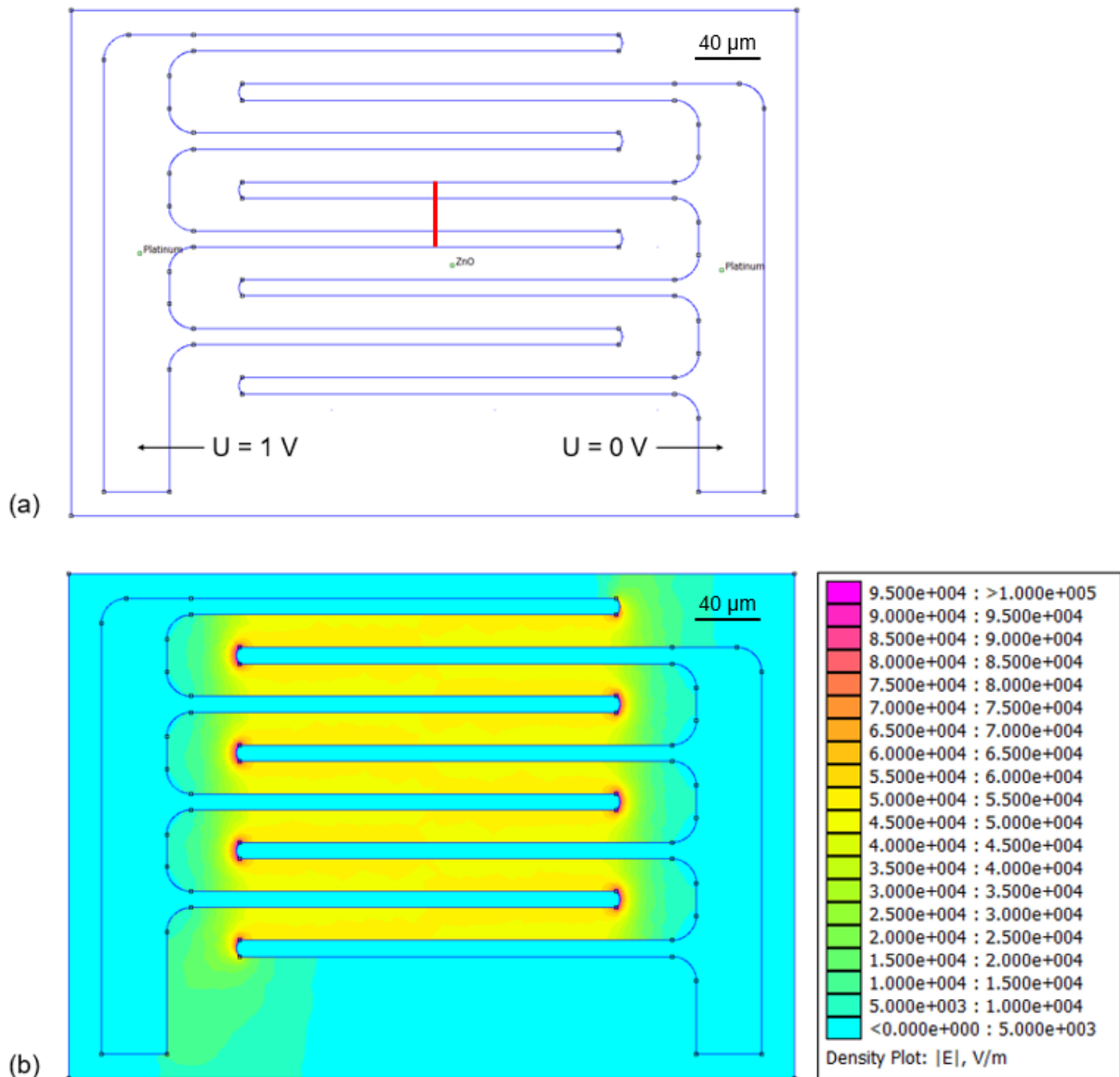


Figure 4.22. (a) 2D Computational domain of the structure's top view. The red line corresponds to the cross-sectional area represented in Fig. 4.21. (b) Resulting distribution of the electric field strength in the ZnO layer.

On Fig. 4.21, it can be observed from the electric field strength distribution that the Schottky contact area is not only extending on the side of the Pt electrode, but also on its top on an approximate length of ~ 200 nm. Moreover, from Fig. 4.22, one can notice that the Schottky contact area is extending over the whole length of the interdigitated Pt fingers l_{if} (~ 280 μm). Nonetheless, it should be noted that the obtained distribution of the electric field is inhomogeneous in the above-mentioned areas. Similar observations can be drawn from the computations performed by using the electrical conductivity of the ZnO thin films deposited at 60 $^{\circ}\text{C}$. Also, the ZnO bulk material

properties remain unchanged while considering a single Pt/ZnO/Pt structure and the equivalent circuit model consisting of the sum of each individual back-to-back Schottky diode current. However, the number of interdigitated fingers n_{if} must be modified according to the design in use, when considering the Schottky contact area in the equivalent circuit model. Based on these considerations, the Schottky contact area A corresponding to the entire structure was thus calculated as:

$$A = (t_{Pt} \cdot 2) \cdot l_{if} \cdot n_{if} \quad (4.25)$$

Where t_{Pt} is the thickness of the Pt metal electrode (200 nm), the factor 2 takes into account the extension of the Schottky contact area on the top the electrode, l_{if} is the length of the interdigitated finger ($\sim 280 \mu\text{m}$) and n_{if} is the number of interdigitated fingers on a single set, which depends on the design use. The resulting Schottky contact area values as a function of the design are reported in Table 4.2.

Parameters \ Reference design	"1"	"2"	"3"	"4"
n_{if}	30	20	15	59
$A \text{ (m}^2\text{)}$	3.36×10^{-9}	2.24×10^{-9}	1.68×10^{-9}	4.48×10^{-9}

Table 4.2. Estimation of the Schottky contact area for the different IDE configurations.

The Schottky contact area values are expectedly increasing as the number of interdigitated fingers are increased, depending on the considered design. Nonetheless, it should be kept in mind that these values are based on a few estimations, which may further lead to a minor deviation in the electrical current properties during their subsequent fitting.

4.2.2.2. Determination of the Schottky barrier height

The method adopted for the determination of the Schottky barrier height involves the measurement of the saturation current value I_S at zero voltage. The saturation current I_S is expressed as:

$$I_S = A \cdot A^* \cdot T^2 \cdot \exp\left(-\frac{q \cdot \phi_B^{\text{eff}}}{k_B \cdot T}\right) \quad (4.26)$$

Where ϕ_B^{eff} is the effective Schottky barrier height, arising from the contributions of both the image-force lowering and the static lowering at zero bias voltage on the original barrier height ϕ_B . This method then takes benefit from the linear relationship between the natural logarithm of the saturation current I_S and the effective Schottky barrier height ϕ_B^{eff} [42,43]. The saturation current is determined by extrapolating the semilogarithmic (I-V) characteristics to $V = 0$ V. The effective Schottky barrier height can thus be extracted from the expression of the saturation current at 0 V and is expressed as [44]:

$$\phi_B^{\text{eff}} = \frac{k_B \cdot T}{q} \cdot \ln\left(\frac{A \cdot A^* \cdot T^2}{I_S}\right) \quad (4.27)$$

Consequently, the determination of the saturation current was performed via the semilogarithmic (I-V) characteristics of the forward biased W/ZnO/Pt single Schottky junction (with Pt as a bottom electrode, and where W is the tungsten tip probe of the (I-V) testing station) displayed in Fig. 4.9(b). These measurements were realized at 300 K in complete dark conditions, using a Schottky contact area value estimated at 0.15 cm². The Richardson constant value of 32 A.cm⁻².K⁻² for n-type ZnO was used [12]. The corresponding results showing the extrapolation of the saturation current to $V = 0$ V are reported in Fig. 4.23(a) and Fig. 4.23(b), for ZnO thin films grown by ALD at 80 °C and 60 °C, respectively.

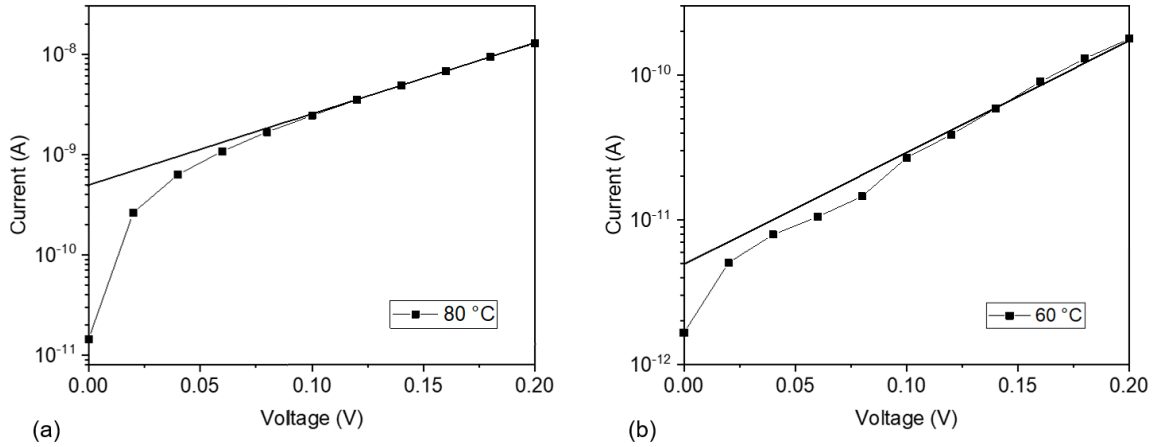


Figure 4.23. Extrapolation of the saturation current to $V = 0$ V from the semi-logarithmic (I - V) characteristics of forward biased W/ZnO/Pt junctions (with Pt as a bottom electrode), (a) for a ZnO thin grown by ALD at 80 °C and (b) for a ZnO thin grown by ALD at 60 °C.

The saturation current values measured for ZnO thin films deposited by ALD at 80 °C and 60 °C are $I_s^{80^\circ\text{C}} = 493$ pA and $I_s^{60^\circ\text{C}} = 4.94$ pA, respectively. The resulting effective Schottky barrier heights calculated from equation (4.27) at both deposition temperatures are $\phi_B^{\text{eff } 80^\circ\text{C}} = 0.889$ V and $\phi_B^{\text{eff } 60^\circ\text{C}} = 1.008$ V. Based on these calculations, it can be concluded that the ALD deposition parameters we developed in this study are well adapted for the fabrication of a Schottky junction at the interface between the ZnO thin film and the Pt metal electrodes.

Furthermore, it is necessary to modify the equations (4.22) and (4.23) in order to express the original Schottky barrier height ϕ_B as a function of the effective barrier height ϕ_B^{eff} , while also taking into account the contributions of both the image-force lowering and the static lowering at zero bias voltage.

Consequently, the Schottky barrier height is expressed as:

$$\phi_B = \phi_B^{\text{eff}} + \Delta\phi_B(0 \text{ V}) + \Delta\phi_B'(0 \text{ V}) \quad (4.28.1)$$

$$\phi_B = \phi_B^{\text{eff}} + \left[\frac{q^3 \cdot N_D}{8 \cdot \pi^2 \cdot \epsilon_s^3} \cdot V_D \right]^{1/4} + \alpha \cdot \sqrt{\frac{2 \cdot q \cdot N_D}{\epsilon_s} \cdot V_D} \quad (4.28.2)$$

Consequently, these equations have been implemented within the master equations (4.22) and (4.23), describing the conduction mechanism through the forward and reverse biased Schottky junctions.

4.2.2.3. Determination of the built-in voltage

As previously mentioned and illustrated in Fig. 4.16, the built-in voltage can be defined as the distance between the conduction band and the effective Schottky barrier height in a M-S junction at thermal equilibrium. The built-in voltage V_D is expressed as:

$$V_D = \phi_B^{\text{eff}} - \xi \quad (4.29)$$

Where ξ is the distance between the Fermi level and the bottom of the conduction band. The value of ξ is often approximated to 0.1 V in the literature while using ZnO as a semiconducting material [45]. However, this approximation is wrong as different electron concentrations lead to deviations from this constant value. Consequently, ξ was expressed as a function of the electron concentration N_D , using [11]:

$$\xi = \frac{k_B \cdot T}{q} \cdot \ln\left(\frac{N_C}{N_D}\right) \quad (4.30)$$

Where N_C is the effective density of states in the conduction band, which is further calculated using the following expression [11]:

$$N_C = 2 \cdot \left(\frac{2 \cdot \pi \cdot m^* \cdot k_B \cdot T}{h^2}\right)^{\frac{3}{2}} \quad (4.31)$$

Where h is the Plank constant.

The built-in voltage V_D is determined using the value of the distance ξ between the Fermi level and the bottom of the conduction band calculated with equation (4.30), together with the effective Schottky barrier height value determined previously. This method thus allows for a determination of the built-in voltage V_D as a function of the electron concentration N_D . The dependence of the effective Schottky barrier height on

the electron concentration is taken into account in the different values of ϕ_B^{eff} determined previously for ALD deposition temperatures of 80 °C and 60 °C.

The evolution of V_D for different electron concentration values using the effective Schottky barrier heights determined at deposition temperatures of 80 °C and 60 °C is presented in Fig. 4.24.

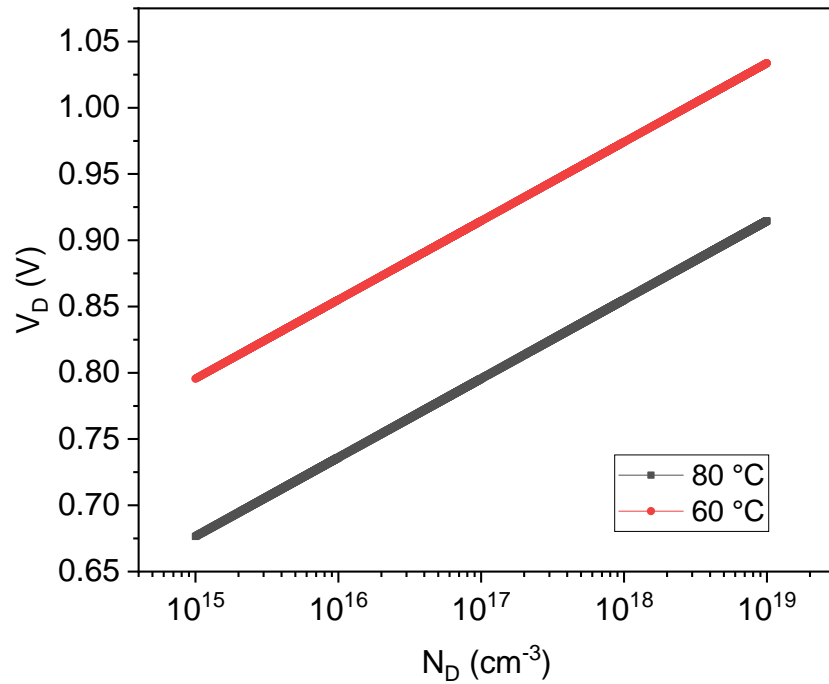


Figure 4.24. Evolution of V_D for electron concentration values ranging between 10^{15} cm^{-3} and 10^{19} cm^{-3} , using the effective Schottky barrier heights determined at deposition temperatures of 80 °C and 60 °C.

As observed from Fig. 4.24, the distance ξ between the Fermi level and the bottom of the conduction band is decreased as the electron concentration values N_D are increased, which leads concomitantly to an increase of the built-in voltage values V_D for higher electron concentrations.

4.2.2.4. Rationalization of the intrinsic barrier lowering coefficient

This section aims at discussing the physical origin of the intrinsic barrier lowering coefficient α , introduced within the developed conduction mechanism to explain the increased leakage current through the reverse biased Schottky junction. It should be reminded that this parameter is based on an empirical relation, where it is multiplied

by the maximum electric field E_{m1} to generate an additional reduction in the Schottky barrier height value for increased applied bias voltages. The physical origin associated with the phenomenon of static lowering is still a matter of discussion. J. M. Andrews et al. [38] stated that an electrostatic dipole layer is induced at a M-S junction free from interfacial layer oxide, interface states or contaminants. The electrostatic dipole layer arises from the presence of electrons in the metal, these electrons having wave functions penetrating into the semiconductor band gap [11,38]. However, they extended the application of the static lowering to all M-S interfaces, reporting that the presence of an interfacial layer or interface states could induce a similar field-dependence on the Schottky barrier height. Moreover, the hypothesis of an intimate M-S contact, free from interfacial layer or interface states is very unlikely, as almost all Schottky junctions present one of the above-mentioned interface effects (unless they are prepared in ultra-high vacuum conditions or by molecular beam epitaxy (MBE) [21]). J. Bardeen [46] first introduced in 1947 a model taking into account the presence of interface states at the M-S junction, by considering a continuous distribution of energy levels at the interface. Moreover, E.H. Rhoderick et al. [21] pointed out that the electrical centres of the interface states must be separated from the metal to have an observable effect on the electrical properties of the M-S junction. Consequently, the region of the semiconductor between the metal and the electrical centre of the interface states would present a similar behaviour as an insulating oxide layer, inducing an electrostatic dipole at the interface leading to the Schottky barrier height lowering. In the case of an interfacial oxide layer, the intrinsic barrier lowering coefficient α could thus be interpreted as the lateral thickness of the oxide layer, while in the case of interface states, α could be interpreted as the distance between the metal and the electrical centre of these interface states.

The formation of localized interface states has been thoroughly reported in M-S Schottky junctions using ZnO as the semiconducting material [10,47,48]. These interface states are localized at energies corresponding to native point defects of the bulk ZnO (i.e. oxygen vacancies, zinc interstitials), while the metal and its deposition temperature contacting the ZnO further determines the nature of these states [10]. Among the native point defects of ZnO, oxygen vacancies have been shown to play a major role at the M-S interface by pinning the Fermi level close to their defect level (at

~ 0.7 eV below the conduction band minimum), making the junction almost insensitive to the metal work function [48]. Furthermore, M. W. Allen et al. [47] showed that oxidized noble metal such as PtO_x in contact with n-type ZnO (grown by hydrothermal method) were forming higher Schottky barrier heights compared to the plain metal counterparts. They attributed this increase in the Schottky barrier height to a reduction in the interfacial oxygen vacancies, due to the oxidizing environment. Additionally, they reported a substantial increase of the Schottky barrier height values between the O-polar face (0.98 eV) and the Zn-polar face (1.20 eV), which is further linked to the increase of oxygen vacancies at the M-S in the case of the O-polar face. Nonetheless, it should be noted that the oxidation of the Pt metal in this study was intentionally provoked by depositing the metal in an oxidizing environment.

Within the frame of our work, a plasma treatment consisting mostly of oxygen was performed on the Pt metal electrodes (60 mTorr, **O₂ - 38 sccm**, Ar - 2 sccm, 50 W, 5 min) prior to the ZnO thin film deposition by ALD. It should be noted that the realization of this plasma treatment was performed on every sensor and consist in a mandatory step within the microfabrication process to increase the substrates' surface wettability, as well as the subsequent adhesion between the different layers.

To investigate the potential formation of an interfacial oxide layer at the Pt/ZnO junctions, XPS measurements were performed on the surface of two Pt samples. More precisely, a reference Pt sample was left exposed to air during several days, while another Pt sample was treated with a similar oxygen rich plasma treatment as the one realized prior to ALD deposition, and immediately transferred to a vacuum chamber for XPS analysis. The obtained XPS survey spectrums corresponding to the Pt 4f core level are displayed in Fig. 4.25. As shown in Fig. 4.25(a), the survey spectrum of the reference Pt sample exposed to environmental conditions exhibits two peaks, deconvoluted in a major contribution from the plain Pt metal, as well as a minor contribution attributed to the PtO / Pt(OH)₂ chemical state [49,50]. However, the survey spectrum obtained for the Pt sample exposed to the oxygen rich plasma, displayed in Fig. 4.25(b), exhibits the emergence of a third contribution attributed to the PtO₂ chemical state [49–51]. These results thus suggest that the oxidation of the Pt metal is arising from two main contributions, where the PtO / Pt(OH)₂ chemical state is stable in environmental conditions while the PtO₂ chemical state is introduced by the oxygen

rich plasma treatment. This is concomitant with the work of J.J. Blackstock et al. [50], who reported the formation of an amorphous ~ 2.5 nm PtO_2 oxide layer on the surface of bare Pt metal exposed to oxygen plasma, whose thickness was independent of the plasma time (from 1 min up to 15 min). They reported as well the formation of a ~ 0.5 nm $\text{Pt}(\text{OH})_2$ oxide layer after exposure to ambient conditions, on top of the PtO_2 oxide layer.

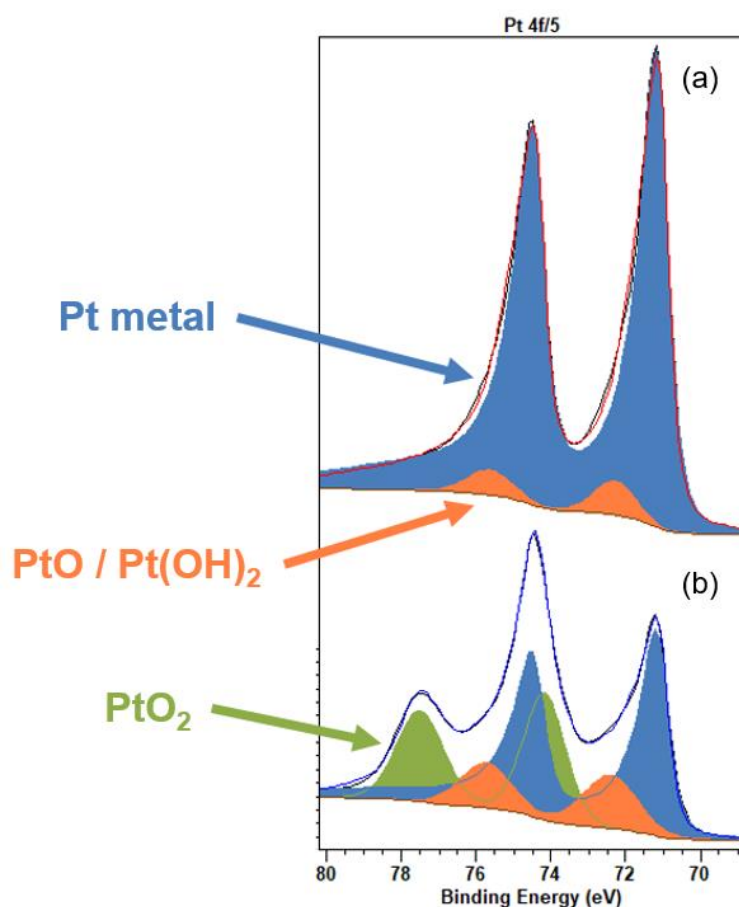


Figure 4.25. XPS survey spectrums of the Pt 4f core level. (a) Reference platinum sample left in air for several days; (b) Platinum sample treated by the oxygen rich plasma right before XPS analysis.

Consequently, it appears clear that Pt metal surface is oxidized by the performed plasma treatment prior to ALD deposition. Nonetheless, previous reports [49–51] suggest the formation of an ultrathin amorphous oxide layer at the Pt surface. Based on these elements, it is thus difficult to associate the static lowering phenomenon to either the presence of an interfacial oxide layer or interface states at the M-S junction.

In order to further assess the potential presence of an interfacial oxide layer at the Pt/ZnO junctions, high resolution TEM investigations were performed, in an approach similar to that adopted for XPS measurements. Two distinct Si samples were first coated with a ~ 100 nm layer of Pt by EBME. The reference was subsequently left exposed to ambient conditions, while the oxygen rich plasma treatment (same as before) was performed on the second sample (further referred as oxidized sample), where the PtO₂ oxide layer is expected to be formed. Subsequently, they were both coated within the same ALD process with a ~ 300 nm thin film of ZnO at a deposition temperature of 80 °C. The resulting TEM micrographs of the Pt/ZnO interface for the reference Pt sample and the oxidized Pt sample are presented in Fig. 4.26 and Fig. 4.27, respectively.

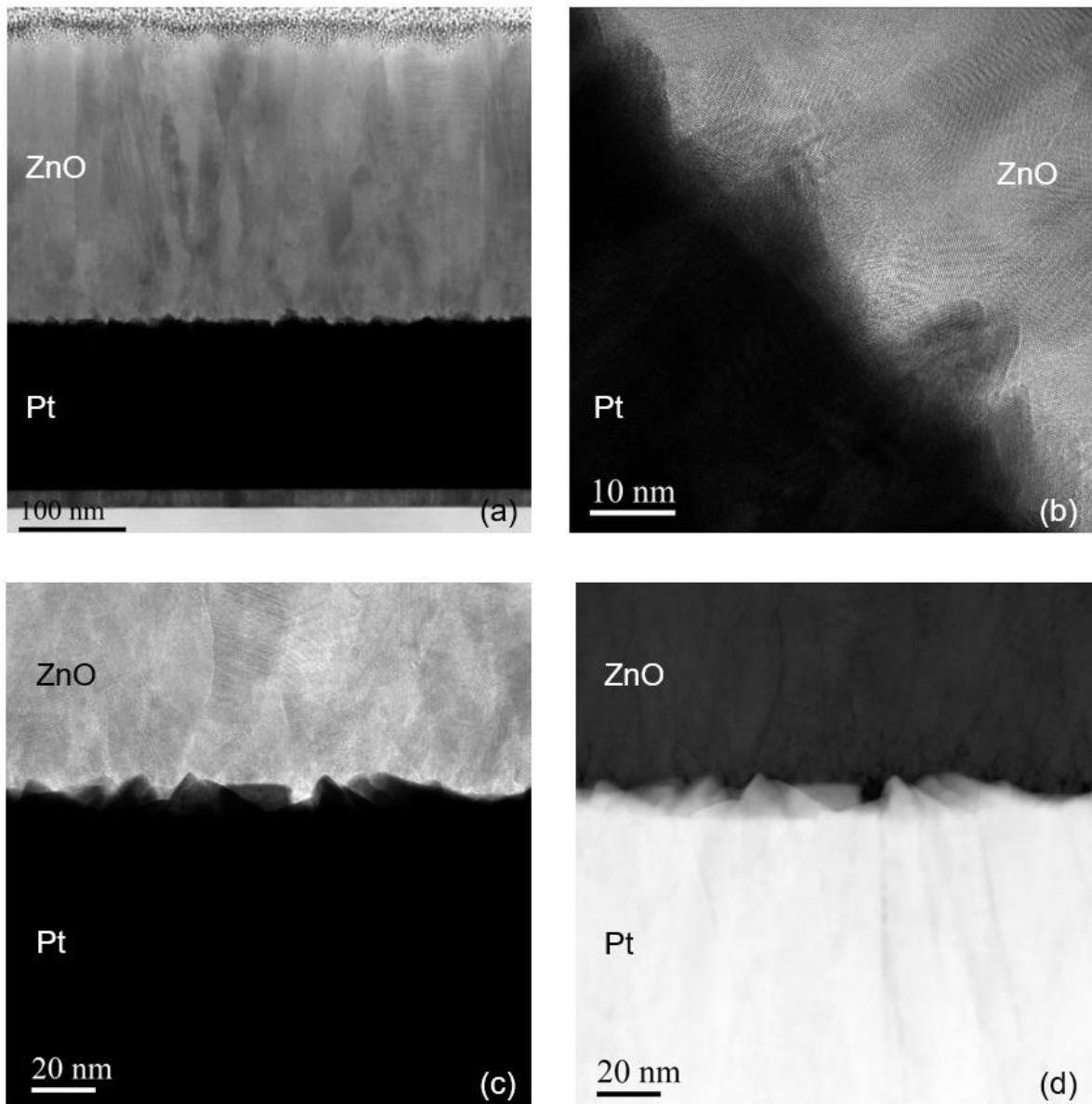


Figure 4.26. (a) Scanning transmission electron microscopy (STEM) Bright Field (BF) micrograph, (b) High-resolution TEM (HRTEM) micrograph, (c) STEM BF micrograph and (d) STEM High Angle Annular Dark Field (HAADF) micrograph of the Pt/ZnO for the reference Pt sample.

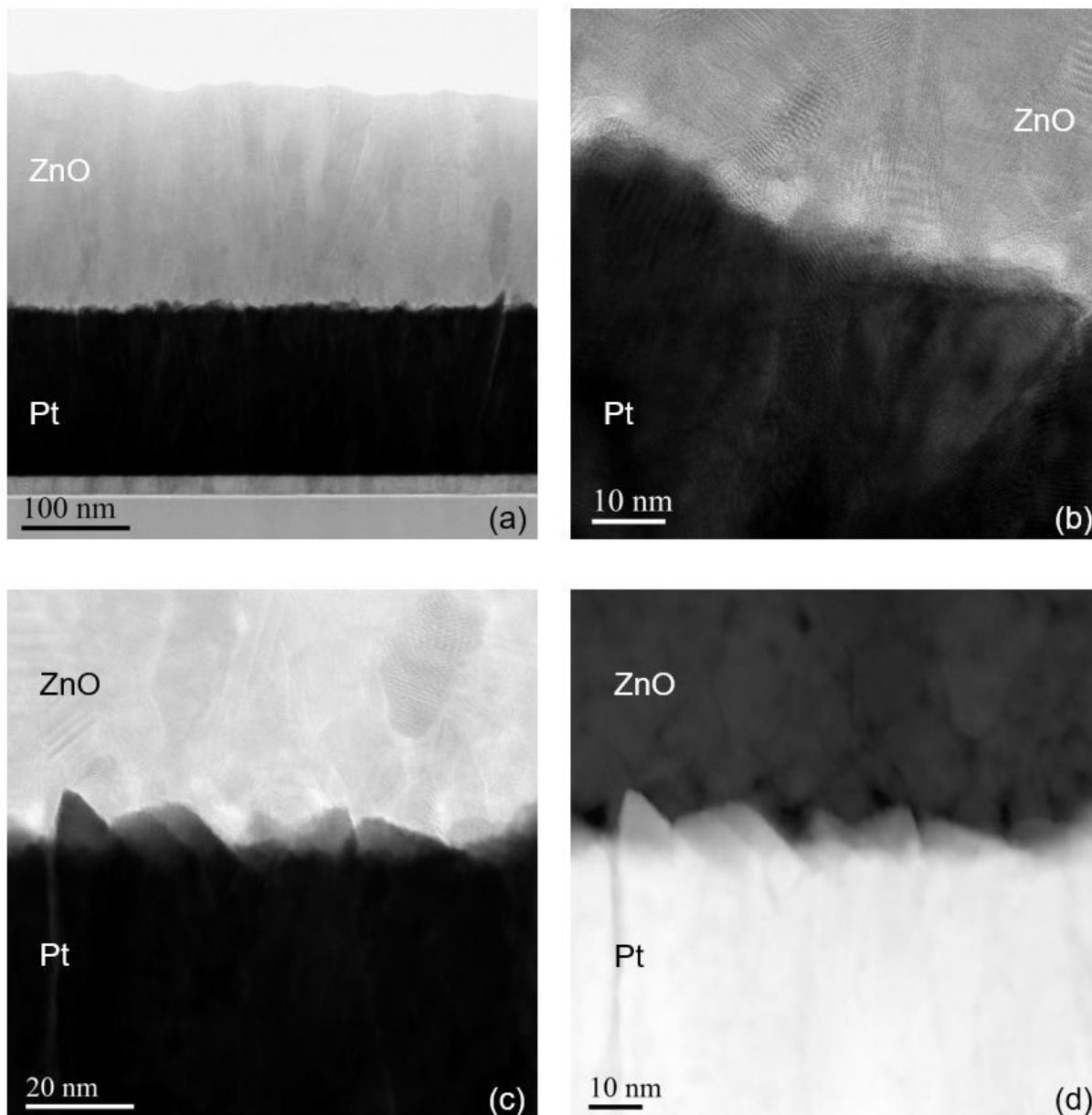


Figure 4.27. (a) STEM BF micrograph, (b) HRTEM micrograph, (c) STEM BF micrograph and (d) STEM HAADF micrograph of the Pt/ZnO interface for the oxidized Pt sample.

The micrographs of the Pt/ZnO interfaces obtained at different magnifications from both the reference and the oxidized sample show that no clear, continuous interfacial oxide layer is formed at the M-S junctions. Nonetheless, for both samples, the interface is highly affected by the roughness of the Pt metal, extending up to 10 nm. Moreover, from the STEM BF and DF micrographs (Fig. 4.26 (c) and (d), Fig. 4.27 (c) and (d)), the interface area between both materials seem to appear as a grey transition colour, defined on an approximate distance of 10 nm. This transition area at the Pt/ZnO

interface can be clearly observed from a STEM DF micrograph obtained on the oxidized sample, depicted in Fig. 4.28.

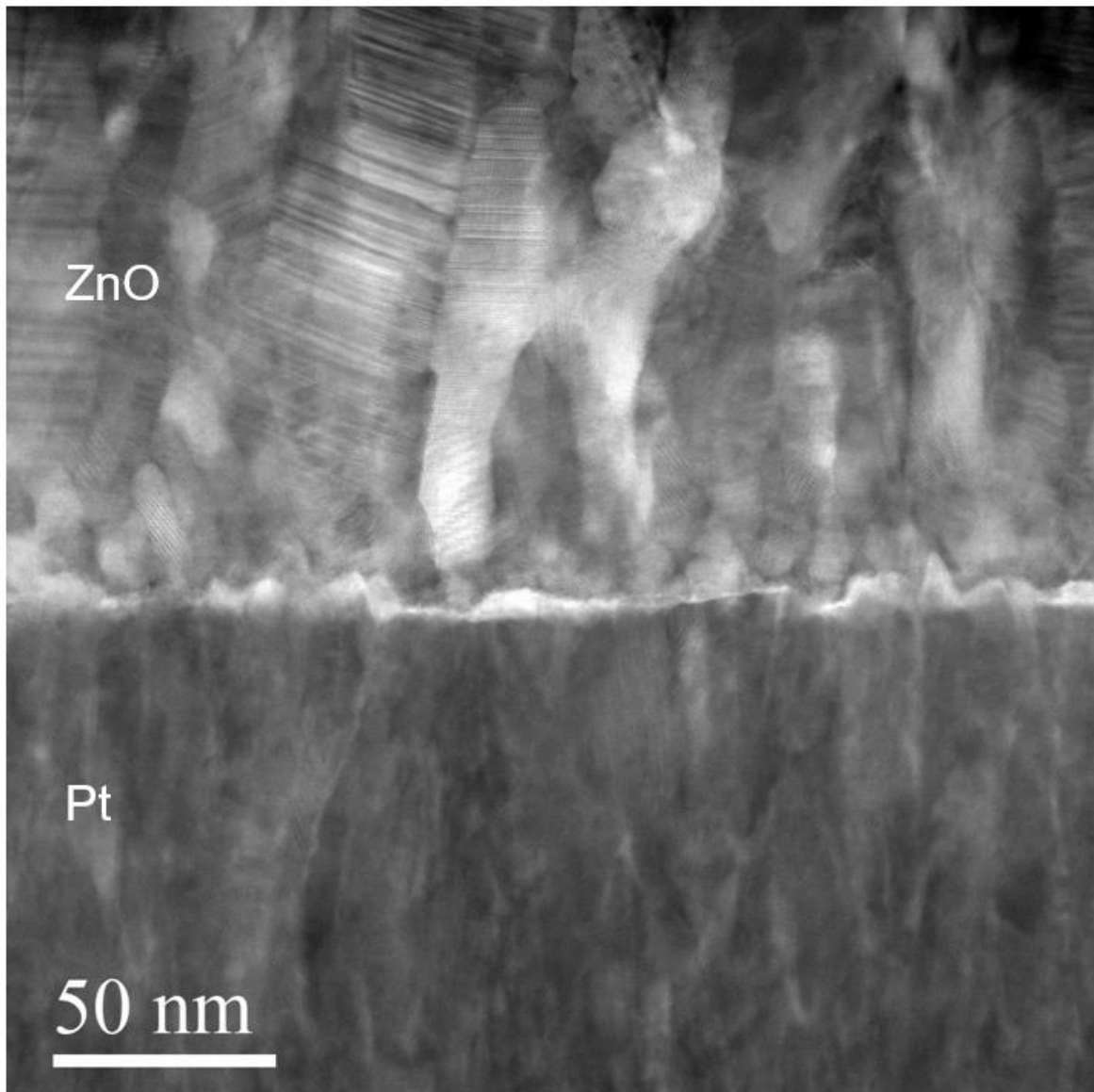


Figure 4.28. STEM Dark Field (DF) micrograph of the Pt/ZnO interface for the oxidized Pt sample.

As stated previously, the transition area between both materials is non continuous and seems to highly depend on the roughness of the Pt metal. As the same interface state can be observed from the reference and the oxidized sample, it is thus unwise to link this transition area to an interfacial oxide layer. Furthermore, the image intensity in STEM DF and BF micrographs is proportional to the atoms' atomic number. As the intensity of the interface appears differently from the bulk Pt and ZnO materials, it could thus be stated that a phenomenon of interdiffusion is occurring at the M-S interface.

Consequently, the elemental composition at the Pt/ZnO interface was investigated by acquiring electron energy loss spectroscopy (EELS) maps combined with STEM. The elemental distribution maps for O (red) and Pt (blue) at the Pt/ZnO interface for the oxidized sample are displayed in Fig. 4.29.

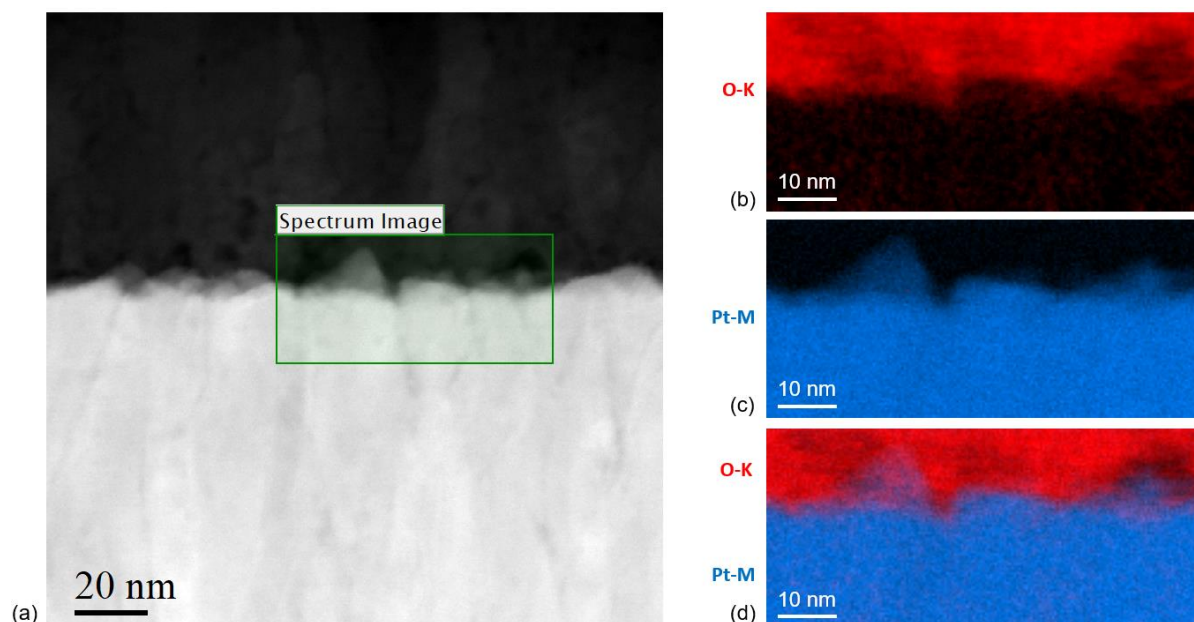


Figure 4.29. (a) STEM HAADF micrograph of the Pt/ZnO interface on the oxidized Pt sample, where the outlined green box corresponds to the area where the EELS maps were acquired. (b) Individual elemental distribution map for O (red). (c) Individual elemental distribution map for Pt (blue). (d) Composite distribution map for O (red) and Pt (blue). K and M correspond to the electron shells associated to the respective materials.

It should be noted that the individual elemental distribution map obtained for Zn was similar to O and was thus not displayed for purposes of clarity. It appears clear from Fig. 4.29(b), (c) and (d) that interdiffusion is occurring at the Pt/ZnO interface, where both O and Pt atoms can be observed at the transition area between the bulk materials. Interestingly, this phenomenon seems to be facilitated and extended on the areas when the roughness of the Pt metal is more important.

To further quantitatively assess the respective presence of oxygen, zinc and platinum atoms at the M-S junction, energy dispersive X-ray spectrometry (EDS) line profiles were realized at the Pt/ZnO interface, with a step length of 1.4 nm along the line profiles. The resulting atomic percentage At% for each atom along the distance of the line profile at the interface for the reference Pt sample and the oxidized Pt sample are shown in Fig. 4.30 and Fig. 4.31, respectively.

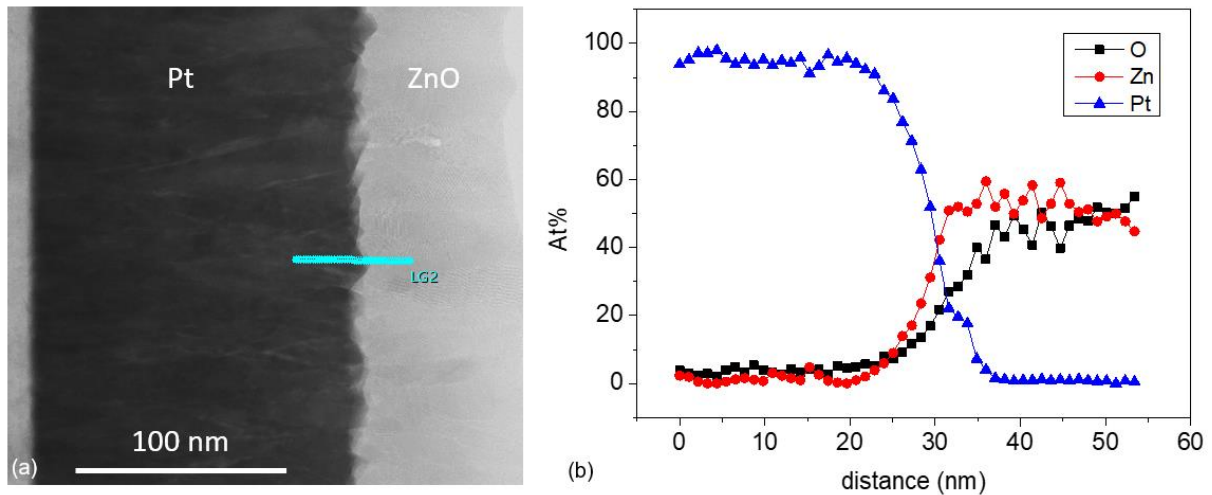


Figure 4.30. (a) Micrograph showing the line profile defined at the Pt/ZnO interface of the reference Pt sample. (b) At% of O, Zn and Pt atoms obtained by EDS analysis as a function of the distance along the line profile.

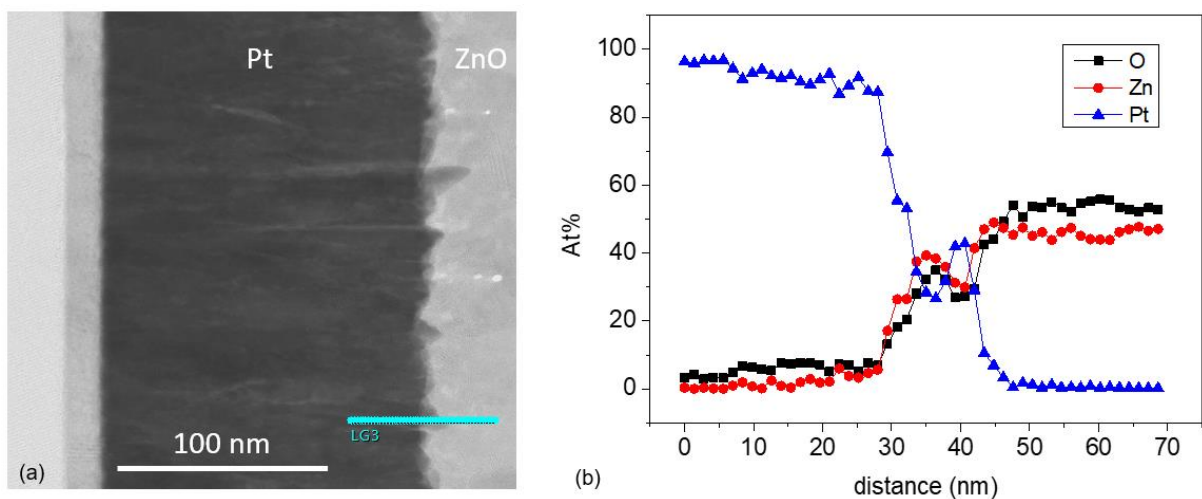


Figure 4.31. (a) Micrograph showing the line profile defined at the Pt/ZnO interface of the oxidized Pt sample. (b) At% of O, Zn and Pt atoms obtained by EDS analysis as a function of the distance along the line profile.

The obtained graphs further confirm the presence of an interdiffusion area showing a coexistence of O, Zn and Pt atoms, extending over a defined distance at Pt/ZnO interface. A total of five line profiles were acquired at different localisations of the Pt/ZnO interface for both the reference Pt and the oxidized Pt samples. The obtained %At of each atom from the EDS analysis corresponding to these line profiles all showed similar trends as the graphs displayed in Fig. 4.30(b) and Fig. 4.31(b). Interestingly, the At% of Zn is constantly slightly higher than the At% of O within the interdiffusion area, while their respective relative contribution equilibrates as the

distance from the interdiffusion area is increased. Moreover, the length of the interdiffusion area seems to be substantially increased where the Pt surface presents a high roughness, as demonstrated by Fig. 4.31(b) where the length of the interdiffusion extends over nearly 20 nm. It could thus be stated that the observed coexistence of the O, Zn and Pt atoms might be linked to an overlapping of the Pt metal substrate and the ZnO thin film at the interface between both materials. Nonetheless, the average length of this interdiffusion area was estimated at a value of 13.2 nm for the reference Pt sample and 13.34 nm for the oxidized Pt sample, with a minimum length of 8.2 nm and a maximum length of 19.6 nm. These results thus suggest that the interdiffusion phenomenon is similar for both the reference Pt and the oxidized Pt sample, showing no specific impact of the performed oxygen rich plasma treatment at the Pt/ZnO interface of the oxidized sample. The presence of this interdiffusion area might thus lead to an increase in the density of point defects (i.e. zinc interstitials and oxygen vacancies), concomitantly increasing the density of interface states at the Pt/ZnO junction. Based on these considerations, the increase of the leakage current due to static lowering can most likely be attributed to the presence of interface states at the Pt/ZnO junction, where α could be interpreted as the distance between the metal and the electrical centre of these interface states. However, estimating the distance α from the obtained TEM micrographs would not be rigorous. Instead, the value of α will be determined empirically, from the performed fitting of the experimental (I-V) curves.

4.2.2.5. Determination of the interface trap states density and time constant through (C-f) and (G-f) measurements

This section aims at investigating the density as well as the time constant of the interface trap states at Pt/ZnO/Pt junctions. Within this scope, capacitance-frequency (C-f) and conductance-frequency (G-f) measurements were performed with an impedance analyser (E4990A Impedance Analyzer, Keysight). A constant AC modulation with an amplitude of 500 mV was superimposed on to a DC bias voltage. The frequency was varied with a logarithmic sweep between 20 Hz and 1 MHz, for defined bias voltage values of 0 V, 1 V, 2 V, 4 V, 6 V, 8 V and 10 V. The devices were contacted with tungsten probes via a probe station (PM8, Cascade Microtech) in dark conditions. The equivalent circuit models of Schottky M-S diodes are presented in Fig.

4.32. It is adapted for a double junctions configuration from the single Schottky barrier model originally proposed by E.H. Rhoderick and R. H. Williams on Figure 4.6(d) of their book [21]. This model takes into account the different capacitive and conductive contributions from both Schottky M-S diodes [21], the reverse and forward biased Schottky junctions together with their respective parameters being designated as 1 and 2, respectively. C_S is the capacitance corresponding to the Schottky depletion region, C_{it} is the capacitance induced by interface trap states, C_{ox} is the oxide capacitance located at the M-S junction, while R_{it} is a resistance representing the lossy process induced by the capture and emission of electrons at the interface trap states.

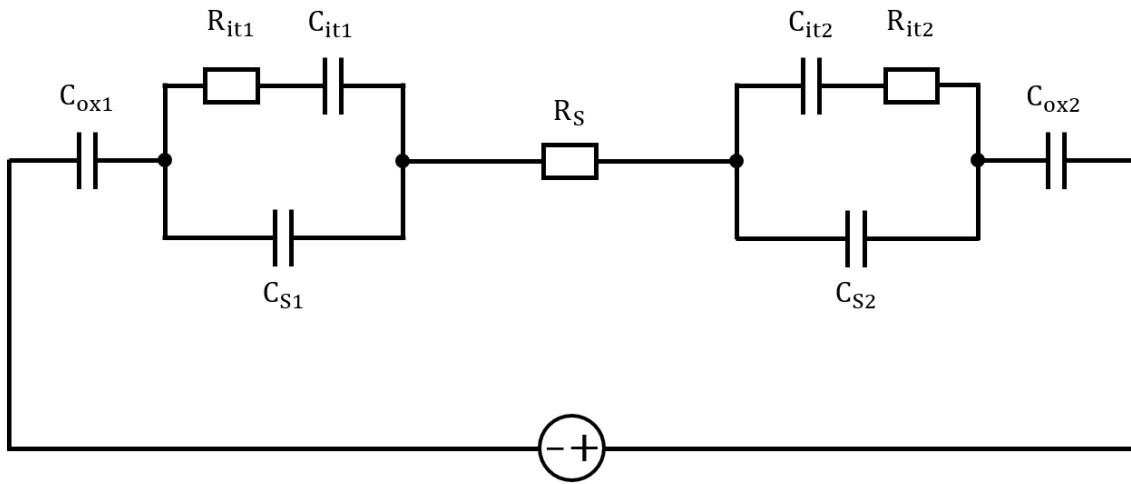


Figure 4.32. Equivalent circuit model of the Pt/ZnO/Pt Schottky junctions, with constitutive capacitance and conductance contributions from each Schottky diode.

The capacitance corresponding to the Schottky depletion region of the reverse and forward biased Schottky junctions C_{S1} and C_{S2} are respectively expressed as:

$$C_{S1} = A \cdot \sqrt{\frac{q \cdot \epsilon_s \cdot N_D}{2 \cdot (V_1 + V_D)}} \quad (4.32)$$

$$C_{S2} = A \cdot \sqrt{\frac{q \cdot \epsilon_s \cdot N_D}{2 \cdot (V_D - V_2)}} \quad (4.33)$$

Where A is the Schottky contact area, whose value was estimated previously within the section 4.2.2.1. The measurements carried out within this section were performed

with devices processed with the reference design “2” (see Table 4.2), with a corresponding Schottky contact area of $2.24 \times 10^{-9} \text{ m}^2$.

By considering two ideal Schottky junctions free from interface states, the total capacitance C_S of the Pt/ZnO/Pt Schottky junctions would result from both capacitances C_{S1} and C_{S2} in series, as [24]:

$$C_S = \frac{C_{S1} \cdot C_{S2}}{C_{S1} + C_{S2}} = A \cdot \sqrt{\left(\frac{q \cdot \epsilon_s \cdot N_D}{2}\right)} \cdot \left[\frac{1}{\sqrt{V_1 + V_D} + \sqrt{V_D - V_2}} \right] \quad (4.34)$$

Based on the assumption of ideal interfaces, equation (4.34) thus predicts a gradual decrease of the total capacitance of the M-S-M structure, arising mainly from the increase of the voltage drop and the depletion region at the reverse biased Schottky junction. As the imposed bias voltage V increases, most of it will thus be distributed across the reverse biased Schottky junction and the total capacitance can be reduced to:

$$C_S \approx A \cdot \sqrt{\left(\frac{q \cdot \epsilon_s \cdot N_D}{2}\right)} \cdot \left[\frac{1}{\sqrt{V + V_D} + \sqrt{V_D}} \right] \quad (4.35)$$

Based on this approximation and using the previously determined values of the built-in voltage V_D , it is therefore possible to estimate the total capacitance C_S as a function of the applied bias voltage V . The total capacitance values are reported for electron concentration values ranging between 10^{15} cm^{-3} and 10^{18} cm^{-3} , as well as for ZnO thin grown by ALD at $80 \text{ }^\circ\text{C}$ and $60 \text{ }^\circ\text{C}$, in Fig. 4.33(a) and Fig. 4.33(b), respectively.

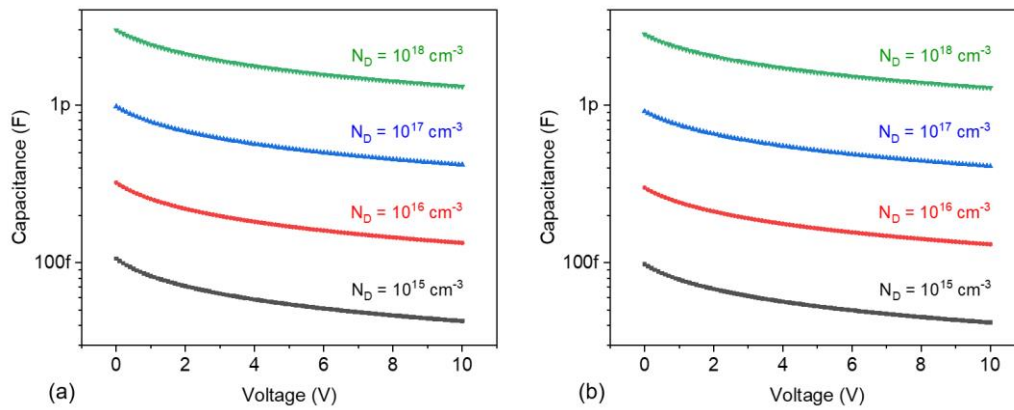


Figure 4.33. Evolution of the capacitance of the Schottky depletion region for electron concentration values ranging between 10^{15} cm^{-3} and 10^{18} cm^{-3} , (a) for a ZnO thin grown by ALD at $80 \text{ }^\circ\text{C}$ and (b) for a ZnO thin grown by ALD at $60 \text{ }^\circ\text{C}$.

As observed, the total capacitance C_s based on the assumption of ideal interfaces takes values in the range of tens of femtoFarads and increases to a few picoFarads as the electron concentration is increased from 10^{15} cm^{-3} to 10^{18} cm^{-3} . It is thus convenient to compare these values with the experimental (C-f) and (G-f) characteristics for ZnO thin films deposited at $80 \text{ }^\circ\text{C}$ and $60 \text{ }^\circ\text{C}$, presented in Fig. 4.34 and Fig. 4.35, respectively.

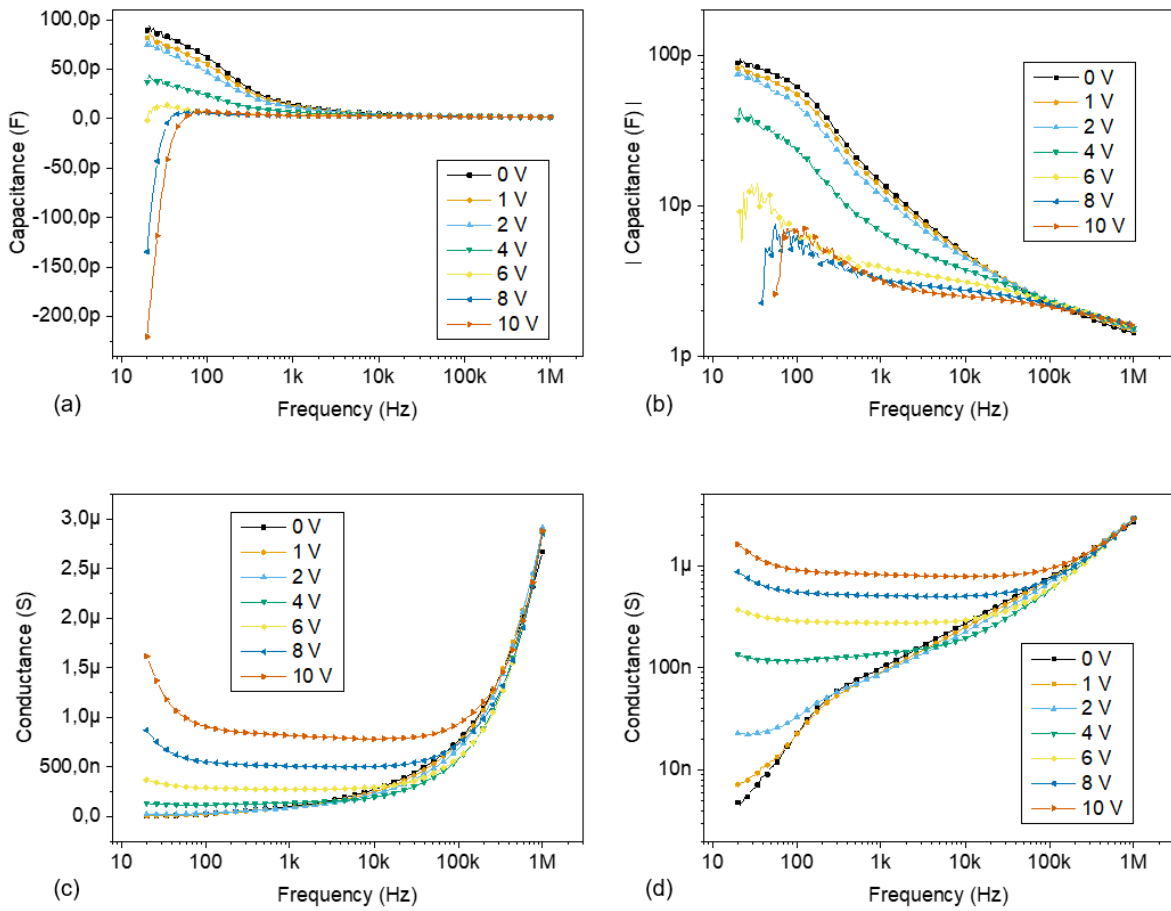


Figure 4.34. (C-f) and (G-f) characteristics under dark conditions, for a ZnO thin film deposited by ALD at $80\text{ }^{\circ}\text{C}$, with different fixed bias voltages ranging between 0 V and 10 V. The frequency was varied with a logarithmic sweep between 20 Hz and 1 MHz; (a) (C-f) characteristics, semi-log scale; (b) (C-f) characteristics, log-log scale; (c) (G-f) characteristics, semi-log scale; (d) (G-f) characteristics, log-log scale. Only the positive capacitance values are displayed in the graphs (b) with a log-log scale.

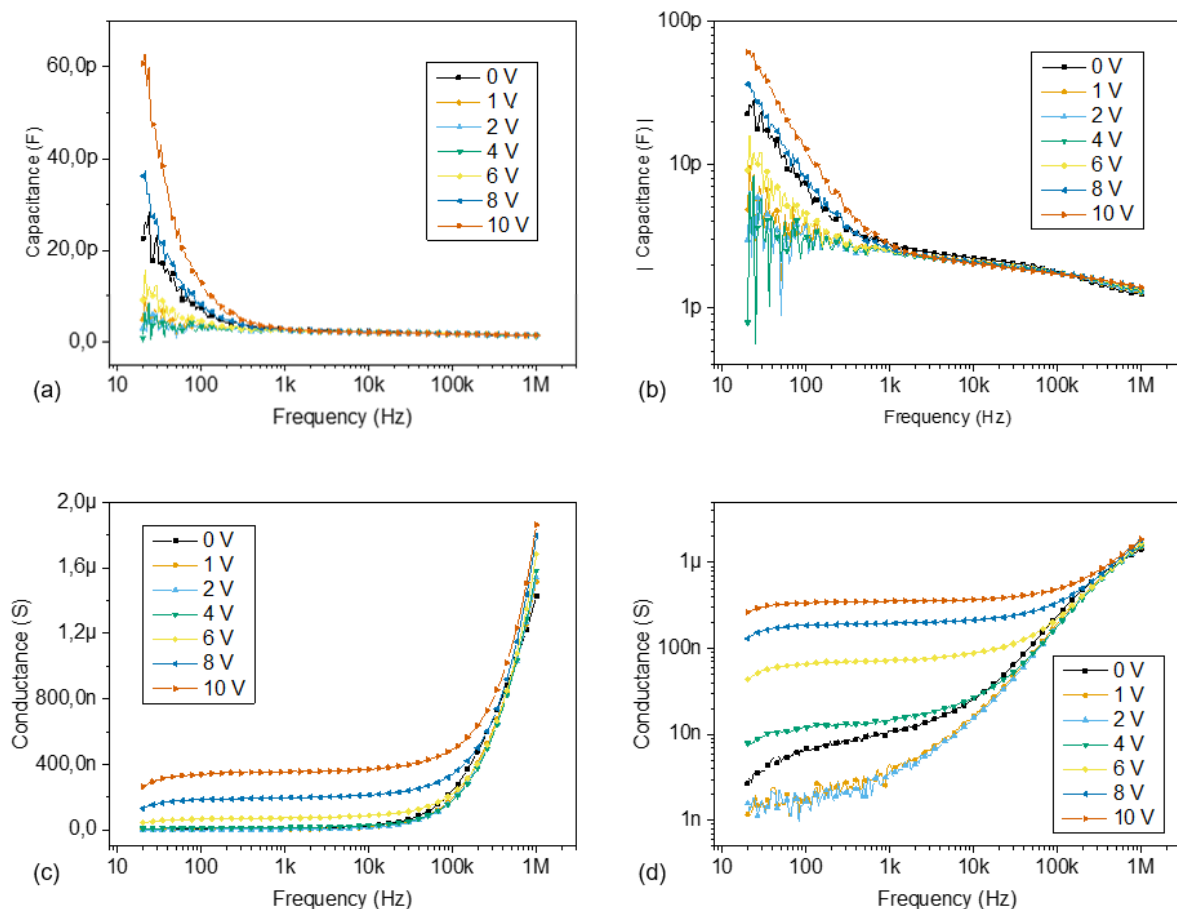


Figure 4.35. (C-f) and (G-f) characteristics under dark conditions, for a ZnO thin film deposited by ALD at $60\text{ }^{\circ}\text{C}$, with different fixed bias voltages ranging between 0 V and 10 V. The frequency was varied with a logarithmic sweep between 20 Hz and 1 MHz; (a) (C-f) characteristics, semi-log scale; (b) (C-f) characteristics, log-log scale; (c) (G-f) characteristics, semi-log scale; (d) (G-f) characteristics, log-log scale. Only the positive capacitance values are displayed in the graphs (b) with a log-log scale.

As displayed in Fig. 4.34 and Fig. 4.35, it can be clearly observed that the values of capacitance and conductance are dependent on both the frequency and the applied DC bias voltage. Moreover, the measured capacitance values at lower frequencies are very different from the Schottky junction capacitance values estimated in Fig. 4.33, which predict a gradual decrease of the capacitance as the bias voltage and the depletion region are increased. This dispersive behaviour of the measured capacitance values as a function of the frequency depends on the ability of the charge carriers to follow the AC signal and is directly linked with the presence of interface trap states at the Schottky junctions. At lower frequencies, the charges localized at the interface trap states are able to follow the AC signal and yield an excess capacitance, corresponding to C_{it} , whose value depends on the relaxation time of the interface trap states, and

increases with decreasing frequencies. However, as the applied frequency is increased, the charges at the interface trap states are less and less able to follow the AC signal, which results in a decrease in the observed capacitance values, linked to the decrease of C_{it} . The capacitance values are reduced to a few picoFarads at 1 MHz, effectively converging towards a range of values corresponding to the Schottky depletion region C_S . Furthermore, in low frequency regime (below 100 Hz) negative capacitance values can be observed in Fig. 4.34(a). This phenomenon will be thoroughly detailed within the next section.

Therefore, the density as well as the time constant of the interface trap states need to be assessed for a better understanding of the electrical characteristics of the Pt/ZnO/Pt junctions over the frequency range. Furthermore, our system consists of two back-to-back Schottky junctions, where one of the Schottky diode junction will necessarily be reversely biased while the other will be forward biased, depending on the sign of the applied bias voltage. Additionally, as shown previously in equation (4.35), the total capacitance of the device is dominated by the reverse biased Schottky junction capacitance. Consequently, the following analysis will be performed by assuming that the observed electrical characteristics of the Pt/ZnO/Pt junctions are linked with a single reverse biased Pt-ZnO Schottky junction.

Within this scope, the so-called conductance method was used, developed by Nicollian and Goetzberger [52]. This method was adopted in several works [53–55] to investigate the density D_{it} and the time constant τ of the interface trap states in Schottky junctions. It relies on the measurement of the parallel conductance, representing the loss mechanism due to interface trap capture and emission of electrons, as a function of the frequency for given applied bias voltages. The conductance method consists of the contribution of the Schottky depletion region capacitance C_S , the interface trap capacitance C_{it} , as well as an oxide capacitance C_{ox} located at the M-S junction. The equivalent circuit models adapted to this method are presented in Fig. 4.36, assuming a negligible impact of the series resistance [44].

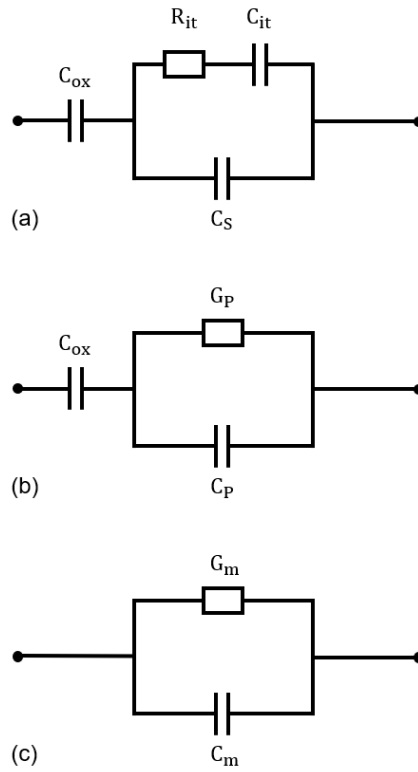


Figure 4.36. Equivalent circuit models of a Schottky junction adapted for the conductance method, with the (a) complete equivalent circuit model, the (b) simplified circuit and the (c) measured circuit.

Where C_p and G_p are the parallel capacitance and conductance, C_m and G_m are the measured capacitance and conductance, respectively, while R_{it} is a resistance representing the lossy process induced by the capture and emission of electrons at the interface trap states.

The parallel capacitance and conductance C_p and G_p are given by [44]:

$$C_p = C_s + \frac{C_{it}}{1 + (\omega \cdot \tau)^2} \quad (4.36)$$

$$G_p = \frac{A \cdot q \cdot \omega^2 \cdot \tau \cdot D_{it}}{1 + (\omega \cdot \tau)^2} \quad (4.37)$$

Where $\omega = 2 \cdot \pi \cdot f$ is the angular frequency, f being the applied frequency.

As observed from equations (4.36) and (4.37), the parallel conductance can be more easily interpreted than the parallel capacitance, as it is not expressed in terms of the Schottky depletion region capacitance C_S . Moreover, it should be noted that equations (4.36) and (4.37) are valid for interface trap states located at a single energy level in the band gap [44]. Considering a continuous distribution of interface trap states around the interface Fermi level, the parallel conductance normalized by the angular frequency ω can be further expressed as [52]:

$$\frac{G_p}{\omega} = \frac{A \cdot q \cdot D_{it}}{2 \cdot \omega \cdot \tau} \cdot \ln[1 + (\omega \cdot \tau)^2] \quad (4.38)$$

However, the capacitance and conductance values presented in Fig. 4.34 and Fig. 4.35 correspond to the measured capacitance and conductance C_m and G_m . Nonetheless, a circuit comparison of Fig. 4.36(b) to Fig. 4.36(c) yields the normalized parallel conductance as a function of C_m , G_m and the oxide capacitance C_{ox} , as [44]:

$$\frac{G_p}{\omega} = \frac{\omega \cdot G_m \cdot C_{ox}^2}{G_m^2 + \omega^2 \cdot (C_{ox} - C_m)^2} \quad (4.39)$$

At high frequencies (typically for frequencies values superior to 500 kHz [52]), the contribution from the interface trap states is usually assumed to be negligible, the oxide capacitance can then be determined as [52,54]:

$$C_{ox} = C_m \cdot \left[1 + \left(\frac{G_m}{\omega \cdot C_m} \right)^2 \right] \quad (4.40)$$

Consequently, the oxide capacitance C_{ox} was determined from equation (4.40) using the measured capacitance and conductance C_m and G_m at 1 MHz, for every applied bias voltage. These calculated values of C_{ox} were thus injected in equation (4.39) to determine the normalized parallel conductance. Subsequently, the normalized parallel conductance is plotted as a function of the frequency. The resulting curves obtained for the different experimental parameters (i.e. applied bias voltage, ZnO deposition temperature) are shown in Fig. 4.37. These plots exhibit a peak, linked with the

presence of interface trap states at the Pt/ZnO junction, whose maximum value depends on the time constant of the interface trap states. The variation of the normalized parallel conductance as a function of the frequency can be understood in terms of energy loss, considering a continuous distribution of energy states at the Fermi level. This energy loss occurs when the interface trap states capture and emission time constants are different or phase shifted from the applied AC period variation at the surface Fermi level [56]. More precisely, for low frequencies values (i.e. between 20 Hz and ~ 10 kHz in this work), the interface trap states are able to follow the AC signal frequency and subsequently change their occupancy in response to the surface Fermi level variations, in such a way that no energy loss occurs. At higher frequencies (i.e. > 1 MHz in this work, not represented on the experimental curves), the interface trap states cannot follow the AC signal frequency and the resulting Fermi level variations, so that no energy loss occurs. However, for an intermediate range of frequencies (i.e. for frequencies located around 1 MHz in this work), the AC signal period is different or phase shifted from the interface trap states time constant. This leads to energy losses as electrons transition from higher to lower energy states at the surface Fermi level, which corresponds concomitantly with the appearance of the peak in the normalized parallel conductance plotted as a function of the frequency.

At the peak location, the first derivative of equation (4.38) is zero (i.e. $\frac{\partial(\frac{G_p}{\omega})}{\partial(\omega \cdot \tau)} = 0$). This relation numerically yields $\omega_{\max} \cdot \tau \approx 1.98$, used to further determine the interface trap states time constant with the maximum angular frequency value at the peak location ω_{\max} , as:

$$\tau = \frac{1.98}{\omega_{\max}} \quad (4.41)$$

Furthermore, the relation $\omega_{\max} \cdot \tau \approx 1.98$ can be substituted in equation (4.38) to determine the density of interface trap states D_{it} at the peak location, using the maximum value of the normalized parallel conductance $\frac{G_p}{\omega_{\max}}$, as:

$$D_{it} \approx \frac{G_p}{\omega_{max}} \cdot \frac{1}{0.402 \cdot A \cdot q} \quad (4.42)$$

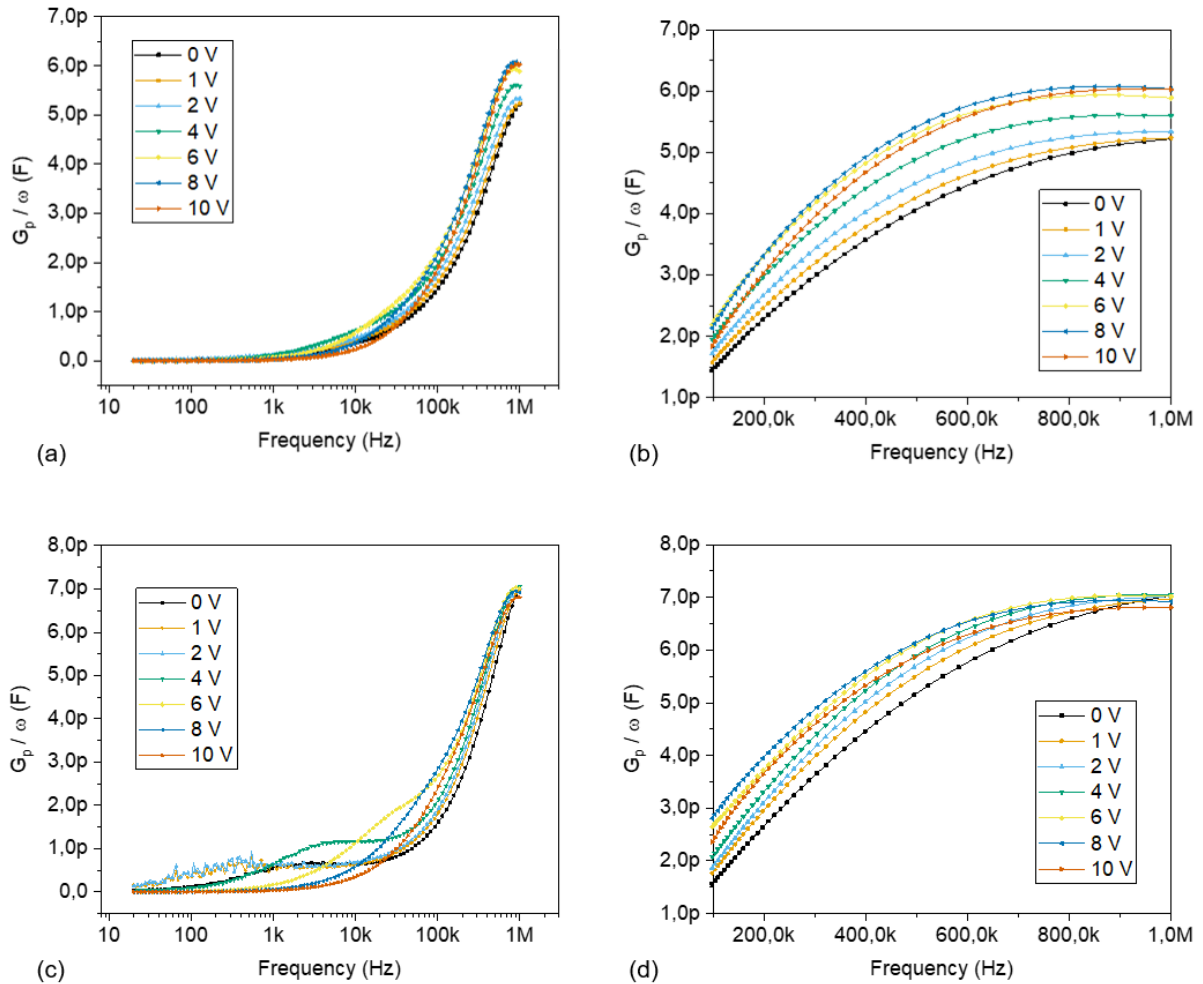


Figure 4.37. (a) Normalized parallel conductance as a function of the frequency (semi-log scale), for the different applied bias voltages between 0 V and 10 V, as well as for a ZnO thin film deposited at 80 °C; (b) Enclosed view of graph (a) between frequency values of 100 kHz and 1 MHz (linear scale). (c) Normalized parallel conductance as a function of the frequency (semi-log scale), for the different applied bias voltages between 0 V and 10 V, as well as for a ZnO thin film deposited at 60 °C; (d) Enclosed view of graph (c) between frequency values of 100 kHz and 1 MHz (linear scale).

As observed from Fig. 4.37, the peak position appears to be located at frequencies values on the vicinity of 1 MHz. However, the performed measurements were limited experimentally to the threshold frequency value of 1 MHz and could thus not be extended to higher frequencies to observe the downward slopes of the peaks. Consequently, the calculated values of τ and D_{it} will be given relative to the maximum

value of the normalized parallel conductance at 1 MHz in the case where $\frac{G_p}{\omega_{\max}}$ is located in the upward slope of the peak. The corresponding values of τ and D_{it} are summarized in Table 4.3 as a function of the different experimental conditions in study.

Bias voltage V [V]	ZnO deposition temperature 80 °C		ZnO deposition temperature 60 °C	
	D_{it} [$10^{12} \text{ eV}^{-1} \cdot \text{cm}^{-2}$]	τ [10^{-7} s]	D_{it} [$10^{12} \text{ eV}^{-1} \cdot \text{cm}^{-2}$]	τ [10^{-7} s]
0	> 3.61	< 3.15	> 4.87	< 3.15
1	> 3.62	< 3.15	> 4.83	< 3.15
2	> 3.70	< 3.15	> 4.86	< 3.15
4	3.88	3.51	> 4.89	< 3.15
6	4.11	3.71	4.87	3.51
8	4.21	3.51	4.81	3.51
10	4.18	3.32	> 4.71	< 3.15

Table 4.3. Calculated values of D_{it} and τ for ZnO thin films deposited by ALD at 80 °C and 60 °C, with bias voltage values ranging between 0 V and 10 V.

The obtained values for the density of interface trap states D_{it} are located in the $10^{12} \text{ eV}^{-1} \cdot \text{cm}^{-2}$ range, while the interface trap states time constant τ takes values in the 10^{-7} s range. For the ZnO thin film deposited at 80 °C, the peak position appears to be slightly shifted to lower frequencies as the bias voltage is increased, leading to an increase of both D_{it} and τ at higher bias voltage values. However, the peak position for the ZnO thin film deposited at 60 °C appears to be relatively constant with the applied bias voltage, yielding no significant change in D_{it} and τ . Both the density and the time constant of interface trap states are highly dependent upon the nature, the deposition method and the morphology of the semiconductor and the metal at the Schottky junction. However, to the best of our knowledge, there is no similar report making use of the conductance method to determine D_{it} and τ between ALD-grown ZnO thin film and Pt metal electrodes.

Nonetheless, the obtained interface trap states time constant value is typically lower by one or two orders of magnitude when compared to other works using the conductance method at M-S or M-I-S junctions [44,53,54,57]. This discrepancy could be explained by the presence of the interdiffusion area at the Pt/ZnO junctions, substituting the oxide layer in the conductance method. As stated previously, this interdiffusion area may increase the defects and interface states density at the Schottky interface, thus facilitating the transport of electrons at the M-S junction when compared to a thick oxide insulating layer. Furthermore, a lower time constant signifies that the interface trap states present a quicker time response and are thus able to follow higher AC signal frequencies up to 1 MHz. Consequently, the contribution of interface trap states in the obtained capacitance characteristics is effectively substantially reduced at higher frequencies (> 500 kHz) but should not be rigorously neglected. Moreover, as stated previously, the obtained experimental capacitance values at high frequencies are effectively converging towards a range of values within a few picoFarads, corresponding to the Schottky depletion region C_S . However, as illustrated in Fig. 4.33, the Schottky depletion capacitance alone is characterized by a decrease of the capacitance for increasing bias voltage values, while in Fig. 4.34 and Fig. 4.35 the experimental capacitance values are slightly increasing for higher applied bias voltages. This further demonstrates the presence of an excess capacitance due to interface trap states at high frequencies, linked with their low time constant. Consequently, this excess interface trap states capacitance at 1 MHz might lead to a minor deviation in the calculated oxide capacitance C_{ox} with equation (4.40), which in turn generates an error in the extraction of D_{it} and τ . Therefore, measurements at frequencies superior to 1 MHz should be performed for better accuracy in the determination of the density and the time constant of the interface trap states.

Besides, another hypothesis might be considered, linked with the presence of broader peaks located between 100 Hz and 100 kHz in Fig. 4.37 and associated with interface trap defects. However, the presence of these peaks is not obvious at all in Fig. 4.37(a), for the ZnO thin film deposited at 80 °C. The following analysis will thus be performed based on measurements from Fig. 4.37(c), for the ZnO thin film deposited at 60 °C, where these broader peaks can be more easily distinguished. These peaks are further

highlighted in Fig. 4.38, where the normalized parallel conductance is represented as function of the frequency for applied bias voltages ranging between 0 V and 10 V.

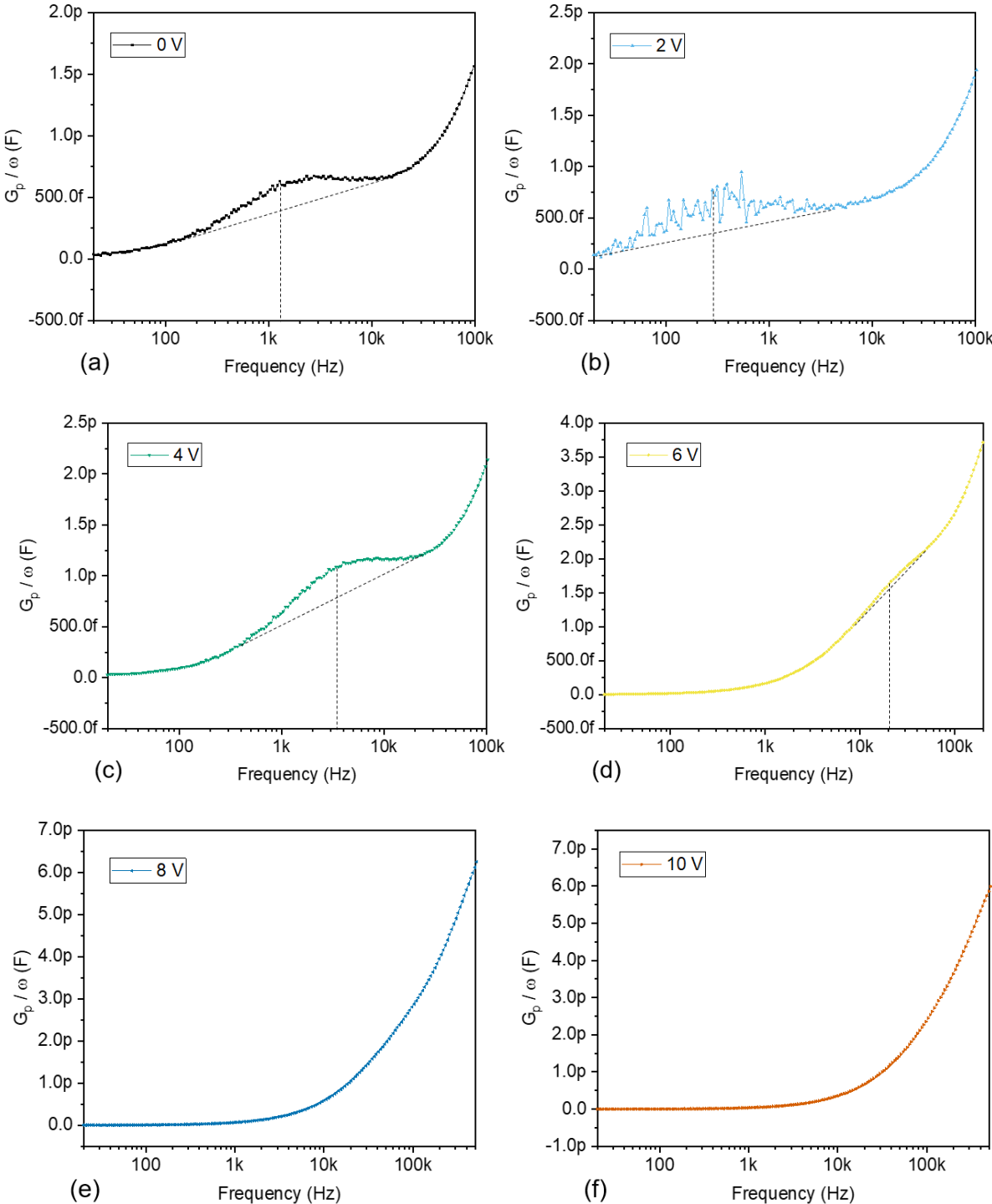


Figure 4.38. Normalized parallel conductance as a function of the frequency (semi-log scale), for a ZnO thin film deposited at 60 °C, as well as for an applied bias voltage of (a) 0 V, (b) 2 V, (c) 4V, (d) 6 V, (e) 8 V and (f) 10 V. The approximate peak position is highlighted with a vertical black dashed line.

The peaks can be easily distinguished in Fig. 4.38(a), Fig. 4.38(b) and Fig. 4.38(c), corresponding to applied bias voltages of 0 V, 2 V and 4 V, respectively. However, as the bias voltage is increased to 6 V, the peak can only be barely observed (see Fig. 4.38(d)) and is not visible at all for applied bias voltages of 8 V and 10 V (see Fig. 4.38(e) and Fig. 4.38(f), respectively). As observed from the previous peaks at 4 V and 6 V, their respective positions seem to be shifted to higher frequencies values as the applied bias voltage is increased. Based on these considerations, it could thus be stated that the peak position for applied bias voltages of 8 V and 10 V would be located at frequencies higher than 20 kHz. However, the increase of the normalized parallel conductance associated with these broader peaks might be too small compared with the peak located at 1 MHz, in such a way that their impact cannot be visually assessed. Consequently, their position will be determined relative to the last peak position for an applied bias voltage of 6 V. The approximate peak positions were thus determined from Fig. 4.38 for a qualitative analysis and the corresponding evolution of the peak position as a function of the applied bias voltage. The interface trap states time constant τ , associated with these broader peaks, was subsequently calculated based on equation (4.41). The corresponding results are reported in Table 4.4:

Bias voltage V [V]	ZnO deposition temperature 60 °C	
	τ [s]	
0	2.44×10^{-4}	
2	1.11×10^{-3}	
4	9.16×10^{-5}	
6	1.53×10^{-5}	
8	$< 1.53 \times 10^{-5}$	
10	$< 1.53 \times 10^{-5}$	

Table 4.4. Calculated values of τ for ZnO thin films deposited by ALD at 60 °C, with bias voltage values ranging between 0 V and 10 V.

As observed from Table 4.4, the interface trap states time constant τ is increased from $\sim 2.44 \times 10^{-4}$ s to $\sim 1.11 \times 10^{-3}$ s as the applied bias voltage is increased from 0 V to 2 V. However, the interface trap states time constant is subsequently reduced to $\sim 9.16 \times 10^{-5}$ s and $\sim 1.53 \times 10^{-5}$ s as the bias voltage is increased to 4 V and 6 V, respectively. Finally, as the applied bias voltage is increased to 8 V and 10 V, the interface trap states time constant is expected to be further decreased to values inferior to $\sim 1.53 \times 10^{-5}$ s. The overall trend indicates that the interface trap states time constant τ is decreased as the applied bias voltage is increased, thus clearly highlighting its voltage-dependence.

The conductance method effectively allows to differentiate bulk and interface trap states, based on their voltage-dependence. On the one hand, the presence of multiple peaks in the $\frac{G_p}{\omega}$ characteristics, shifting to higher frequencies for increased applied bias voltages, is typical of interface trap states with continuous energy levels [58,59]. On the other hand, bulk trap states are commonly observed at discrete energy levels, leading to a similar peak loss located at the same frequency for different applied bias voltages [58]. Based on these considerations, it could thus be stated that the peak observed at the vicinity of 1 MHz could be linked with either the series resistance of the semiconductor, or with bulk trap states located at a single discrete energy level. Concomitantly, the broader peaks observed within the $\frac{G_p}{\omega}$ characteristics shall be attributed to the presence of interface trap states distributed with continuous energy levels, where the peak position and the resulting interface trap states time constant depend on the depth of these interface trap states [58,59]. The capture/re-emission processes of interface trap states would thus be more pronounced for the ALD-grown ZnO thin films at 60 °C compared to the one at 80 °C, which would explain why this phenomenon could only be observed at 60 °C.

Furthermore, it is noteworthy that the bias voltage values reported in this analysis (from 0 V to 10 V) should be balanced by the voltage drops V_1 and V_2 at each junction for a better understanding of these interface phenomena. This further demonstrates the need of a numerical method to determine V_1 and V_2 at the reverse and forward biased Schottky diodes, in order to assess their respective contribution on the electrical characteristics of the Pt/ZnO/Pt junctions.

4.2.2.6. Experimental (I-V) characteristics of the Pt/ZnO/Pt Schottky junctions

The (I-V) characteristics of the Pt/ZnO/Pt Schottky junctions were measured with DC bias modulation under dark conditions, for ZnO thin films grown by ALD at 80 °C and 60 °C. The voltage was linearly swept with forward and backward sweeps between -10 V and 10 V, using a step voltage of 100 mV. The current measurements were performed with an integration time of 200 ms, a step length of 100 mV, a sweep speed of 200 mV.s⁻¹ and a delay of 300 ms between the step and the measurement. The obtained (I-V) curves are presented in Fig. 4.39. The hysteresis between the forward and backward sweep observed in the (I-V) curves is linked to the filling of the interface trap states at the M-S junctions. Indeed, during the forward sweep (i.e. from zero bias to a higher bias voltage), the interface trap states are gradually filled up as the current and the bias voltage are increased. However, during the backward sweep (i.e. from a high bias voltage to zero bias), the initial high bias voltage is directly filling up the interface trap states. Some of these trap states remained filled up during the rest of the backward sweep to 0 V, which led to a lower density of interface trap states actively involved in the current conduction mechanism, thus reducing the current in the devices. This is linked to the different capture and re-emission charge carriers' dynamics at the M-S junctions, resulting in the hysteresis observed in the (I-V) curves. The subsequent fitting of the (I-V) characteristics will be performed on the curves displayed in Fig. 4.39.

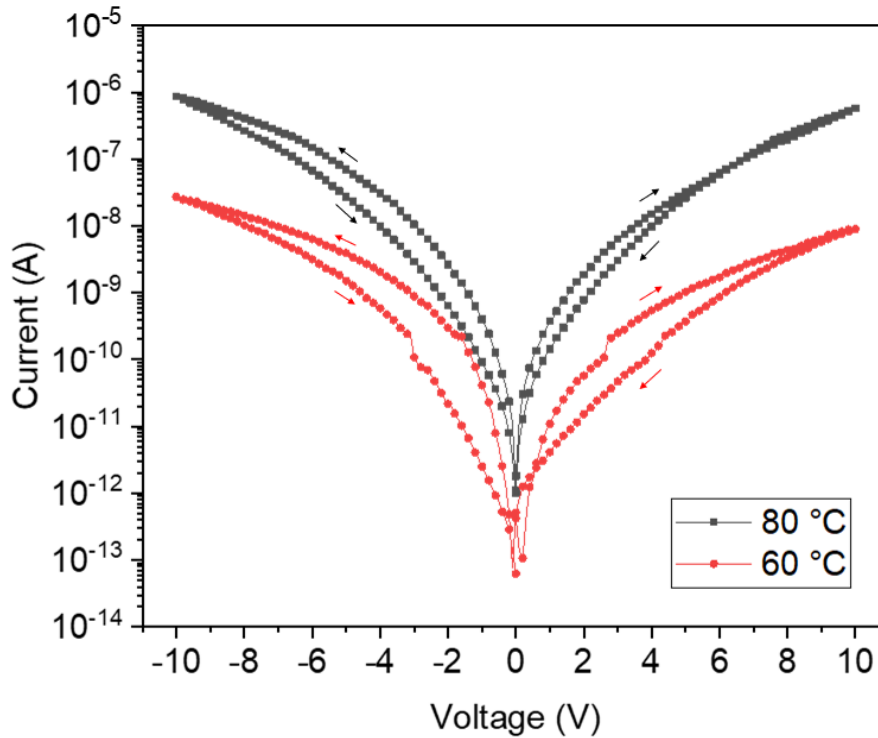


Figure 4.39. (I-V) characteristics of Pt/ZnO/Pt Schottky junctions measured with DC bias modulation under dark conditions, for ZnO thin films grown by ALD at 80 °C and 60 °C. The current is represented on a logarithmic scale with absolute values. The current measurements were performed with an integration time of 200 ms, a step length of 100 mV, a sweep speed of 200 mV.s⁻¹ and a delay of 300 ms between the step and the measurement. The voltage was swept for dark characteristics between -10 V and 10 V, with a step voltage of 100 mV. The arrows indicate the parts of the curves corresponding to the forward and backward sweeps.

4.2.2.7. Impact of the series resistance

As detailed within the previous section, the series resistance R_S shall not be always considered as negligible, as the product of the electrical current I with R_S leads to a voltage drop V_{ZnO} occurring in the bulk of the ZnO thin film. The series resistance is particularly important in forward biased Schottky junctions, where high current values occur even at low bias voltages due to the direct exponential dependence of the (I-V) characteristics. Therefore, depending on the series resistance value, the product of I with R_S might lead to a significant voltage drop V_{ZnO} compared with the applied bias voltage V , resulting in a deviation of the (I-V) characteristics. However, as observed from Fig. 4.39, due to the reverse biased Schottky junction with the back-to-back configuration of two diodes, our system consists of low current values, typically extending from ~ 1 pA at 0 V to ~ 1 μ A at 10 V for the ALD-grown ZnO thin film at

80 °C. When comparing with the ALD-grown ZnO thin film at 60 °C, the current values are typically decreased by one up to two orders of magnitude. Therefore, a higher series resistance is needed for the voltage drop V_{ZnO} to be appreciable compared with the applied bias voltage. Nonetheless, a quantitative estimation of the series resistance value shall be performed to rigorously determine whether its impact shall be taken into account in the electrical model or neglected.

Within this scope, the series resistance at 0 V was determined further in this chapter by the mean of noise analysis, as detailed within section 4.3.3. The corresponding series resistance R_S values at 0 V were obtained as 161.8 k Ω at 60 °C and 92.6 k Ω at 80 °C, respectively. Consequently, the voltage drop V_{ZnO} occurring in the bulk of the ZnO thin film can be calculated by matching the determined series resistance from noise analysis with the experimental current values (shown in Fig. 4.39) as a function of the applied bias voltage, following the equation:

$$V_{ZnO} = R_S \cdot I_{exp} \quad (4.43)$$

It should be noted that the voltage dependence of the series resistance R_S as a function of the applied bias voltage was not considered in this analysis. The obtained voltage drops V_{ZnO} as a function of the applied bias voltage for the ZnO thin film deposited at 80 °C and 60 °C are represented in Fig. 4.40.

The voltage drop V_{ZnO} remains negligible for low applied bias voltages but quickly increases as the bias voltage is increased up to 10 V. More precisely, the voltage drop V_{ZnO} reaches a maximum value of ~ 80 mV for an applied bias voltage of 10 V, corresponding to the ZnO thin film deposited at 80 °C. Correspondingly, the voltage drop V_{ZnO} reaches a maximum value of ~ 4 mV for an applied bias voltage of 10 V, corresponding to the ZnO thin film deposited at 60 °C. Based on these considerations, the voltage drop due to the series resistance is not significant when compared to the applied bias voltage on the studied range and can thus be neglected in the subsequent fitting of the experimental (I-V) characteristics. Nonetheless, this analysis indicates that increasing the bias voltage to values superior to 10 V would most likely result in a significant voltage drop V_{ZnO} which should be accounted for.

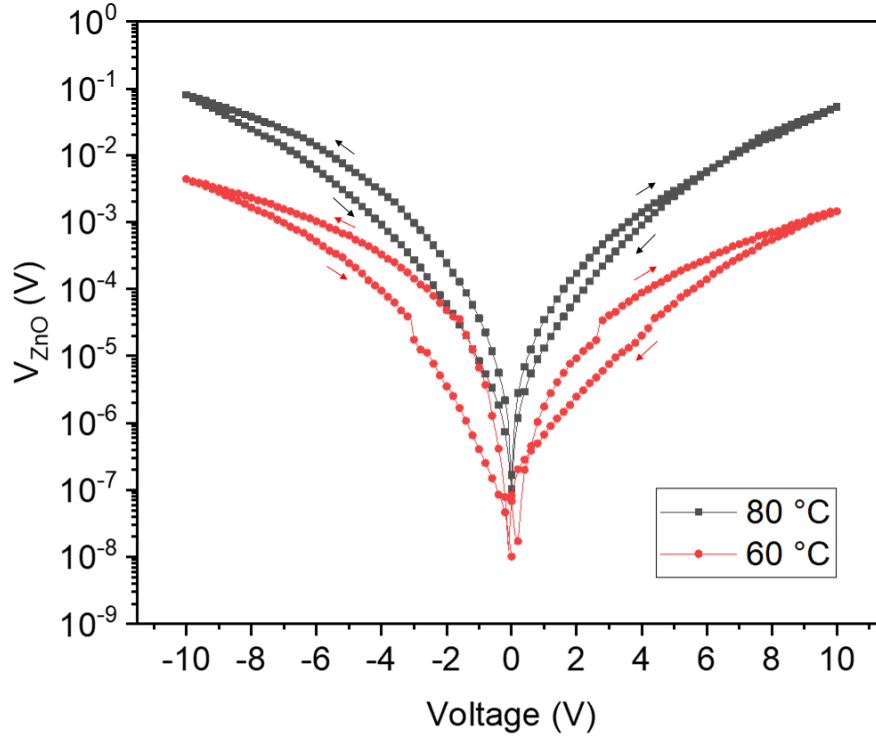


Figure 4.40. Voltage drop V_{ZnO} as a function of the applied bias voltage for the ZnO thin film deposited at 80 °C and 60 °C, calculated by matching the determined series resistance from noise analysis with the experimental current values. The arrows indicate the parts of the curves corresponding to the forward and backward sweep.

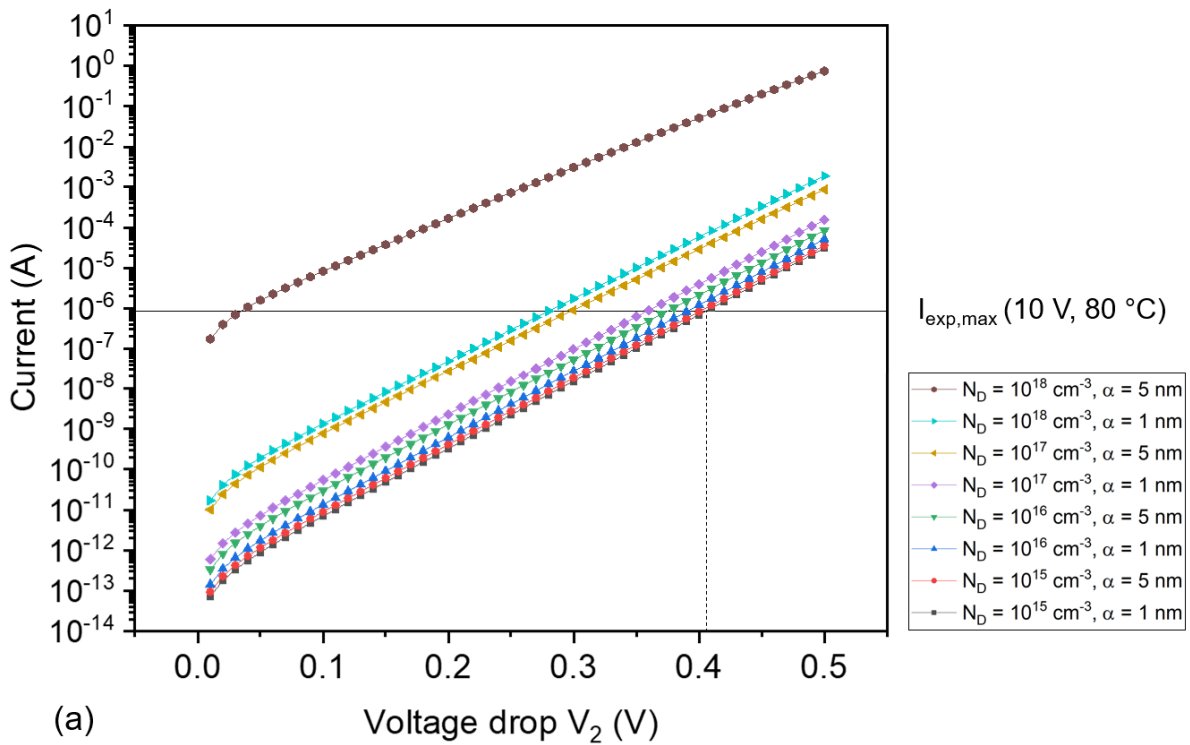
4.2.2.8. Impact of the voltage drop V_2 at the forward biased Schottky junction

Before proceeding to the fitting of the experimental (I-V) characteristics, it is paramount to estimate the magnitude of the voltage drop V_2 at the forward biased Schottky junction, in order to provide appropriate boundaries values during the extraction of this parameter via the numerical method. As described previously in equation (4.23), the (I-V) characteristics through the forward biased Schottky junction are given by:

$$I_2 = A \cdot A^* \cdot T^2 \cdot \exp\left(-\frac{q \cdot \Phi_B}{k_B \cdot T}\right) \cdot \exp\left(\frac{q \cdot (\Delta\Phi_{B2} + \Delta\Phi_{B2}')}{k_B \cdot T}\right) \cdot \left[\exp\left(\frac{q \cdot V_2}{k_B \cdot T}\right) - 1\right]$$

As the electron concentration N_D and the intrinsic barrier lowering coefficient α remain unknown, their respective values were set between minimum and maximum boundary conditions. More precisely, based on the values reported within chapter 3 for low ALD deposition temperatures, N_D was varied between 10^{15} cm^{-3} and 10^{18} cm^{-3} with an

increment of one order of magnitude, while α was set as a minimum of 1 nm and a maximum of 5 nm, based on reported values in the literature [21,38]. The simulated set of curves describing the current through the forward biased Schottky junction was thus calculated via equation (4.23), using bias voltage values ranging between 0 V and 0.5 V, which can be physically interpreted as the voltage drop V_2 . Nonetheless, it should be noted that the current within the simulated set of curves correspond to a single forward biased Schottky junction. When integrated within a back-to-back diode configuration, due to the current continuity requirement, the current through the forward biased Schottky junction is matched to the experimental current through the reverse biased junction by adjusting the value of V_2 . The corresponding simulated (I-V) characteristics are presented in Fig. 4.41(a) and Fig. 4.41(b), for ALD deposition temperatures of 80 °C and 60 °C, respectively.



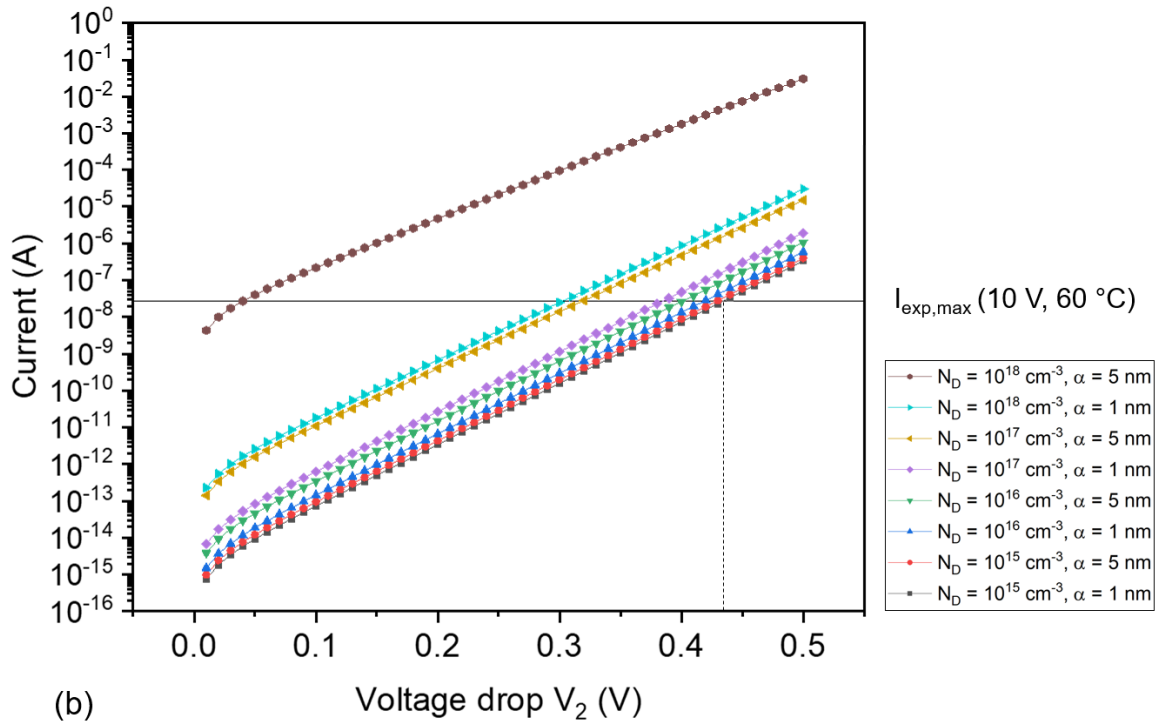


Figure 4.41. Current curves simulated analytically through the forward biased Schottky junction, as a function of the voltage drop V_2 , for the ZnO thin film deposited at (a) 80 °C and (b) 60 °C. N_D was varied between 10^{15} cm^{-3} and 10^{18} cm^{-3} with an increment of one order of magnitude, while α was set as a minimum of 1 nm and a maximum of 5 nm. The maximum experimental current reached at 10 V, for an ALD deposition temperature of 80 °C and 60 °C (i.e. $I_{\text{exp,max}}(10 \text{ V}, 80 \text{ °C})$ and $I_{\text{exp,max}}(10 \text{ V}, 60 \text{ °C})$, respectively) are indicated by the straight horizontal lines.

Therefore, the simulated set of curves was compared with the maximum experimental current reached at 10 V, for an ALD deposition temperature of 80 °C and 60 °C (i.e. $I_{\text{exp,max}}(10 \text{ V}, 80 \text{ °C})$ and $I_{\text{exp,max}}(10 \text{ V}, 60 \text{ °C})$, respectively). The intercept of these straight lines with the simulated curves thus graphically yields an estimation of the voltage drop V_2 at 10 V on the horizontal axis, for given values of N_D and α . Consequently, by considering both minimum boundary values for N_D and α (i.e. 10^{15} cm^{-3} and 1 nm, respectively), the maximum value of the voltage drop V_2 at the forward biased Schottky junction can be estimated graphically at $\sim 0.405 \text{ V}$ for and ALD deposition temperature of 80 °C, and at $\sim 0.434 \text{ V}$ for and ALD deposition temperature of 60 °C. By considering the experimental applied bias voltage V ranging between 0 V and 10 V, we can therefore reasonably estimate that the voltage drop V_2 is taking values continuously distributed between 0 V and $\sim 0.405 \text{ V}$ for and ALD deposition temperature of 80 °C. Similarly, V_2 is continuously distributed between 0 V and $\sim 0.434 \text{ V}$ for and ALD deposition temperature of 60 °C.

4.2.2.9. Fitting of the experimental (I-V) characteristics

As mentioned previously, a numerical solution was implemented by the mean of a non-linear curve fitting, based on an Orthogonal Distance Regression iteration algorithm via the software Origin. This fitting method is well suited for (I-V) characteristics with strongly varying slopes [60]. The conduction mechanism being dictated by the reverse biased Schottky junction, the experimental (I-V) characteristics presented in Fig. 4.39 were fitted using equation (4.22), as:

$$I_{\text{exp}} = A \cdot A^* \cdot T^2 \cdot \exp\left(-\frac{q \cdot \Phi_B}{k_B \cdot T}\right) \cdot \exp\left(\frac{q \cdot (\Delta\Phi_{B1} + \Delta\Phi_{B1}')}{k_B \cdot T}\right) \cdot \left[1 - \exp\left(-\frac{q \cdot V_1}{k_B \cdot T}\right)\right]$$

Where:

$$\Phi_B = \Phi_B^{\text{eff}} + \left[\frac{q^3 \cdot N_D}{8 \cdot \pi^2 \cdot \epsilon_s^3} \cdot V_D\right]^{1/4} + \alpha \cdot \sqrt{\frac{2 \cdot q \cdot N_D}{\epsilon_s} \cdot V_D}$$

$$\Delta\Phi_{B1} = \sqrt{\frac{q \cdot E_{m1}}{4 \cdot \pi \cdot \epsilon_s}}$$

$$\Delta\Phi_{B1}' \approx \alpha \cdot E_{m1}$$

$$E_{m1} = \sqrt{\frac{2 \cdot q \cdot N_D}{\epsilon_s} \cdot (V_1 + V_D)}$$

$$V_D = \Phi_B^{\text{eff}} - \left[\frac{k_B \cdot T}{q} \cdot \ln\left(\frac{N_C}{N_D}\right)\right]$$

The number of unknown variables within the electrical model was successfully reduced via the determination/estimation of the Schottky contact area A , the Schottky barrier height Φ_B , as well as the expression of the built-in voltage V_D as a function of Φ_B^{eff} and

the electron concentration N_D . The impact of the interface trap states was clearly demonstrated by a careful investigation of the Pt/ZnO interface and the determination of their density and time constant. As indicated by J. M. Andrews et al. [38], the impact of the interface trap states in the (I-V) characteristics can be integrated into the intrinsic barrier lowering coefficient α , whose magnitude depends upon the density of interface trap states. Moreover, the impact of the series resistance R_S and its resulting voltage drop V_{ZnO} occurring in the bulk of the ZnO thin film was considered as negligible. As only the total experimentally applied bias voltage V is known as an input voltage parameter, the voltage drop V_1 through the reverse biased Schottky junction was thus expressed as $V_1 = V - V_2$. It should be noted that the forward voltage drop V_2 is interpreted as a constant. However, a bias-dependent distribution of V_2 should be considered for a better fitting accuracy, which will be discussed in the following analysis.

Consequently, three parameters remain unknown within the developed electrical model, i.e. the electron concentration N_D , the intrinsic barrier lowering coefficient α and the voltage drop through the forward biased Schottky junction V_2 . Boundary values were set for each parameter in order to facilitate the subsequent non-linear curve fitting of the experimental (I-V) characteristics. These boundary values are summarized in Table 4.5.

Parameter	Lower boundary	Upper boundary
N_D [cm^{-3}]	10^{15} cm^{-3}	10^{18} cm^{-3}
α [nm]	1 nm	5 nm
$V_2^{80^\circ\text{C}}$ [V]	0 V	0.405 V
$V_2^{60^\circ\text{C}}$ [V]	0 V	0.434 V

Table 4.5. Boundary values for each unknown parameter determined through the non-linear curve fitting of the experimental (I-V) characteristics.

As the experimental (I-V) characteristics are symmetrical, the fitting was thus realized in the range of applied bias voltage from 0 V to ± 10 V. Nonetheless, as observed from Fig. 4.39, the forward (from 0 V to ± 10 V) and backward (from ± 10 V to 0 V) sweeps have a substantial impact on the electrical behaviour, they were consequently fitted

separately to better assess their respective impact on the electrical parameters. The performed fittings of the experimental (I-V) characteristics for an ALD deposition temperature of 80 °C, with the associated values and errors of the electrical parameters corresponding to the forward and backward sweeps are presented in Fig. 4.42(a) and Fig. 4.42(b), respectively.

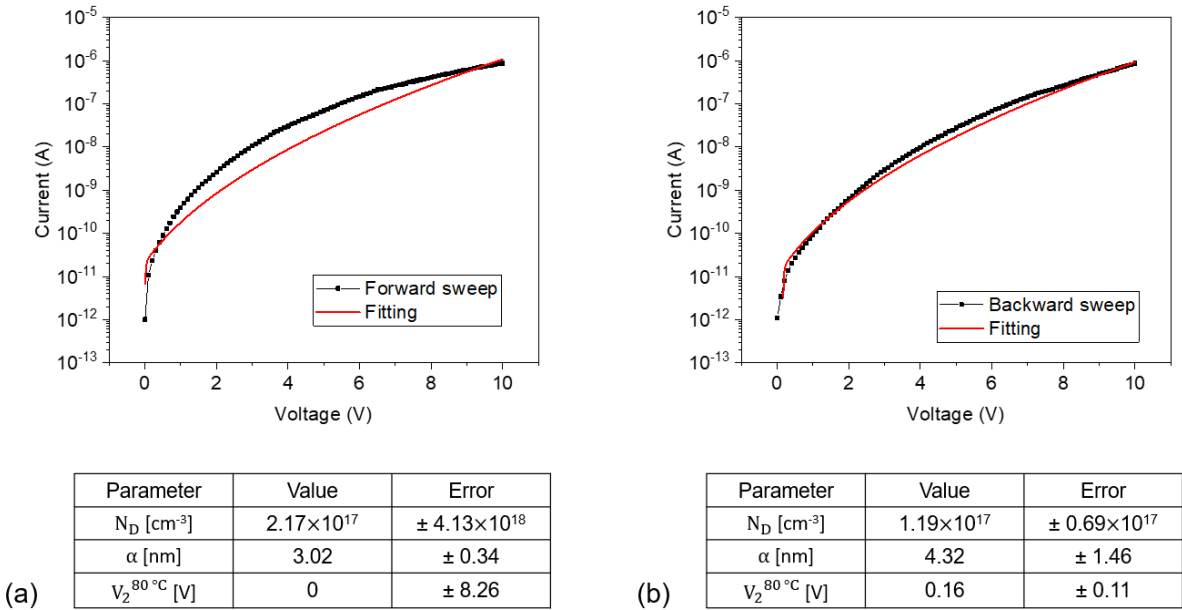
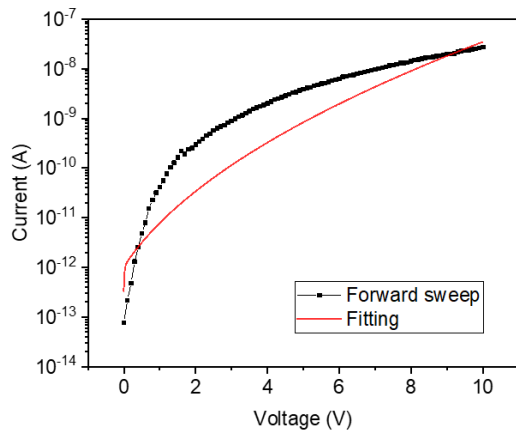


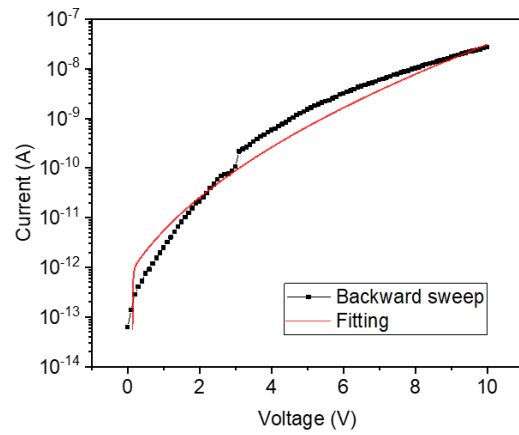
Figure 4.42. Non-linear curve fitting of the experimental (I-V) characteristics for an ALD deposition temperature of 80 °C, with the associated values and errors of the electrical parameters corresponding to (a) the forward and (b) backward sweeps.

A similar methodology was adopted for the non-linear fitting of the (I-V) curves at a deposition temperature of 60 °C. The performed fittings of the experimental (I-V) characteristics for an ALD deposition temperature of 60 °C, with the associated values and errors of the electrical parameters corresponding to the forward and backward sweeps are presented in Fig. 4.43(a) and Fig. 4.43(b), respectively.



Parameter	Value	Error
N_D [cm^{-3}]	1.05×10^{17}	$\pm 2.29 \times 10^{18}$
α [nm]	4.38	± 0.54
$V_2^{60^\circ\text{C}}$ [V]	0	± 9.51

(a)



Parameter	Value	Error
N_D [cm^{-3}]	7.49×10^{16}	$\pm 8.73 \times 10^{16}$
α [nm]	4.86	± 3.58
$V_2^{60^\circ\text{C}}$ [V]	0.15	± 0.21

(b)

Figure 4.43. Non-linear curve fitting of the experimental (I-V) characteristics for an ALD deposition temperature of 60°C , with the associated values and errors of the electrical parameters corresponding to (a) the forward and (b) backward sweeps.

Several information can be extracted from these results. On the one hand, the algorithm's convergence was not achieved within the fitting of the forward sweeps of the experimental (I-V) curves (see Fig. 4.42(a) and Fig. 4.43(a)), which explains the large reported error values. On the other hand, the algorithm was able to achieve convergence within the backward sweeps (see Fig. 4.42(b) and Fig. 4.43(b)), resulting in a more accurate fitting of the experimental (I-V) characteristics. Reportedly, based on the fitting obtained within the backward sweep, the electron concentration N_D was determined as $1.19 \times 10^{17} \pm 0.69 \times 10^{17} \text{ cm}^{-3}$, while the intrinsic barrier lowering coefficient α was determined as $4.32 \pm 1.46 \text{ nm}$, with a corresponding forward voltage drop V_2 of $0.16 \pm 0.11 \text{ V}$ at a deposition temperature of 80°C . Similarly, the electron concentration N_D was determined as $7.49 \times 10^{16} \pm 8.73 \times 10^{16} \text{ cm}^{-3}$, while the intrinsic barrier lowering coefficient α was determined as $4.86 \pm 3.58 \text{ nm}$, with a corresponding forward voltage drop V_2 of $0.15 \pm 0.21 \text{ V}$ at a deposition temperature of 60°C . The reported error values of N_D , α and V_2 in Fig. 4.43(b), obtained for ALD-grown ZnO thin films at 60°C , are substantially higher than those reported in Fig. 4.42(b) at a deposition temperature of 80°C . This is linked with the lower experimental current values at a deposition temperature of 60°C being more sensitive to instrumentation

noises, leading to local fluctuations in the measured current values when compared to the ideal electrical model.

These extracted values were used within the algorithm and set as constants to compare the resulting fitting with the experimental curves on the entire bias voltage range, including both forward and backward sweeps, as depicted in Fig. 4.44.

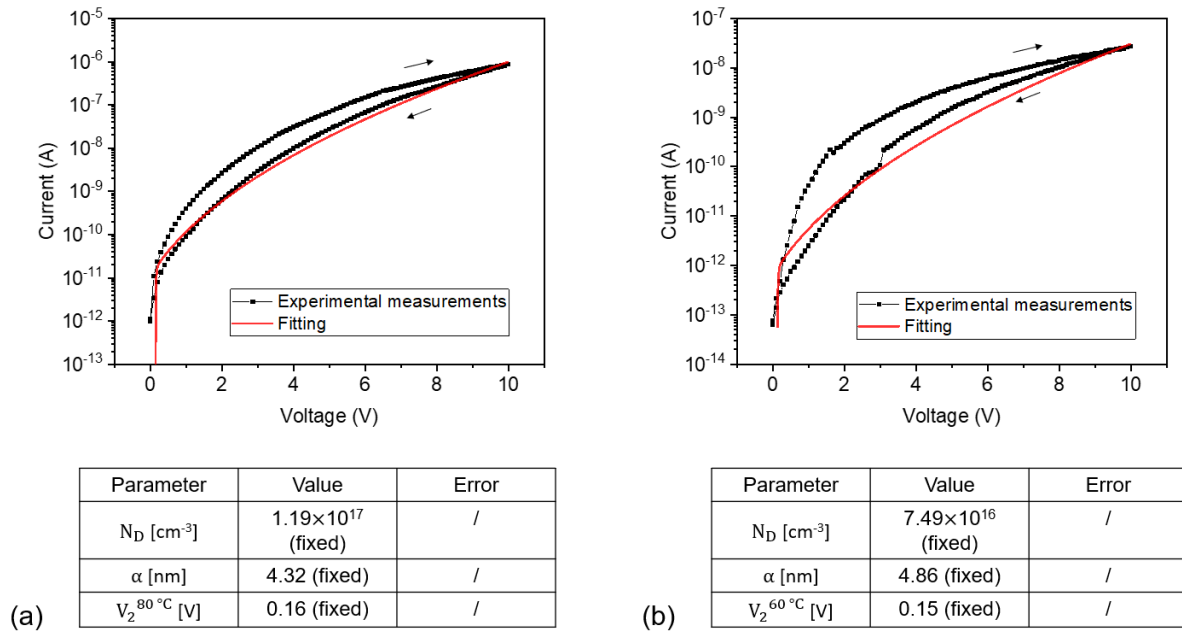


Figure 4.44. Non-linear curve fitting of the experimental (I - V) characteristics on the whole bias voltage range, using fixed parameters' values determined within the backward sweep, for the ZnO thin film deposited at (a) 80 °C and (b) 60 °C. The arrows indicate the parts of the curves corresponding to the forward and backward sweeps.

As detailed previously, the observed hysteresis between the forward and backward sweeps is associated with the bias-dependent occupancy of the interface trap states at the Pt/ZnO Schottky junctions, linked to the different capture and re-emission charge carriers' dynamics at the MS junctions. This discrepancy between the forward and backward sweeps could thus be understood by considering a bias-dependent density of interface trap states involved in the conduction mechanism, which could be taken into account within the parameter α . Based on this explanation, during the forward sweep, the interface states would be initially empty at 0 V, meaning that a higher density of interface trap states is available for the electrons to be involved within the charge transport mechanism at the Pt/ZnO interface. As the current and the applied bias voltage are increased, the interface states are gradually filled up by electrons remaining trapped at the interface, concomitantly resulting in a decrease of the density

of interface trap states involved in the charge transport mechanism. This leads to a gradual decrease of α as the applied bias voltage is increased, which could explain the change in the inflection of the experimental (I-V) curves in the forward sweep. Nonetheless, as the backward sweep is initiated at 10 V, a given density of interface trap states remained filled up by electrons as the applied bias voltage is decreased to 0 V. This results in a less significant variation of α within the backward sweep of the experimental (I-V) curves, which could explain the better fitting obtained.

Furthermore, the total applied bias voltage V is distributed between the voltage drops V_1 and V_2 at the reverse and forward biased Schottky junctions. The value of the forward voltage drop V_2 determined by the fitting algorithm is averaged on the entire bias voltage range between 0 V and 10 V. However, for low values of V , the magnitude of the forward voltage drop V_2 is significant compared to the reverse voltage drop V_1 , yielding an error in the input voltage supplied within the electrical model. Additionally, as the applied bias voltage V is increased, the magnitude of the voltage drop V_1 becomes increasingly important compared to V_2 . The impact and the variation of the forward voltage drop V_2 is thus less and less significant as the applied bias voltage V is increased. A bias-dependent distribution of the voltage drop V_2 should thus be considered for a better fitting accuracy, especially at low bias voltage.

The electrical parameters determined by non-linear fitting within the backward sweep of the experimental (I-V) characteristics, for ALD deposition temperatures of 80 °C and 60 °C (displayed in Fig. 4.42(b) and Fig. 4.43(b), respectively) are further reported in Table 4.6.

ZnO thin film deposition temperature [° C]	N_D [cm ⁻³]	α [nm]	V_2 [V]
80	$1.19 \times 10^{17} \pm 0.69 \times 10^{17}$	4.32 ± 1.46	0.16 ± 0.11
60	$7.49 \times 10^{16} \pm 8.73 \times 10^{16}$	4.86 ± 3.58	0.15 ± 0.21

Table 4.6. Electrical parameters determined by non-linear fitting within the backward sweep of the experimental (I-V) characteristics, for ALD deposition temperatures of 80 °C and 60 °C.

As observed from Table 4.6, the electron concentration determined from the non-linear curve fittings is decreased from $1.19 \times 10^{17} \pm 0.69 \times 10^{17} \text{ cm}^{-3}$ to $7.49 \times 10^{16} \pm 8.73 \times 10^{16} \text{ cm}^{-3}$, while the intrinsic barrier lowering coefficient α is increased from $4.32 \pm 1.46 \text{ nm}$ to $4.86 \pm 3.58 \text{ nm}$, when the deposition temperature is decreased from $80 \text{ }^\circ\text{C}$ to $60 \text{ }^\circ\text{C}$, respectively. Concomitantly, the forward voltage drop V_2 is decreased from $0.16 \pm 0.11 \text{ V}$ to $0.15 \pm 0.21 \text{ V}$. Nonetheless, it should be reminded that the determined electrical parameter values are only valid within the backward sweep of the experimental (I-V) curves. Moreover, as described previously, a bias-dependent distribution of α shall be considered for a more accurate fitting on the entire bias voltage range, as well as to better explain the discrepancy between the forward and backward sweeps of the experimental (I-V) curves. This might lead to significant local deviations in the values of α , especially regarding the upper boundary condition of 5 nm which shall be carefully reassessed. Similarly, a bias-dependent distribution of V_2 should be taken into account for a better fitting accuracy, especially at low bias voltage. Nonetheless, N_D and α are the most influent parameters in the developed electrical model, which mainly determine the shape of the experimental (I-V) characteristics. Due to the very strong intercorrelation between these parameters, their physical interpretation shall thus be considered extremely carefully. Most importantly, the reported values of the electron concentration N_D within our devices are consistent with similar works making use of ALD-deposited ZnO thin films at low temperatures [61–63], concomitantly showing a decrease of N_D as the deposition temperature is decreased. As discussed within chapter 3, our electron concentration values are thus well appropriated for the formation of Schottky junctions at the Pt/ZnO interfaces. Furthermore, the physical validity of the determined electrical parameters by the non-linear curve fitting demonstrates the reliability of the developed electrical model based on thermionic emission.

4.2.2.10. Impact of the interdigitated electrodes structure on the electrical properties

As described within section 4.1.1, different layouts of the interdigitated Pt electrodes planar structure were processed by varying the inter-finger spacing and thus the total number of interdigitated fingers. The aim formulated at an early stage of this work was

initially to assess the impact of these different designs on the electrical properties of the sensors, by anticipating a potential modulation of their transducing properties.

The main impact of the different interdigitated layouts is translated into a modulation of the Schottky contact area A as well as into the number of parallelized sensing elements. Therefore, we observed that the difference in the Schottky contact area between the different designs experimentally led to minor shifts in the electrical current values. However, this modulation was not significant as the electrical current characteristics are mainly determined by the electron concentration N_D and the intrinsic barrier lowering coefficient α . Furthermore, the modulation of the Schottky contact area might have a substantial impact on the values of the Schottky depletion capacitance, used to calculate the density of interface trap states at high frequencies. Nonetheless, the additional capacitance due to interface trap states at 1 MHz, linked with their low time constant, resulted in a partial screening of the Schottky depletion capacitance. Consequently, the corresponding impact of the different interdigitated layouts on the sensors' capacitive response could not be assessed rigorously. Moreover, as the number of parallelized sensing elements are macroscopically equally distributed along the length of the cantilever between the different interdigitated layouts, no major difference could be deduced from the sensors' transducing properties.

4.2.3. Evidence of negative capacitance phenomena and capacitance modulation by light and mechanical strain

We report on the evidence of negative capacitance values in a system consisting of metal-semiconductor-metal (M-S-M) structures, with Schottky junctions made of zinc oxide thin films deposited by Atomic Layer Deposition (ALD) on top of platinum interdigitated electrodes (IDE). The M-S-M structures were studied over a wide frequency range between 20 Hz and 1 MHz. Light and mechanical strain applied to the device modulate positive or negative capacitance and conductance characteristics by tuning the flow of electrons involved in the conduction mechanisms. A complete study was carried out by measuring the capacitance and conductance characteristics under the influence of both dark and light conditions, over an extended range of applied bias voltage and frequency, as illustrated in the summary figure 4.45. An impact-loss

process linked to the injection of hot electrons at the interface trap states of the metal-semiconductor junction is proposed to be at the origin of the apparition of the negative capacitance values. These negative values are preceded by a local increase of the capacitance associated with the accumulation of trapped electrons at the interface trap states. Thus, we propose a simple device where the capacitance values can be modulated over a wide frequency range via the action of light and strain, while using cleanroom-compatible materials for fabrication. These results open up new perspectives and applications for the miniaturization of highly sensitive and low power consumption environmental sensors, as well as for broadband impedance matching in radio frequency applications.

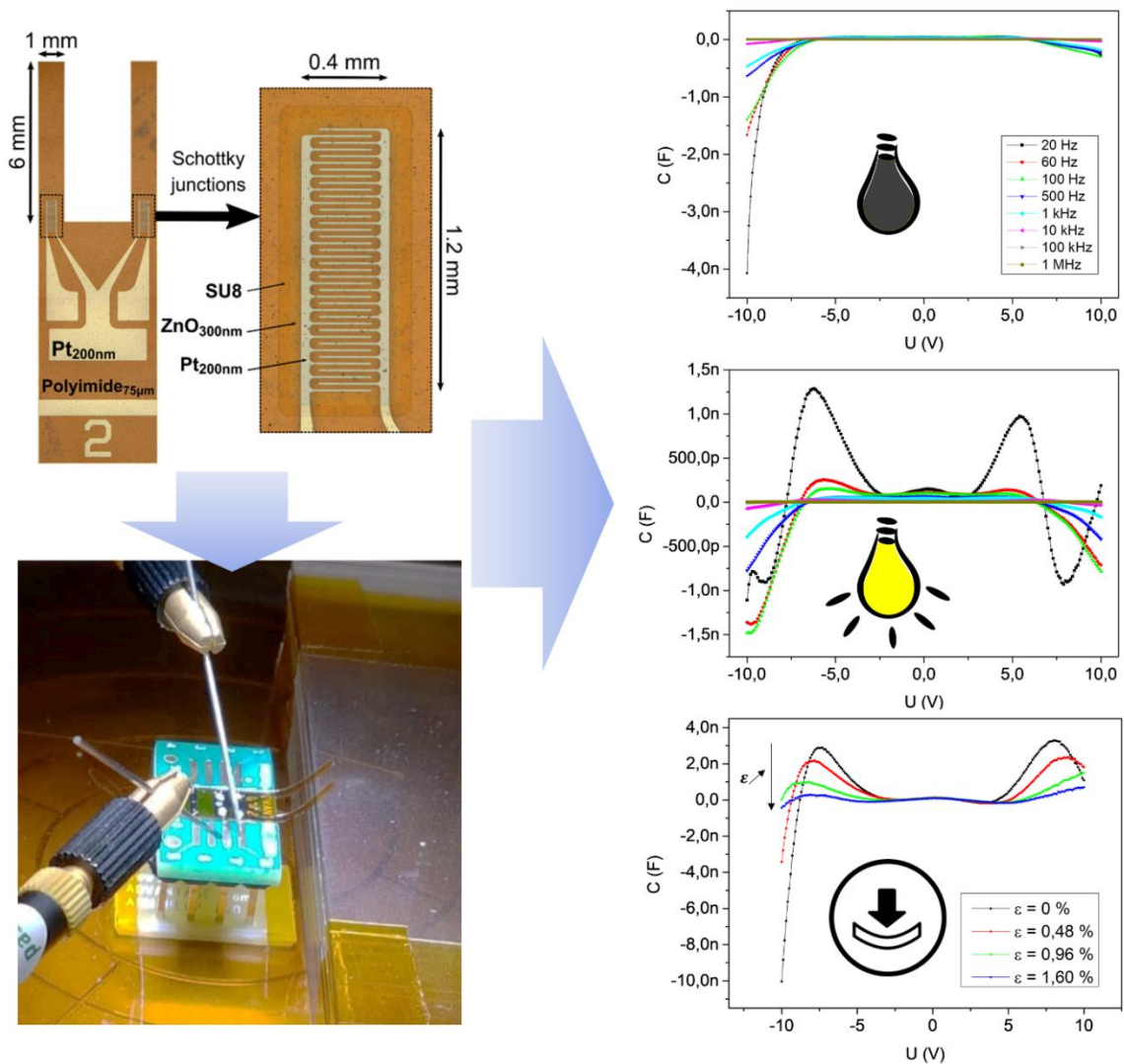


Figure 4.45. Summary figure of the evidence of negative capacitance phenomena and capacitance modulation by light and mechanical strain [2]. The metal-semiconductor-metal (M-S-M) structures were studied over a wide frequency range between 20 Hz and 1 MHz.

These results have been reported within an article published in the peer-reviewed journal *Sensors* [2], and placed within Appendix B for detailed description.

4.3. Electromechanical transduction

This section details the transduction properties of the piezotronic strain sensors, based on the results from an article published in the peer-reviewed journal *Sensors and Actuators A* [1].

4.3.1. Integration and testing

The processed piezotronic strain microsensors described in Appendix A were fixed to a PCB (PA0002-KIT, Proto Advantage, Canada) with double-sided polyimide tape (Micro to Nano, the Netherlands). The platinum metal electrodes were connected to the PCB via wire bonding using a thermosonic wirebonder (TPT HB16, Accelonix, the Netherlands). A ball bonding process was performed at a temperature of 50 °C, with gold wires of 25 µm diameter. Prior to the wire bonding, a plasma activation (100 W, 2 minutes, in Ar:O₂ gases environment at 100 mTorr) was performed on the mounted sensors to improve the metal-to-metal adhesion [64]. After soldering the pins, the sensors were integrated into the nose of an AFM (Nanonics MultiView 4000, Nanonics Imaging, Israel), as shown in Fig. 4.46. The head displacement can be controlled precisely using a stepper motor driver and a high-voltage Z-axis piezo driver.

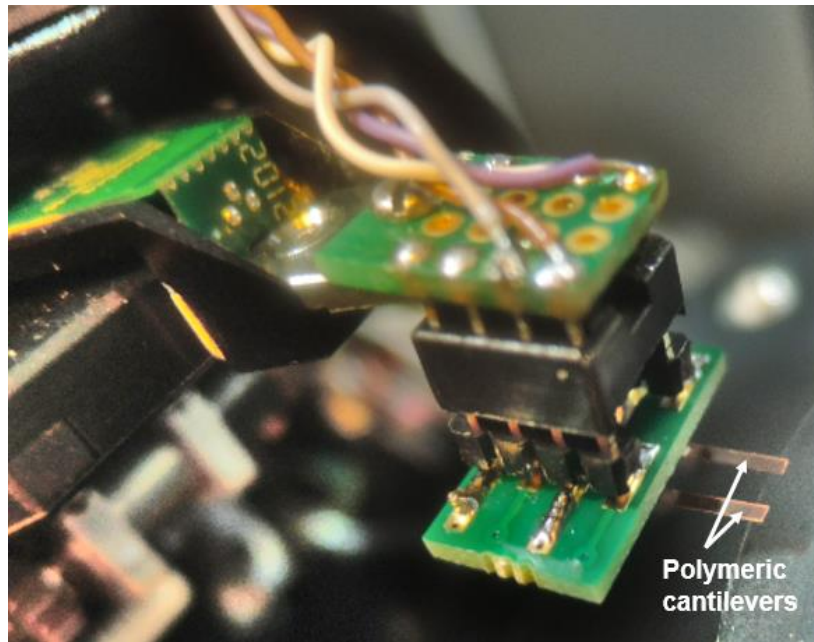


Figure 4.46. Integration of a piezotronic strain microsensor into the AFM nose. The sensors are bonded on the PCB and represented upside down on the picture, with the polymeric cantilevers positioned and clamped at the edge of the PCB.

The measurement chain illustrated in Fig. 4.47 consisted of an arbitrary function generator (AFG1062, Tektronix) connected to an amplifier (33502A, Keysight), leading to the input of the sensors integrated within the AFM head. The imposed bias was either AC or DC modulated. A variable gain transimpedance preamplifier (DLPCA-200, FEMTO, Germany) was connected to the output of the sensors, converting the sensor's current into usable voltage. The gain used was switched between 10^3 and 10^8 in order to reach an output voltage of approximately 1 V, depending on the imposed bias voltage and the sensor's electrical properties, with the corresponding detection time constants inferior to 2 μs and 140 μs , respectively [65]. This voltage was visualized and recorded in the frequency domain using an oscilloscope (WaveSurfer 3024, Teledyne LeCroy), also used for noise analysis. The piezotronic self-sensing cantilevers were put in contact with a thin silicon wafer clamped to the Z-axis piezo stage, inducing the cantilevers' upward bending. The stepper motor driver from the Nanonics was used to coarsely approach and position the sensors close to the clamped obstacle. Force spectroscopy measurements in Atomic Force Microscopy (AFM) configuration were achieved in AC and DC modulated bias voltage by connecting the output of the transimpedance preamplifier to a lock-in amplifier (HF2LI,

Zurich Instruments, Switzerland), with a time constant defined as 70 μs . Approach/withdraw sequences were performed by using a Z-axis piezo positioner with a time constant of 1 ms (P-622-ZCD, Physik Instrumente GmbH, Germany) connected to a piezo controller (E-754_1CD, Physik Instrumente GmbH, Germany), allowing a linear travel range of 250 μm by a closed loop configuration. Furthermore, the piezotronic sensors' performances were compared with a commercial piezoresistive strain gauge consisting of metal Cu/Ni electrodes embedded within a polyimide foil (Wire Lead Strain Gauge 3.5mm, RS PRO 865-6226). Similarly to the piezotronic sensors, the piezoresistive references were stuck to a PCB with double-sided polyimide tape. An in-house preamplifier was designed and connected to the strain gauge, where the output DC bias voltage was monitored by a Wheatstone bridge using a three-wire, quarter-bridge circuit to minimize noise effect. The piezoresistive preamplifier was used with a gain of 100 and a time constant of 220 μs [66].

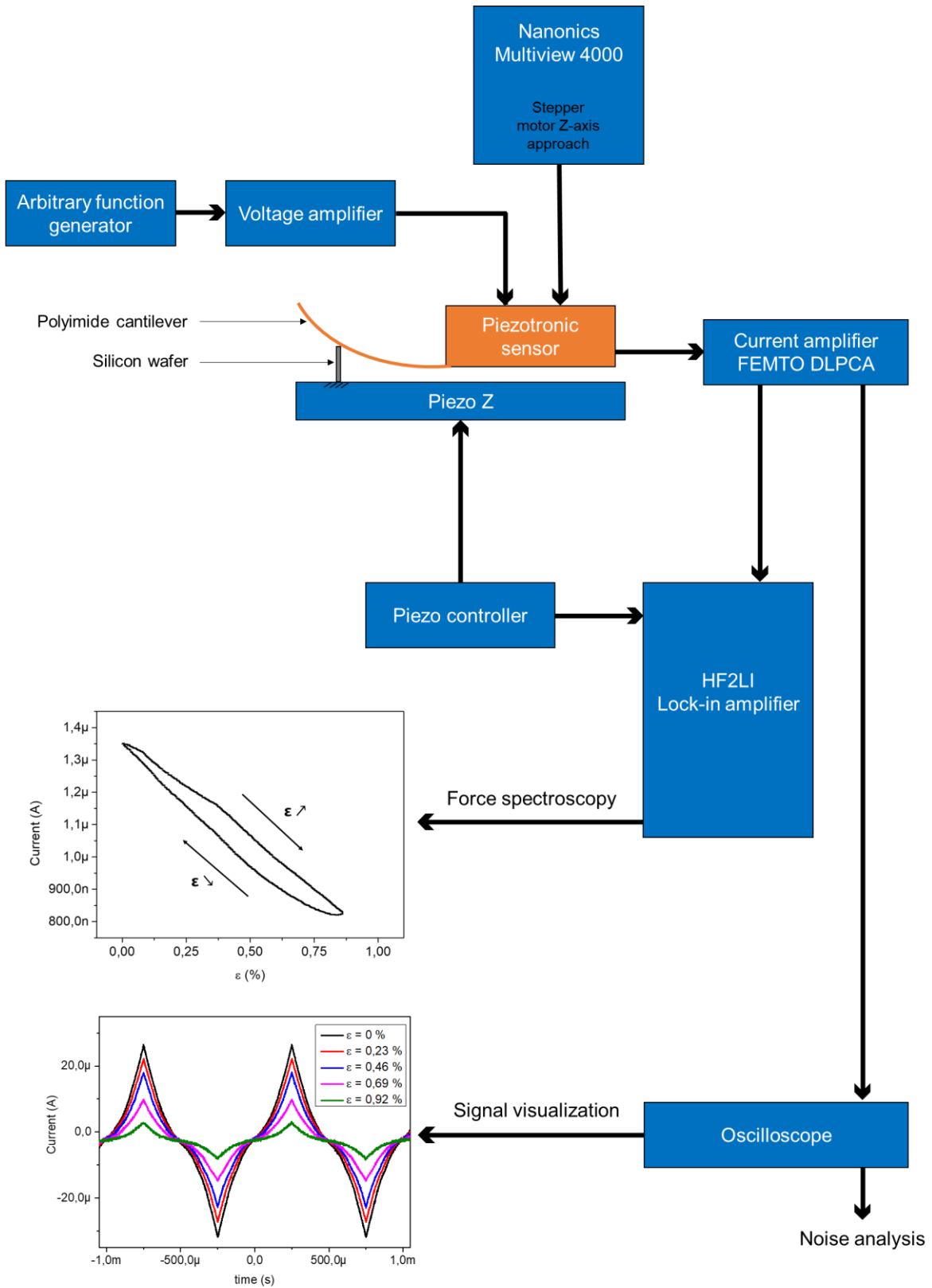


Figure 4.47. Illustration of the measurement chain used for the electromechanical transduction.

4.3.2. Results and discussion

As discussed in chapter 3 and in sections 4.2.1 and 4.2.2, in order to promote the formation of a Schottky junction and to favour the piezoelectric response of the ZnO material, low temperature ALD depositions of 80 °C and 60 °C were used for the deposition of ZnO thin films integrated within the piezotronic strain microsensors. The use of low temperatures is further motivated to avoid the degradation of the polyimide substrate and the protective SU8 resist.

Two sets of interdigitated platinum electrodes were used to maximize the size of the Schottky contact interface, leading to the creation of several back-to-back Schottky diodes within the area defined by the ZnO pad. Upon downward displacement of the head, the cantilevers were bent upwards, leading to the generation of a compressive strain calculated in the clamped area of the sensors. Our devices showed electromechanical transducing with the current response being modulated by different controlled compressive strain under a defined AC bias voltage, as illustrated in Fig. 4.48(a). The current values are decreased as increasing compressive strains are applied, which signifies that negative piezoelectric polarization charges are induced at the Pt/ZnO interfaces, concomitantly leading to an increase of the Schottky barrier height. The use of an AC bias voltage allows for the visualization of the sensor current response over the whole tension range at a defined frequency. Another reason is synchronous detection, where the sensor signal can be easily collected in a high-noise environment. The current response is non-linear and shows a clear rectification behaviour. The sensors' responses are constantly symmetrical for both forward and reverse bias, which is typical for devices using the same metal electrodes in the case of back-to-back diodes [34,67]. Some small differences may appear between the forward and reverse cases, leading to minor deviations in the current values. This is linked to the presence of interface states at the metal-semiconductor junctions, which can randomly affect the Schottky barrier formation and its subsequent height in both junctions [26]. Due to the high resistivity of the sensors, related to low temperature deposition, the bias voltage imposed had to be substantially increased to 10 volts to further promote the non-linear behaviour. An electrical power consumption inferior to

50 μW is reported, which is in consensus with the piezotronic sensor technologies typically operating within the microAmpere and microWatt ranges [68]. Piezotronic sensors thus appear as a promising candidate for low power consumption sensing technologies, compared to piezoresistive and capacitive sensors operating in milliWatts range.

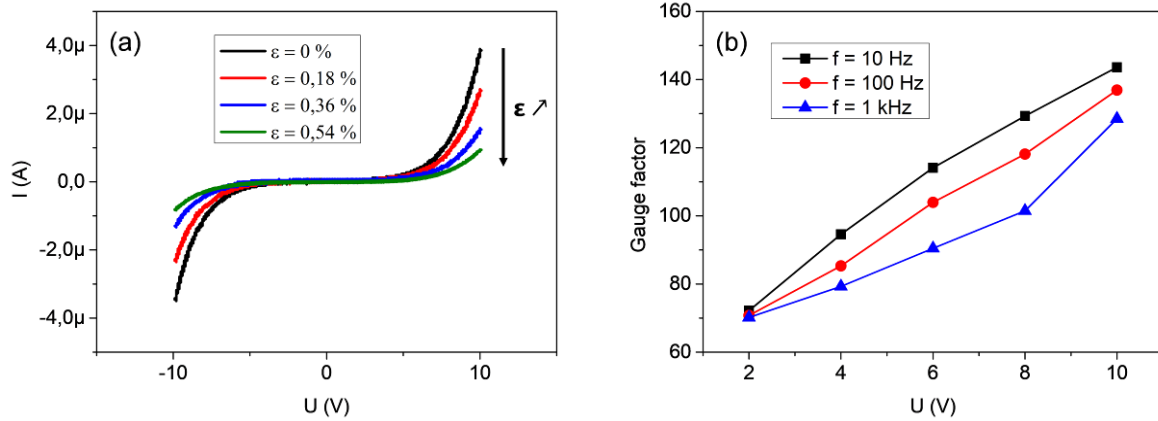


Figure 4.48. Transducing response of the piezotronic strain microsensors. The ZnO thin film was deposited by ALD at 80 °C; (a) Current response under controlled compressive strain steps. The bias voltage is AC modulated at 100 Hz; (b) Gauge factor evolution for different AC bias voltages at different frequencies.

The strain ε generated in the clamped area of the cantilevers was calculated using equation (4.4) presented earlier in this chapter:

$$\varepsilon = \frac{3}{2} \cdot \frac{(t - t_s)(2L - L_s)}{L^3} \cdot d \quad (4.4)$$

With t being the cantilever thickness, t_s the sensor thickness, L the cantilever length, L_s the sensor length, and d the deflection imposed on the cantilever relative to the contact point (at length L) of the force applied by the Z-axis piezostage object.

Moreover, the following equation was used to calculate the gauge factor, based on the absolute value of the ratio of relative change in the electrical current I to the mechanical strain ε [67,68]:

$$GF = \left| \frac{\Delta I}{I_0} \cdot \frac{1}{\varepsilon} \right| \quad (4.44)$$

With I_0 being the steady state current for a given bias, and ΔI the change in current under a given strain ε for the same applied bias. The strain used in equation (4.44) corresponds to the strain generated in the clamped area of the sensors, calculated using equation (4.4).

Based on these considerations, gauge factor values were calculated by sweeping the AC bias voltages, as well as the bias frequencies imposed to the sensors processed with an ALD deposition temperature of 80 °C, as shown in Fig. 4.48(b). A clear trend can be identified as the gauge factor values increase while increasing the AC bias voltages, for every frequency studied. The highest gauge factor value was evaluated at 150, for a bias voltage of 10 V promoting the non-linear behaviour of the sensors. As reported in the previous section, decreasing the ALD deposition temperature to 60 °C leads to a meaningful increase in the resistivity and decrease of the electron concentration of the ZnO thin films, which is accompanied by a decrease in the sensors' current values, as illustrated by Fig. 4.49.

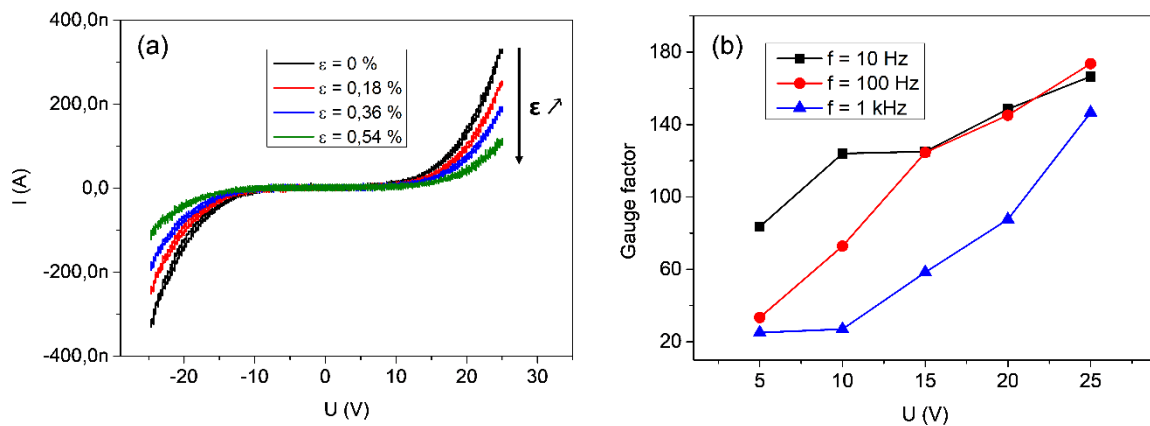


Figure 4.49. Transducing response of a piezotronic strain microsensors. The ZnO thin film was deposited by ALD at 60 °C; (a) Current response under controlled compressive strain steps. The bias voltage is AC-modulated at 10 Hz; (b) Gauge factor evolution for different AC bias voltages and frequencies.

At this lower growth temperature of the ZnO thin film, the sensors typically operate within a range of tens to hundreds of nanoAmperes while the imposed AC bias voltage increased up to 25 V. The same trends can be identified, as both the non-linear behaviour and the increase of the gauge factor are promoted at higher bias voltages. Interestingly, these gauge factor values decrease as the AC bias frequency increases.

Low bias signal frequency measurements are also accompanied by a decrease in the hysteresis observed for lower AC bias voltages, as illustrated by Fig. 4.50, which is attributed to the carriers' dynamics following the AC bias signal at lower frequencies.

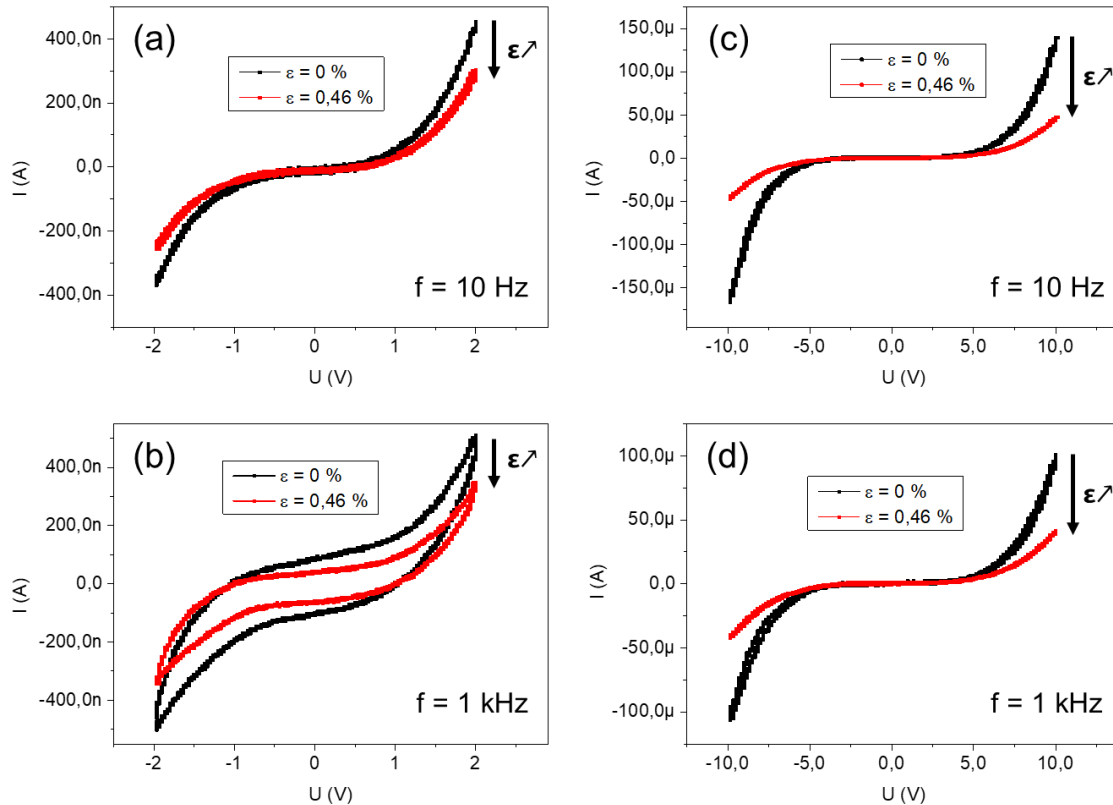


Figure 4.50. Current response of a piezotronic strain microsensor under a controlled compressive strain step for different AC bias voltages and frequencies. The ZnO thin film was deposited by ALD at 80 °C; (a) The bias voltage is AC modulated at 2 V and 10 Hz; (b) The bias voltage is AC-modulated at 2 V and 1 kHz; (c) The bias voltage is AC-modulated at 10 V and 10 Hz; (d) The bias voltage is AC-modulated at 10 V and 1 kHz.

Hussain et al. [13] attributed these carrier dynamics in Schottky junctions to the presence of a continuous distribution of interface state traps. When the time period of the AC bias signal corresponds to this interface trap time constant, the peak loss associated with the interface trap levels then occurs. If the bias frequency is lower, the interface trap states are thus able to follow the AC signal, in such a way that no energy loss occurs.

We used AFM force spectroscopy to characterize the sensitivity of the piezotronic strain sensors by their gauge factor. Approach/withdraw sequences of the cantilever

end on top of a hard silicon surface were performed at a scan speed of 10 $\mu\text{m/s}$. The stability and linearity of the sensors' response was carefully studied. The current response of the piezotronic strain microsensor under a compressive strain for several approach and withdraw sequences is depicted in Fig. 4.51.

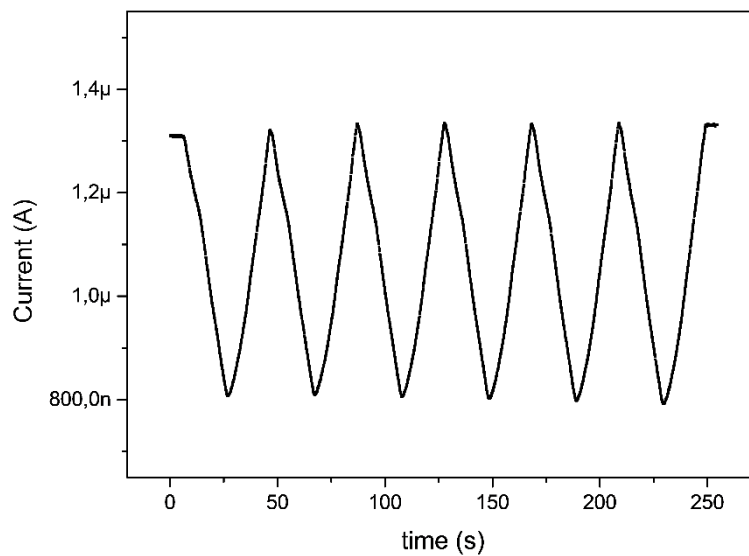


Figure 4.51. Current response of a piezotronic strain microsensor as a function of several approach and withdraw sequences, using a compressive strain. The bias voltage is AC-modulated at 10 V and 10 Hz for lock-in detection. The measurement was performed in a closed loop configuration, using the travel range of 250 μm from the z-axis piezo positioner and a scan speed of 10 $\mu\text{m/s}$. The zinc oxide thin film was deposited by ALD at 80 $^{\circ}\text{C}$.

As observed, the current values are similar for every approach/withdraw sequence performed. Furthermore, the current recovered its initial value when the strain was released, which demonstrates the good stability of the sensor. Moreover, the current was quantitatively described as a function of the strain applied to the sensors upon the AC modulation of the bias signal. A typical curve obtained describing a single approach/withdraw sequence is illustrated in Fig. 4.52.

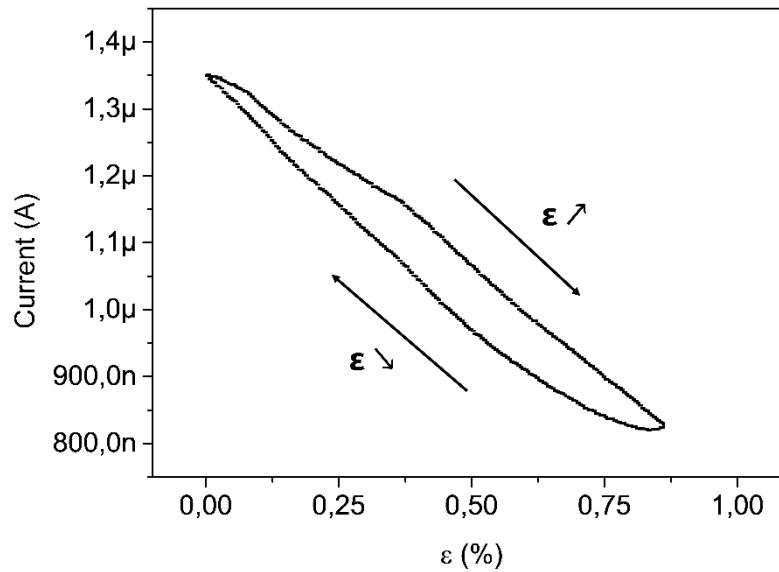


Figure 4.52. Transducing the current response of a piezotronic strain microsensor as a function of a forward and backward increasing compressive strain. The bias voltage is AC modulated at 10 V and 10 Hz for lock-in detection. The measurement was performed in a closed loop configuration of the z-axis piezo positioner within a range of 250 μm. The sensor is made of a ZnO thin film deposited by ALD at 80 °C.

As shown in Fig. 4.52, the sensor's behaviour is monotonic for both the approach and the withdraw sequences. Nevertheless, a hysteresis can be observed. The relative hysteresis error [69] was calculated over the whole strain range, which is defined as the difference in percentage of Amperes (%A) of the output current when measuring it with the same applied strain between the approach and withdraw sequences.

More precisely, the relative hysteresis error is defined as the difference between the approach and withdraw sequences determined with increasing and decreasing strain. It is the difference in %A of the output current when measuring it with the same applied strain between the approach and withdraw sequences. First, the current y-axis scale was rescaled from 0%A to 100%A between its minimal and maximal value, by using the following equation:

$$Y_{\text{new}} = \frac{Y_{\text{max}_{\text{new}}} - Y_{\text{min}_{\text{new}}}}{Y_{\text{max}_{\text{old}}} - Y_{\text{min}_{\text{old}}}} \cdot (Y_{\text{old}} - Y_{\text{max}_{\text{old}}}) + Y_{\text{max}_{\text{new}}} \quad (4.45)$$

With Y_{new} and Y_{old} being the current values expressed in the new scale (%A) and the old scale (A), respectively, $Y_{\text{max}_{\text{new}}}$ and $Y_{\text{min}_{\text{new}}}$ being the maximal and minimal

values of the new scale corresponding to 100%A and 0%A, respectively, and $Y_{\max_{\text{old}}}$ and $Y_{\min_{\text{old}}}$ being the maximal and minimal values of the old scale expressed in A.

By applying the numerical values to the new scale between 0% and 100%, we obtain:

$$Y_{\text{new}} = \frac{100}{Y_{\max_{\text{old}}} - Y_{\min_{\text{old}}}} \cdot (Y_{\text{old}} - Y_{\max_{\text{old}}}) + 100 \quad (4.46)$$

The relative hysteresis error was thus calculated for the piezotronic strain microsensors based on measurements from Fig. 4.52, as well as for the commercial piezoresistive strain gauge based on measurements from Fig. 4.56 (displayed further within this section). The corresponding results are presented in Fig. 4.53 and 4.54, respectively.

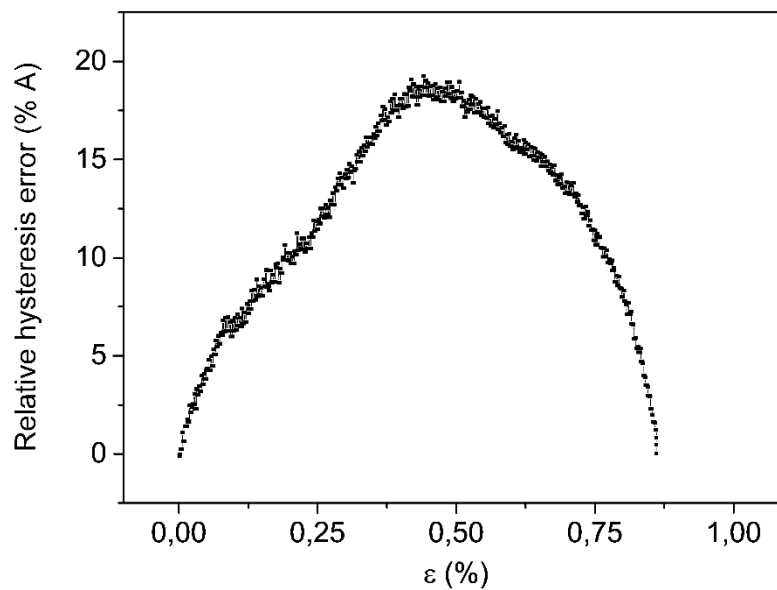


Figure 4.53. Relative hysteresis error of the piezotronic strain microsensors, based on measurements from Fig. 4.52.

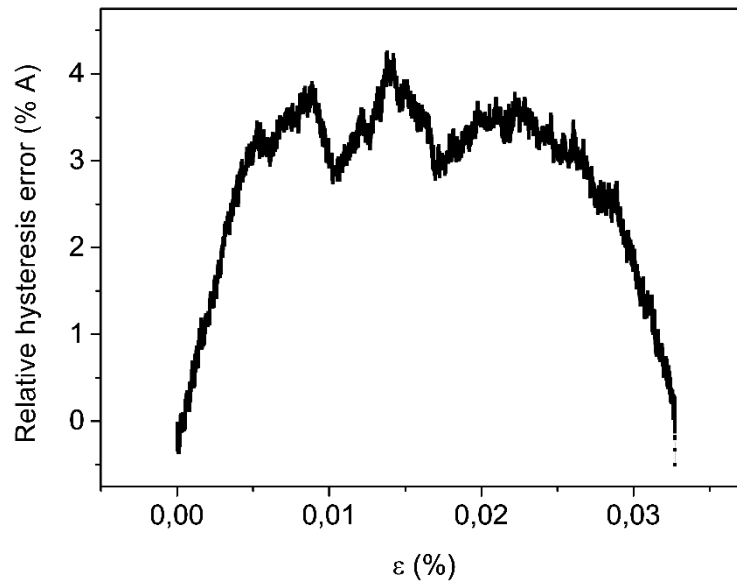


Figure 4.54. Relative hysteresis error of the commercial piezoresistive strain gauge, based on measurements from Fig. 4.56.

The maximum hysteresis error is defined as the maximum deviation in the current values expressed in %A between the approach and the withdraw sequences. It has been calculated at a value of 19.3%A for the piezotronic strain microsensor, based on measurements from Fig. 4.53, and at a value of 4.3%A for the commercial piezoresistive strain gauge based on measurements from Fig. 4.54.

Force spectroscopy measurements were also performed while applying a DC biasing to the piezotronic sensors, depicted in Fig. 4.55.

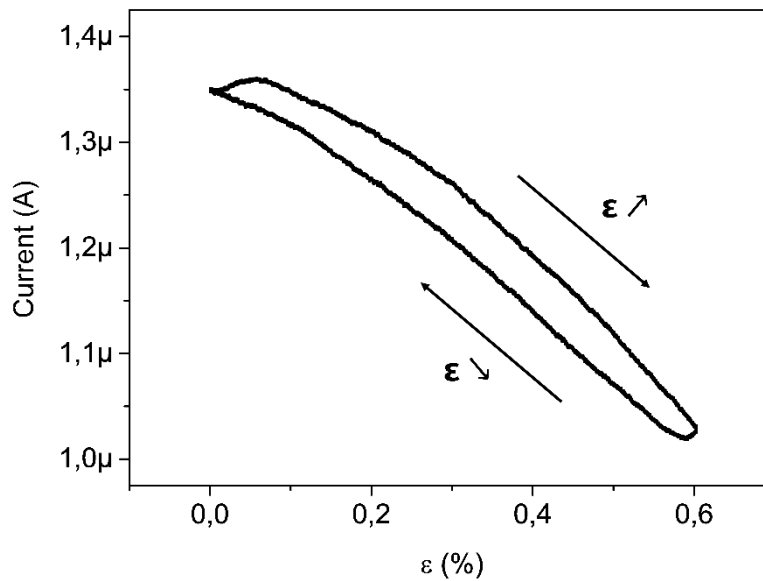


Figure 4.55. Transducing current response of a piezotronic strain microsensor as a function of a forward and backward increasing compressive strain for a DC bias voltage set to 10 V. The measurement was performed in a closed loop configuration of the z-axis piezo positioner within a range of 250 μm . The sensor is made of a ZnO thin film deposited by ALD at 80 $^{\circ}\text{C}$.

The same trends were observed when compared to an AC modulation of the bias, showing that DC bias also exhibits similar strain sensitivity while reaching comparable current values under straining. Given the fast response inferior to the millisecond of every electrical component in the measurement chain, and the scan speed of 10 $\mu\text{m/s}$ for an approach and withdraw sequence of 25 s, one can eliminate artefacts of time delays originating from the instrumentation. Another hypothesis to explain this hysteresis concerns the viscoelastic response of the creep deformation of the polymer films [70]. The viscoelastic relaxation stress of polyimide foil after strain releasing was thoroughly characterized by B. Y. Dharmadasa et al. with stress relaxation time in the order of hundreds of seconds [71]. The same authors have also highlighted the impact of the strain rate with force-time measurements using different compressive velocity and inducing substantial changes in the stress relaxation time of the polyimide sample. In order to investigate the origin of that hysteresis in more detail, we took similar measurements with a commercial piezoresistive strain gauge consisting of thick metal Cu/Ni electrodes embedded within a polyimide foil. The curve obtained is displayed in Fig. 4.56.

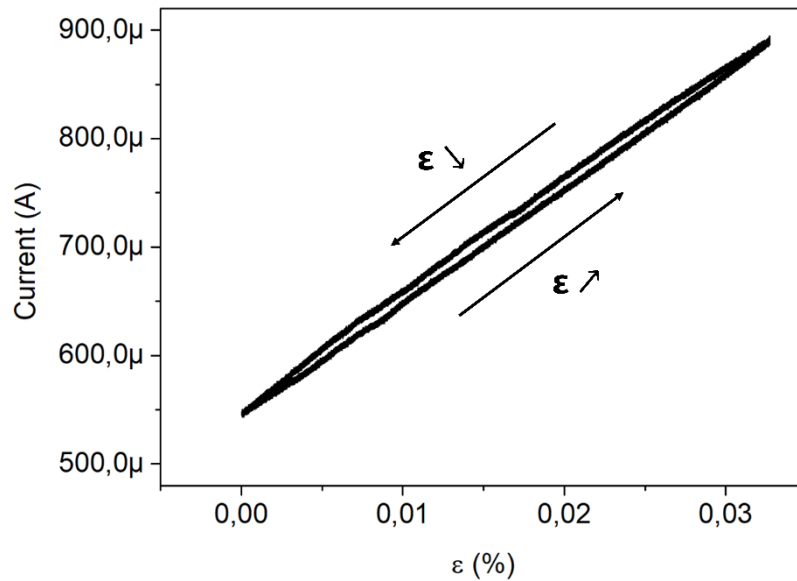


Figure 4.56. Current response of a commercial piezoresistive strain gauge as a function of a forward and backward increasing tensile strain. The bias voltage is DC modulated at 1 V. The measurement was performed in a closed loop configuration, using the travel range of 250 μm from the z-axis piezo positioner with a scan speed of 10 $\mu\text{m/s}$.

A slight hysteresis can still be seen, although it is less marked than the one observed for the piezotronic sensors, as observed by the decrease of the maximum hysteresis error calculated at a value of 4.3%A. This can be explained by the more rigid structure of the piezoresistive strain gauge, where the metal Cu/Ni electrodes are 10 μm thick and integrated along the whole length of the cantilever. As pointed out by N. Obaid et al., if the aspect ratio of the reinforcement structures in the polymer structure is high, the properties of the composite approach those of these long metallic structures with shorter stress relaxation time [72]. Nonetheless, in our strain sensors, the thicknesses of the ZnO thin film and the Pt metal electrodes are inferior to 1 μm , and are located close to the clamped area of the cantilevers. This leads to a softer structure where the viscoelastic response of the substrate is thus more pronounced and close to neat polyimide with an increase of the observed strain-displacement hysteresis.

In order to assess the impact of the piezotronic effect on the sensors, namely the change in the Schottky barrier height under straining, Zhou et al. [34] introduced the following equation, based on the thermionic emission model:

$$\Delta\phi_B^{\text{piezotronic}} = -\frac{k_B \cdot T}{q} \cdot \ln\left(\frac{I_\varepsilon}{I_0}\right) \quad (4.47)$$

Where $\Delta\phi_B^{\text{piezotronic}}$ is the change in the Schottky barrier height due to the piezotronic effect expressed in eV, I_ε and I_0 are the current flowing out of the piezotronic sensors, with and without straining applied, respectively. The corresponding evolution of the Schottky barrier height as a function of the applied strain (based on data from Fig. 4.52) is displayed in Fig. 4.57.

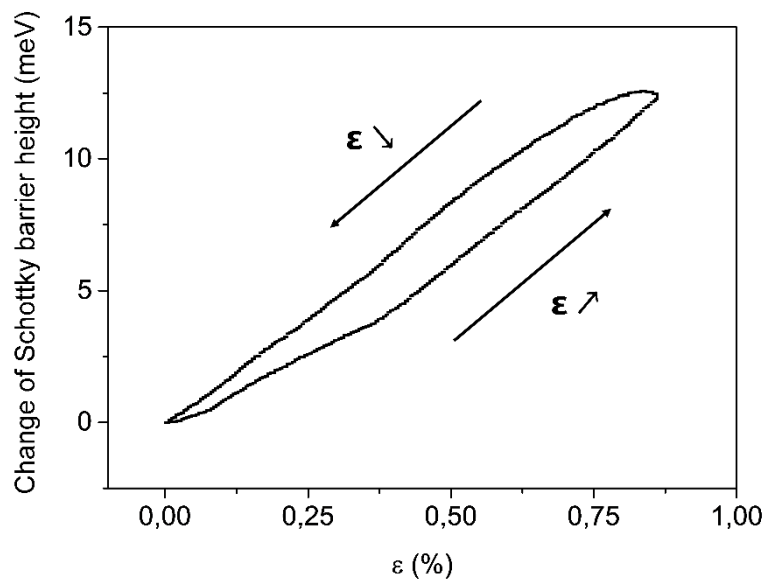


Figure 4.57. Change of the Schottky barrier height of a piezotronic strain microsensors as a function of a forward and backward increasing compressive strain.

Its values increase monotonously up to 12.6 meV with an increasing compressive strain up to 0.83%. These values are consistent with those reported in the literature [34,67] and confirm the expected modulation of the Schottky barrier height by the piezotronic effect.

4.3.3. Noise analysis

The spectral noise density S_{total} was measured for different DC bias voltages, with a sensor made of a ZnO thin film deposited by ALD at 80 °C, as illustrated in Fig. 4.58.

These measurements revealed the presence of three main sources of noise (detailed in Chapter 2, section 2.3.11), as shown by the following equations [73,74]:

$$S_{\text{total}} = S_{\text{Johnson-Nyquist}} + S_{\text{Shot noise}} + S_{\text{Flicker noise}} \quad (4.48(a))$$

$$S_{\text{total}} = \frac{4k_B T}{R_S} + 2q(I_{\text{diode}} + 2I_S) + \frac{AI^\beta}{f^\gamma} \quad (4.48(b))$$

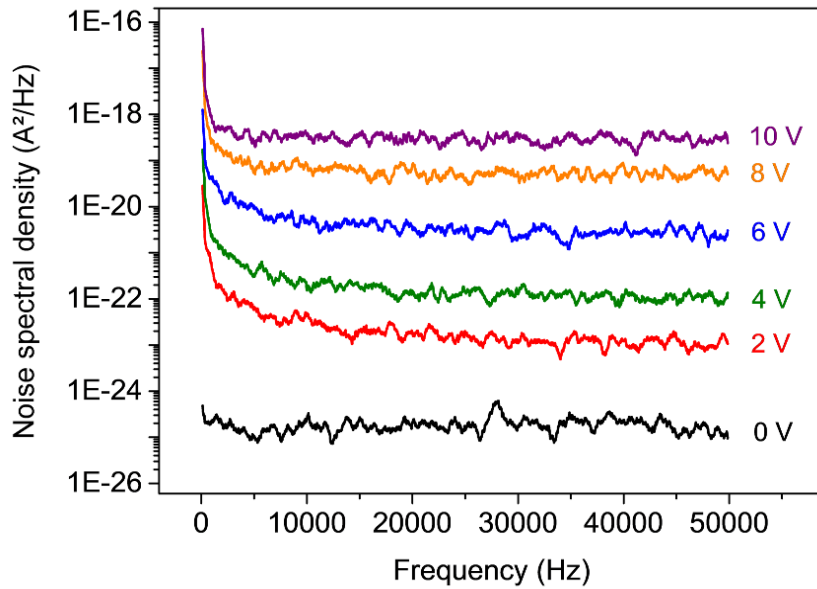


Figure 4.58. Noise spectral density evolution of a piezotronic strain microsensor for different DC bias voltages measured at room temperature. The sensors integrated a ZnO thin film deposited by ALD at 80 °C.

More details concerning the experimental protocol for the extraction of the noise spectral density values are available in the Appendix C. When no DC bias voltage was applied, the noise spectral density resulted in a constant background level corresponding to the Johnson-Nyquist noise. However, when the DC bias voltage values were increasing, the two other sources of noise started appearing at a bias voltage of 2 V. On the one hand, the flat background level was gradually shifting to higher noise spectral density values while the bias voltage was increasing, which corresponded to the appearance of shot noise in the sensors, typical for diode junctions. On the other hand, we observed that the noise spectral density values were

increasing for low frequencies (below 5 kHz) with a $1/f$ shape, which is commonly attributed to the flicker noise appearance. The same trends were observed for a junction made of a ZnO thin film processed at a lower ALD deposition temperature of 60 °C, as shown by Fig. 4.59.

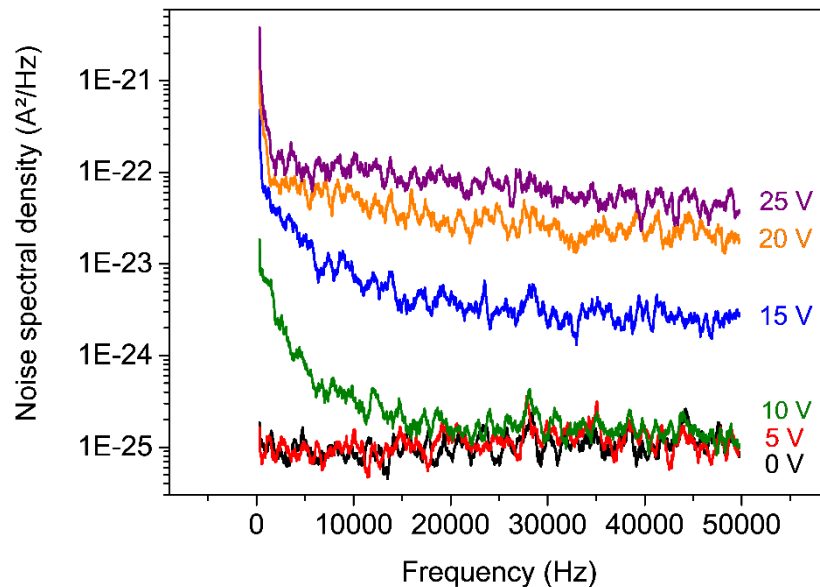


Figure 4.59. Noise spectral density evolution of a piezotronic strain microsensor for different DC bias voltages measured at room temperature. The sensors integrated a ZnO thin film deposited by ALD at 60 °C.

Interestingly, the noise spectral density values remained extremely constant when the applied DC bias was increased from 0 V to 5 V, where they related to the Johnson-Nyquist noise background level. For DC bias voltage higher than 10 V, the background level and the low frequencies' noise spectral density values showed a meaningful increase, linked to the respective appearance of the shot noise and the flicker noise in the piezotronic sensors. Hence, there was a transition occurring between 5 V and 10 V where the diode behaviour was predominant in the sensors, leading to the reported apparition and increase of the shot noise. One way of estimating the series resistance at 0 V consists of measuring the average noise spectral density value in the current without applying any DC bias. In doing this, the total noise only corresponds to the Johnson-Nyquist noise and the series resistance can be extracted with the following equation:

$$R_S(0 \text{ V}) = \frac{4 \cdot k_B \cdot T}{S_{\text{total}}} \quad (4.49)$$

The average noise spectral density was estimated at a value of $1.02 \times 10^{-25} \text{ A}^2 \cdot \text{Hz}^{-1}$ for $60 \text{ }^\circ\text{C}$ and $1.78 \times 10^{-25} \text{ A}^2 \cdot \text{Hz}^{-1}$ for $80 \text{ }^\circ\text{C}$. The corresponding series resistance values at 0 V were obtained as $161.8 \text{ k}\Omega$ at $60 \text{ }^\circ\text{C}$ and $92.6 \text{ k}\Omega$ at $80 \text{ }^\circ\text{C}$, respectively. These observations further confirm that the resistivity and series resistance of the ZnO thin films are increased at lower deposition temperatures and strongly affect the conduction transport mechanism for low bias voltages. A careful consideration should thus be given to low frequency measurements achieved with an AC modulation. On the one hand, the low frequency measurements achieved on our sensors contribute to decreasing the hysteresis and increasing the sensitivity of the sensors as demonstrated previously. On the other hand, they are accompanied by a strong increase in the noise spectral density values linked with the apparition of the flicker noise.

Furthermore, the minimal strain ε_{min} detectable by the instrumentation can be determined via the signal-to-noise ratio (SNR), defined as the ratio between the desired signal and the background noise. The desired signal in our case corresponds to the minimal current change ΔI_{min} detectable by the instrumentation induced by ε_{min} . It was thus determined by using the gauge factor equation (4.44), as the product between the gauge factor GF , the steady state current I_0 and the minimal strain ε_{min} detectable by the instrumentation. Also, the background noise must be expressed in units of Amperes to be homogeneous with ΔI_{min} . Consequently, the background noise was defined as the square root of the noise spectral density integrated over the bandwidth of the lock-in amplifier (i.e. 500 Hz) for a given frequency. Given these considerations, the SNR was thus expressed as:

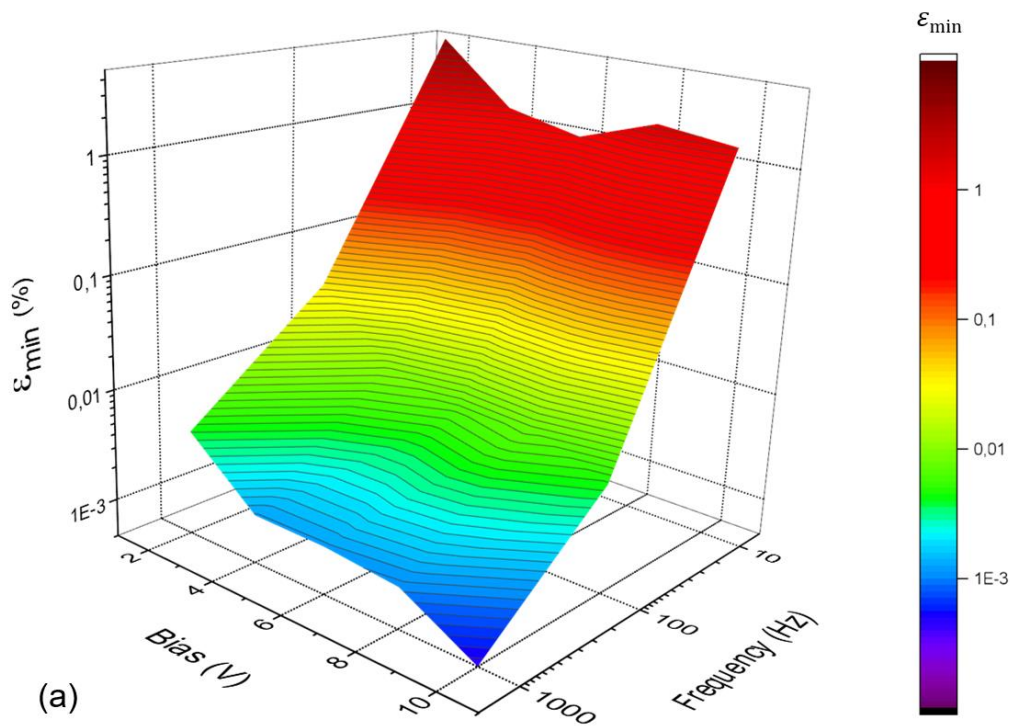
$$\text{SNR} = \frac{\Delta I_{\text{min}}}{\sqrt{\int_{-BW/2}^{BW/2} S_{\text{total}} \cdot df}} = \frac{GF \cdot I_0 \cdot \varepsilon_{\text{min}}}{\sqrt{\int_{-BW/2}^{BW/2} S_{\text{total}} \cdot df}} \quad (4.50)$$

In order to estimate ε_{min} , a value of 3 was attributed to the SNR, that value being considered acceptable for estimating the detection limit for a lock-in amplifier as

defined by R.E. Best [75] (i.e. the signal being measured should be three times superior to the background noise signal to be detected). The minimal strain ε_{\min} detectable by the instrumentation was thus calculated as:

$$\varepsilon_{\min} = \frac{3 \cdot \sqrt{\int_{-BW/2}^{BW/2} S_{\text{total}} \cdot df}}{GF \cdot I_0} \quad (4.51)$$

The noise spectral density values reported in this section were thus associated to the gauge factor and steady-state current values reported in the previous section for applied frequencies of 10 Hz, 100 Hz and 1 kHz, as well as with different bias voltage values. The resulting ε_{\min} values as a function of the applied bias voltage and frequency, for ZnO deposition temperatures of 80 °C and 60 °C are displayed in Fig. 4.60(a) and (b), respectively:



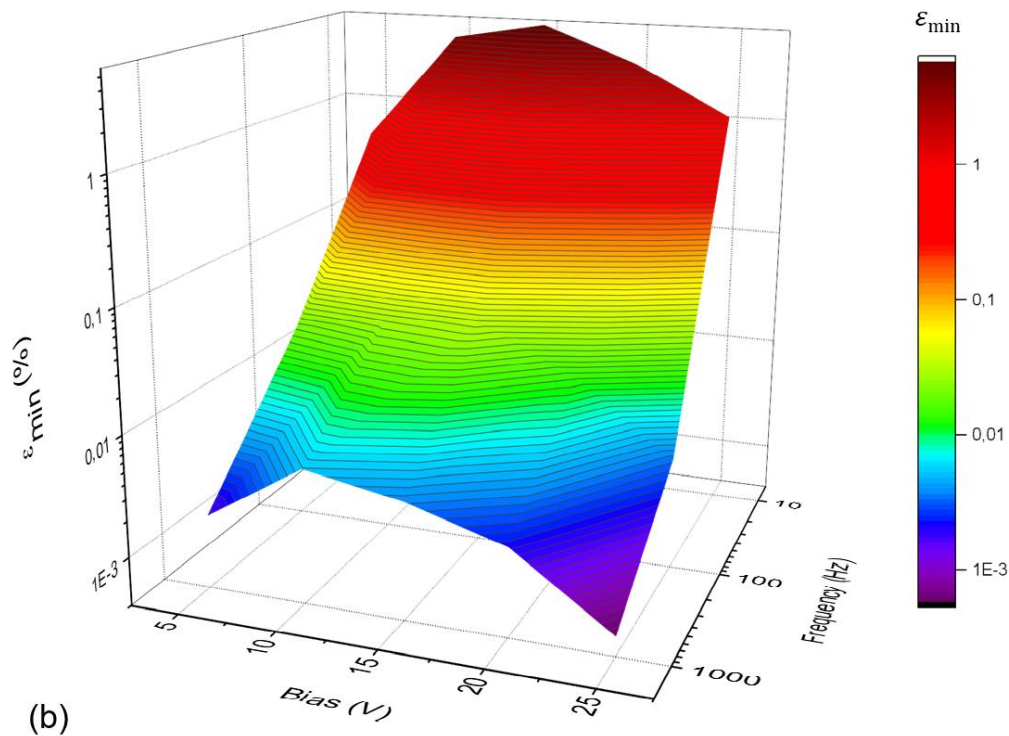


Figure 4.60. Minimal strain detectable by the developed instrumentation for a SNR value of 3 according to R. E. Best [75] for a lock-in amplifier, as a function of the applied bias voltage and frequency, for piezotronic sensors with (a) a ZnO deposition temperature of 80 °C and (b) a ZnO deposition temperature of 60 °C.

The obtained evolution of ϵ_{\min} is similar for deposition temperatures of 80 °C and 60 °C, as the minimal strain detectable by the instrumentation is substantially increased from approximately 10^{-3} % at 1 kHz to 1 % at 10 Hz. This is linked with the presence of the flicker noise at low frequencies, which is consistent with the sharp increase of the noise spectral density values reported in Fig. 4.58 and Fig. 4.59 in the low frequency domain. Moreover, ϵ_{\min} is not meaningfully affected by the applied bias voltage, as ΔI_{\min} is increasing accordingly to the background noise level for increasing bias voltage values. This strong increase in the minimal strain ϵ_{\min} detectable by the instrumentation at lower frequencies provide useful guidelines for future integration and testing of piezotronic sensors and should thus be carefully considered when performing measurements and designing the measurement chain.

4.4. Conclusion

The microfabrication of strain-sensitive microsensors integrated in millimetre-sized cantilevers on flexible polymeric substrates was successfully achieved by means of maskless laser lithography. The developed microfabrication process flow highlighted the difficulties linked with the integration of inorganic thin films onto a polymeric substrate. A particular attention was directed to the choice of the metal electrodes as well as to the mitigation of cracks propagation due to thermal shocks by appropriate adjustments of the sensor's design and process flow. Pt/ZnO/Pt back-to-back Schottky diode junctions have been shaped in interdigitated microelectrodes to get piezotronic strain sensing on the clamp area of the cantilever structure. The description of the conduction mechanisms occurring within the piezotronic strain microsensors has been thoroughly studied based on the thermionic emission model. The electrical current characteristics are dominated by the reverse biased Schottky junction. The lack of saturation was explained by considering the combined impact of the image-force lowering and the static lowering. A careful investigation of the Pt/ZnO interface was conducted, revealing the prominent impact of the interface trap states on the electrical properties with an estimation of their density and time constant. Non-linear fittings of the experimental (I-V) curves were performed, highlighting the dominant impact of both the electron concentration N_D and the intrinsic barrier lowering coefficient α on the electrical characteristics, as well as the strong intercorrelation between these parameters. The determined values of the electron concentration are ranging between $1.19 \times 10^{17} \pm 0.69 \times 10^{17} \text{ cm}^{-3}$ to $7.49 \times 10^{16} \pm 8.73 \times 10^{16} \text{ cm}^{-3}$ for ALD deposition temperatures of 80 °C and 60 °C, respectively. This results in ZnO thin films with low electron concentration, whose values are appropriated for the formation of a Schottky junction, concomitantly demonstrating the reliability of the developed electrical model based on thermionic emission. Furthermore, we evidenced the presence of negative capacitance values at the Pt/ZnO/Pt Schottky junctions, where the capacitance can be modulated over a wide frequency range via the action of light and strain. These results open up new perspectives and applications in the miniaturization of highly sensitive and low power consumption environmental sensors, as well as for broadband impedance matching by tank circuit in radio frequency applications. Transducing

capability was demonstrated for applied strains inferior to 1% for both DC and AC bias modulation, with the measured gauge factor as high as 150, leading to the expected Schottky barrier height modulation by the piezotronic effect. Spectral noise density measurements revealed the presence of the Johnson-Nyquist noise background level, as well as the appearance of the shot noise and the flicker noise when the bias voltage imposed on the sensors was increased. The results obtained are highly promising and pave the way towards the processing of ultrasensitive strain microsensors on MEMS structures.

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5. Full-SU8 body piezotronic strain microsensors

This chapter is dedicated to the strain sensors size miniaturization for integration in microcantilevers in a full polymer body. The miniaturization of our strain sensors into a MEMS (Micro-Electro-Mechanical-Systems) makes them more prone for AFM (Atomic Force Microscopy) scanning probe operations on commercial machines, while greatly improving the sensitivity to small mechanical deformations. Miniaturized structures are also more prone for sensors' array architectures able to perform faster parallelized analysis for two-dimensional mapping of strain as AFM force spectroscopy [1,2]. Furthermore, a new microfabrication flow chart has been developed to address the problematic of the cantilever miniaturization, which raised several issues in terms of metal adhesion and electrical contact continuity. These different microfabrication steps are thoroughly detailed with the corresponding development of adapted solutions. The electrical and transduction properties of these devices will also be part of analyses and performance comparisons against the reference polymer cantilever strain sensors described in the previous chapter.

5.1. Microfabrication

5.1.1. Processing of MEMS with SU8 photoresist

The negative tone SU8 epoxy-based photoresist was first introduced by IBM in 1989 (US Patent 4882245 [3]) and reported in peer-reviewed journals in 1995 [4,5]. Subsequently, the first SU8 products were commercialized by MicroChem in 1996 [6]. The SU8 photoresist formulation is typically composed of epoxy oligomers containing

acid-labile groups (i.e. epoxy functionalities) together with photoacid generators. The chemical structure of the SU8 oligomer molecule is illustrated in Fig. 5.1.

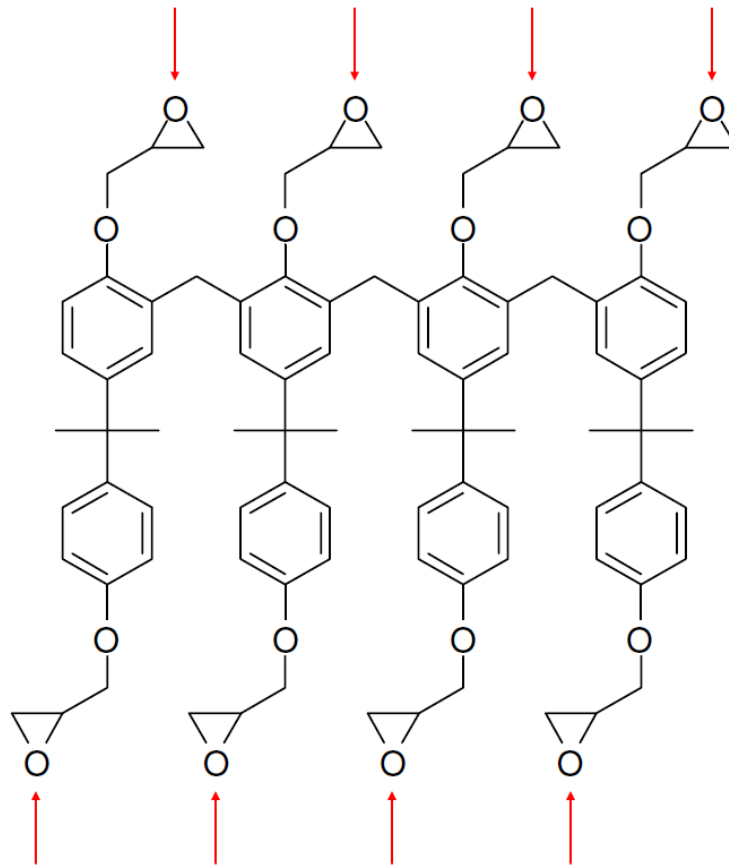


Figure 5.1. Chemical structure of the epoxy oligomer contained within SU8 formulations. Eight reactive epoxy functionalities, indicated by the red arrows, allow a high degree of cross-linking after photoactivation. Adapted from [6].

The photoacid generator contained within the SU8 formulation acts as a catalyst for the cross-linking process. More precisely, when the UV-exposure is performed, the photoacid generator decomposes and further protonates the epoxides functionalities of the oligomer (indicated by the red arrows in Fig. 5.1). Subsequently, upon the application of heat, the protonated ions react with neutral epoxides, resulting in a series of cross-linking reactions [6,7]. Moreover, as observed from Fig. 5.1, the SU8 monomer consists of eight reactive epoxy functionalities per molecule, which allows for a high degree of cross-linking, resulting in high aspect ratio and straight sidewalls after the photothermal activation of the photoresist [6,7]. This dense network provides a high

chemical and thermal stability to the cross-linked SU8 photoresist, together with good mechanical properties. The physical properties of the SU8 photoresist are summarized in Table 5.1.

Property	Value
Young's modulus Y (post bake at 95 °C)	4.02 GPa
Young's modulus Y (hard bake at 200 °C)	4.95 ± 0.42 GPa
Film stress (post bake at 95 °C)	16-19 MPa
Maximum stress (hard bake at 200 °C)	34 MPa
Glass temperature (unexposed)	~ 50 °C
Glass temperature (fully cross-linked)	> 200 °C
Degradation temperature (fully cross-linked)	~ 380 °C
Thermal expansion coefficient (post bake at 95 °C)	52 ± 5.1 ppm.K ⁻¹
Polymer shrinkage upon cross-linking	7.5 %

Table 5.1. Physical properties of the SU8 photoresist. Reproduced from [7].

These reported physical properties show the importance of the respective lithography steps in the SU8 properties, as the glass transition temperature is increased from approximately 50 °C to temperatures over 200 °C between the unexposed and fully cross-linked SU8 photoresist, respectively. The different lithography steps of SU8 processing and their respective goal and impact are further detailed in section 2.2.2 of chapter 2, consisting of the successive realization of the SU8 spin coating, its soft baking, UV-exposure, post exposure baking, development and hard baking. Several SU8 formulations are readily available, resulting in thicknesses ranging from 500 nm to values superior to 200 μm [8–10]. The corresponding spin coating parameters, bakes durations, exposure dose and development time thus need to be adjusted appropriately, depending on the resist dilution, viscosity and the targeted thickness [6].

Most importantly, the exposure dose applied during the UV-exposure of the SU8 is a critical factor, which determines the quantity of catalytic acid generated within the exposed areas of the photoresist. R. Daunton et al. [11] evidenced the impact of the exposure dose on the patterned SU8 edges. If the exposure dose is too low, not

enough acid will be generated for the cross-linking at the bottom of the SU8 film, which results in a phenomenon of undercutting, as illustrated in Fig. 5.2(a) and Fig. 5.2(b) [11]. On the contrary, if the exposure dose is too high, the top of the SU8 film will form an area of higher cross-link density after the post exposure bake, resulting in a t-topping sidewall profile, as illustrated in Fig. 5.2(c) and Fig. 5.2(d) [11].

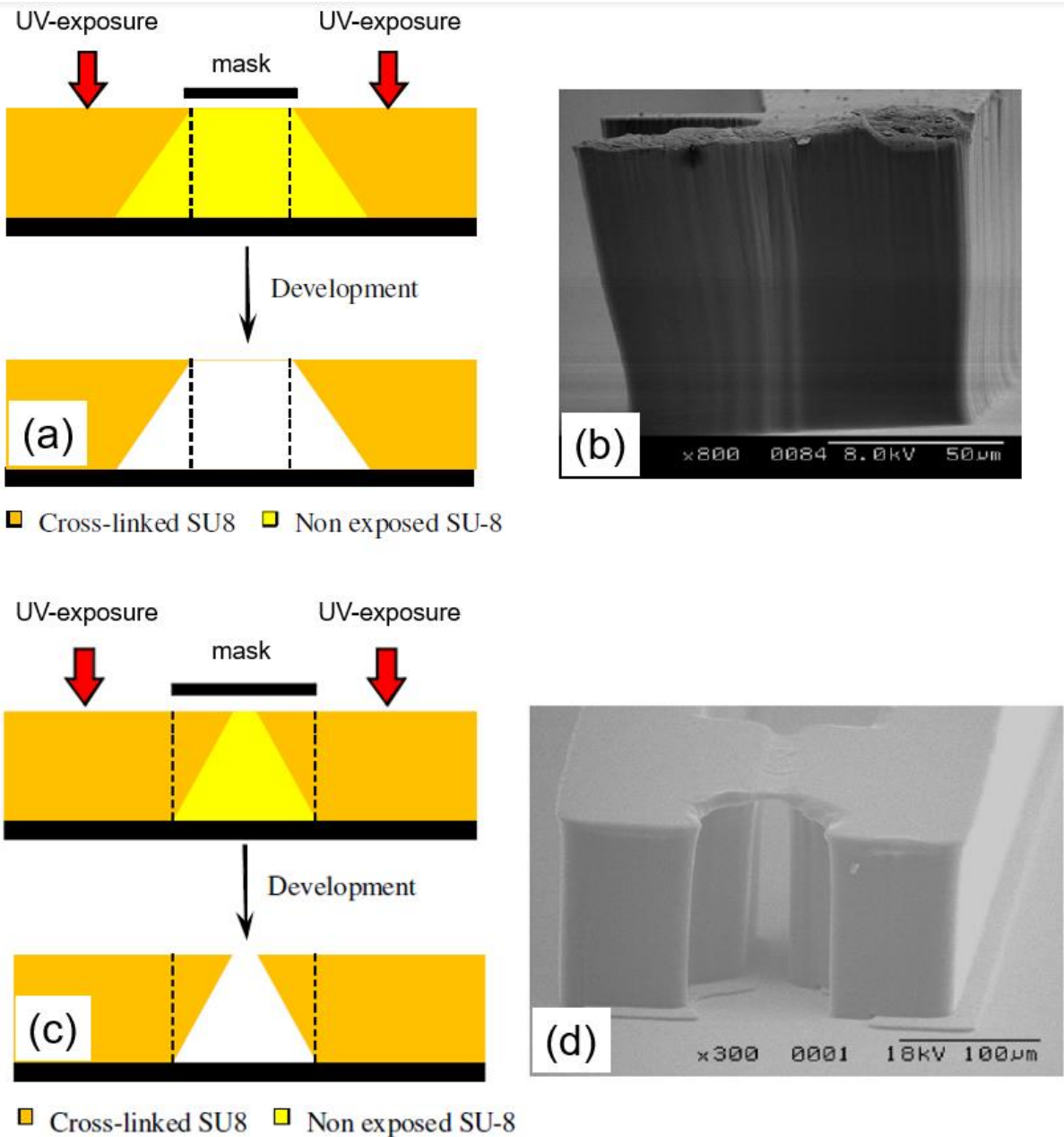


Figure 5.2. (a) Illustration of the undercutting effect after underexposure of a SU8 layer. (b) Corresponding SEM image of undercutting and feature collapse due to underexposure. (c) Illustration of the t-topping effect after overexposure of a SU8 layer. (d) Corresponding SEM image of fused features due to overexposure. Reprinted from [11].

Moreover, in the case of thick SU8 resist films, a minimum exposure dose is required to fully expose the SU8 layer. Therefore, the exposure dose needs to be determined carefully and adjusted as a function of the SU8 film thickness.

Owing to its unique features, the SU8 photoresist democratized the processing of MEMS structures by conventional lithography [10] without the constraints of wet etching and releasing harsh chemistry used for silicon based structures. On the one hand, the Young's modulus of the SU8 photoresist (i.e. 4.95 GPa) is high enough to ensure the mechanical stability of MEMS structures and devices. On the other hand, its value is substantially lower compared to Si (i.e. 190 GPa), which allows for the processing of either thicker cantilevers with similar stiffness of equivalent thickness cantilevers but with a substantial reduction of the stiffness to obtain more flexible structures. Consequently, the low Young's modulus of SU8 photoresist makes it an ideal candidate for the processing of microcantilevers adapted for scanning probe applications, allowing higher sensitivities and further degrees of freedom in the dimensioning when compared to commercial Si microcantilevers.

Most notably, G. Genolet et al. (IBM labs, Zurich) introduced in 1999 the concept of plastic MEMS by the mean of SU8 microstructuring to realise probes for scanning force microscopy (SFM), as depicted in Fig. 5.3 [12]. This work paved the way towards the microprocessing of MEMS and microcantilevers with SU8 photoresist dedicated to scanning probe applications (e.g. surface stress measurements).

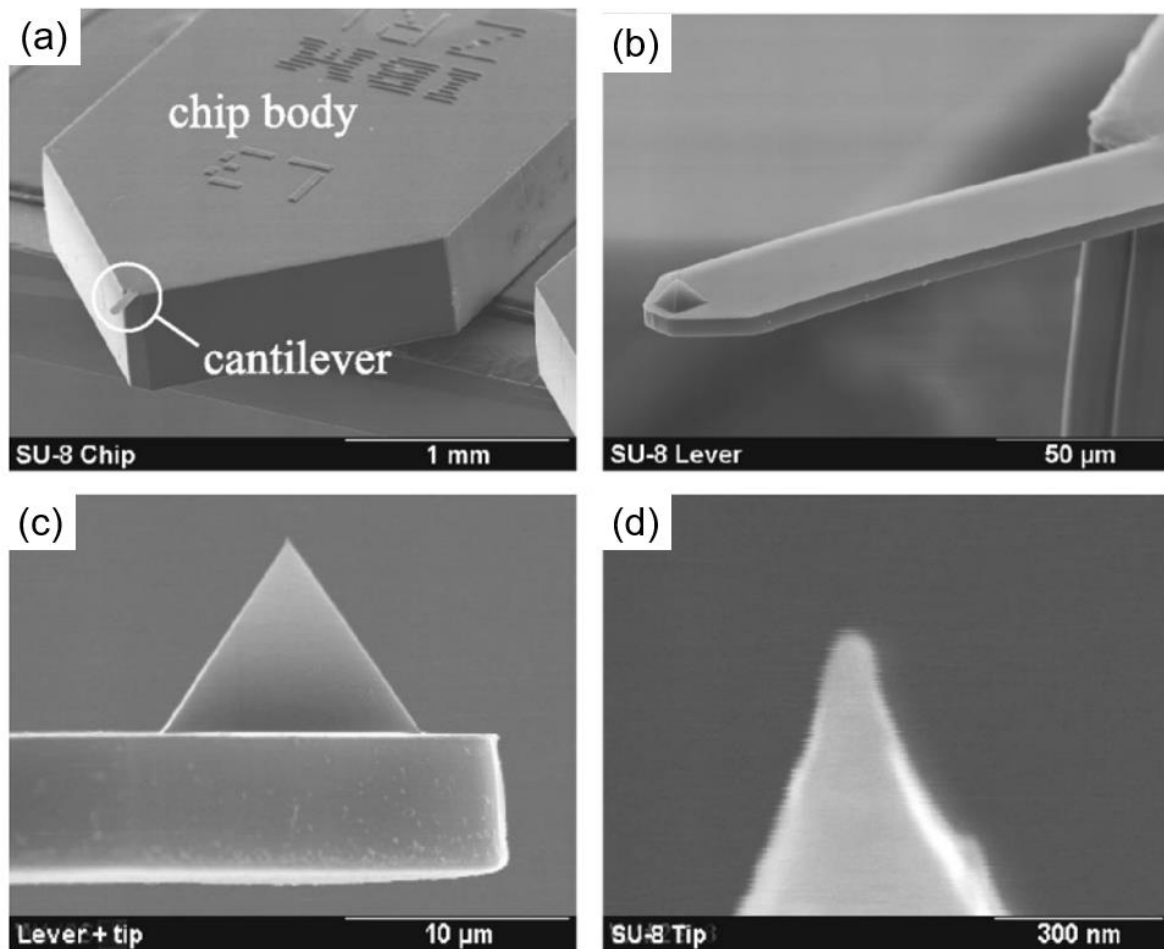


Figure 5.3. Photoplastic SU8 microcantilever for AFM operation proposed by G. Genolet et al. [12]. (a) General view of an SU8 SFM probe. (b) Close up of an SU8 cantilever. (c) Close-up of a pyramidal tip at the end of the cantilever. (d) Enclosed view of an SU8 pyramidal tip. The radius of curvature corresponding to the cantilever's tip is approximately 30 nm. Reprinted from [12].

Within this scope, A. Johansson et al. part of the group of Anja Boisen (DTU, Technical University of Denmark), proposed in 2005 the processing of SU8 microcantilevers integrating piezoresistive strain gauges for detection of surface stress changes, as illustrated in Fig. 5.4 [13].

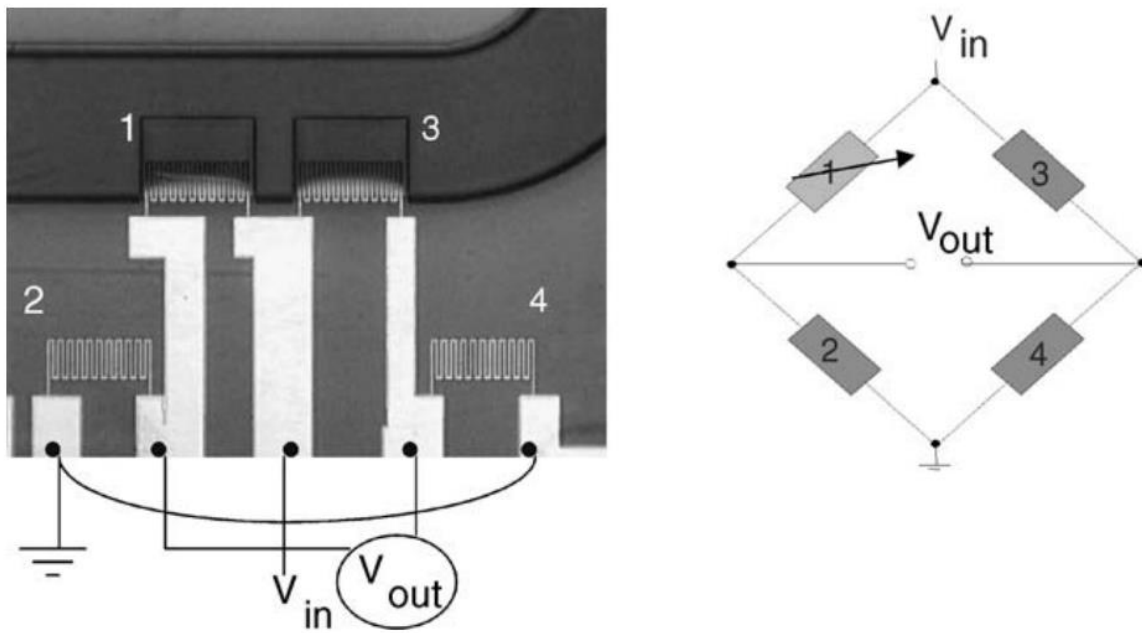


Figure 5.4. SU8 microcantilevers integrating piezoresistive strain gauges proposed by A. Johansson et al. [13]. Two cantilevers in the channel are connected to two on-chip resistors forming a Wheatstone bridge. The induced strain by deflection of the cantilever is detected as a change in output voltage. Reprinted from [13].

More recently, Hana Han et al. (ETH Zürich) proposed a more sophisticated SU8 hollow cantilevered structure integrating a microfluidic channel with a silver nanowires piezoresistive strain gauge [14], as depicted in Fig. 5.5. The force feedback provided by the piezoresistive strain gauge allows force spectroscopy operation on a hard surface as well as on soft objects such as cells.

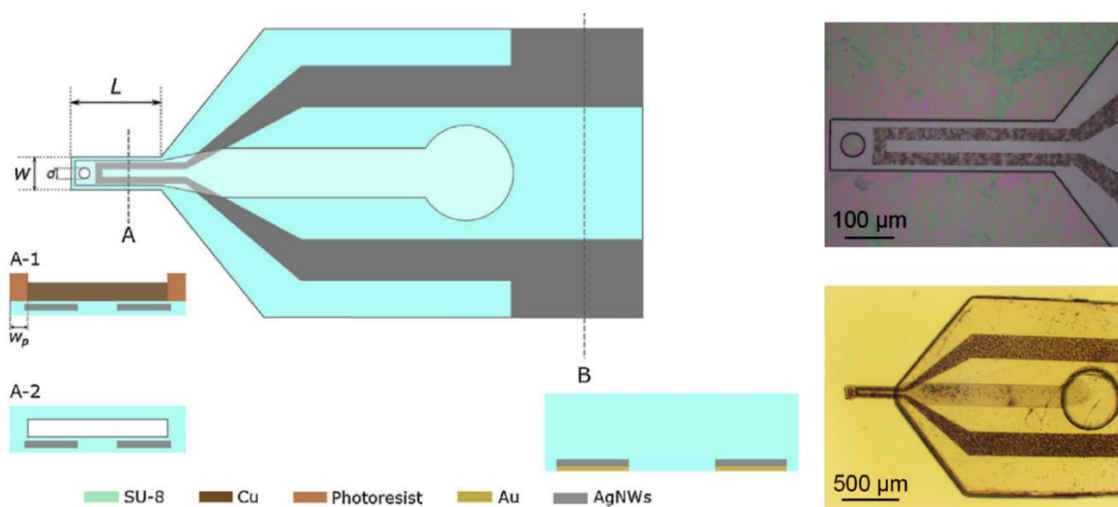


Figure 5.5. SU8 microcantilevers integrating a microfluidic channel and a silver nanowires piezoresistive strain gauge proposed by H. Han et al. [14]. The induced strain by deflection of the cantilever is detected as a change in the strain gauge resistance.

This work further demonstrates the compatibility of the SU8 photoresist with MEMS dedicated to strain sensing applications, with a successful integration of strain sensors into SU8 microcantilevers. Moreover, the processing of SU8 by photolithography allows for a cost-effective microfabrication method with a relative ease of implementation. These reasons thus highly motivated our choice to integrate our piezotronic sensors with SU8, where the photoresist was used both for the microcantilevers but also as the main building block of the sensor (i.e. the chip body). Nonetheless, the composite integration of inorganic thin films structure in a SU8 body raises several difficulties of interfacial compatibility of materials within the different microfabrication steps. Within this chapter, we thus present this study aimed at reducing the size of the developed piezotronic sensors with adapted solutions for their integration in microcantilevers within a full-SU8 body.

5.1.2. Control of ZnO thin deposition by ALD on SU8 photoresist

The ALD processing of the ZnO thin layer has been initially developed on a reference silicon substrate, and further transferred to polyimide and platinum substrates for the first generation of sensors. Concerning the miniaturization of the polymeric cantilevered strain sensors, the SU8 has been used as a substrate, which is an epoxy-based negative photoresist layer as described in the previous section. As the ALD technique is based on surface reactions for the deposition of thin films onto a substrate, changing the substrate thus consists in a major challenge. An important technical requirement is related with the deposition temperature of the ALD process, in order to avoid the degradation of the substrate. Because the glass transition temperature of SU8 after cross-linking is located around 200 °C, with a corresponding degradation temperature located around 380 °C [15], subsequent ALD processes should be performed below this temperature to prevent reflow and outgassing phenomena. Additionally, prior to the deposition of the ZnO thin film, a plasma pre-treatment was applied on the SU8 surface, consisting in a soft oxygen/argon plasma. The aim of this pre-treatment is to increase the wettability of the top surface of the photoresist by inducing surface oxidation. However, the oxygen contained within the plasma has a

meaningful etching effect on the polymeric substrates. An appropriate set of plasma parameters (power, time, flow of gases, reactor pressure) thus had to be found to achieve an adequate surface activation while preventing a significant etching of the resist. Moreover, the deposited ZnO thin films on SU8 should maintain similar structural and electrical properties when compared to the reference silicon, polyimide and platinum substrates, for further benchmarking with the polyimide cantilevered strain sensors described in the previous chapter. Consequently, in order to validate the transfer of the ZnO thin film from the reference substrates to SU8, structural and electrical characterizations of ALD-grown ZnO thin films on a SU8 thin film were performed, with deposition temperatures ranging from 60 °C to 100 °C. Within this scope, a 500 nm thick SU8 layer was spin coated on Si substrates. These characterizations were compared with ZnO thin films grown on Si substrates during the same ALD processes. The obtained cross-sectional SEM micrographs, XRD diffraction patterns and resistance values are presented in Fig. 5.6, Fig. 5.7 and Fig. 5.8, respectively.

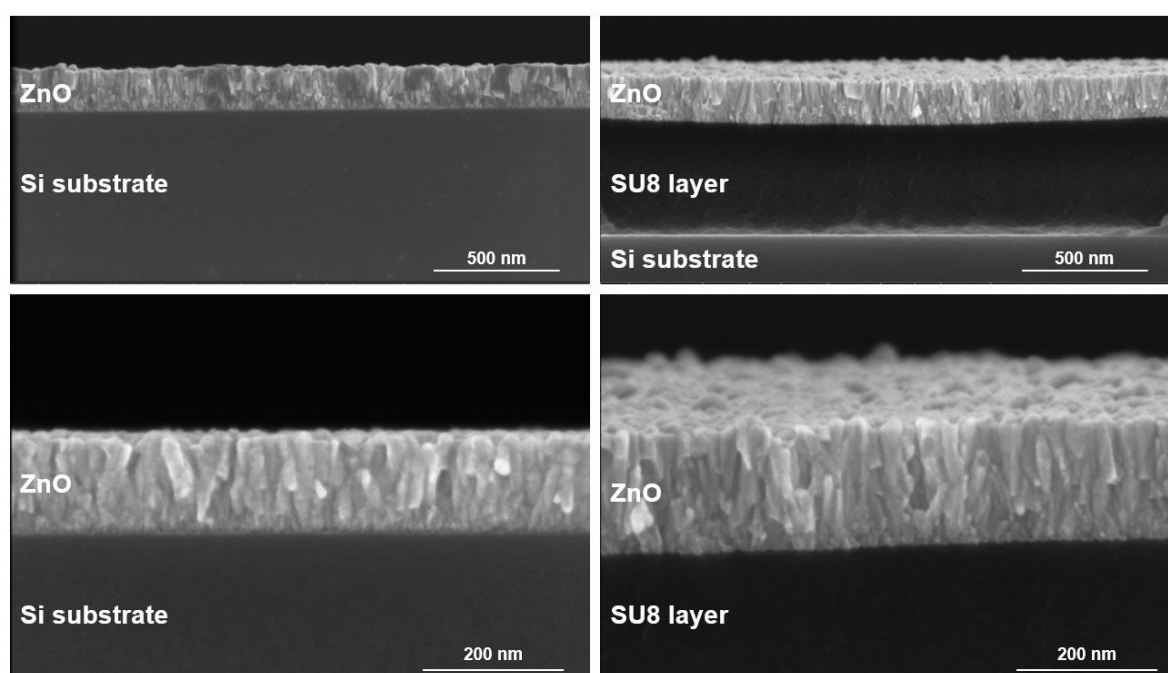


Figure 5.6. Cross-sectional SEM pictures of ZnO thin films deposited at a temperature of 80 °C on Si wafer substrates (left) and on a thin layer of SU-8 (right).

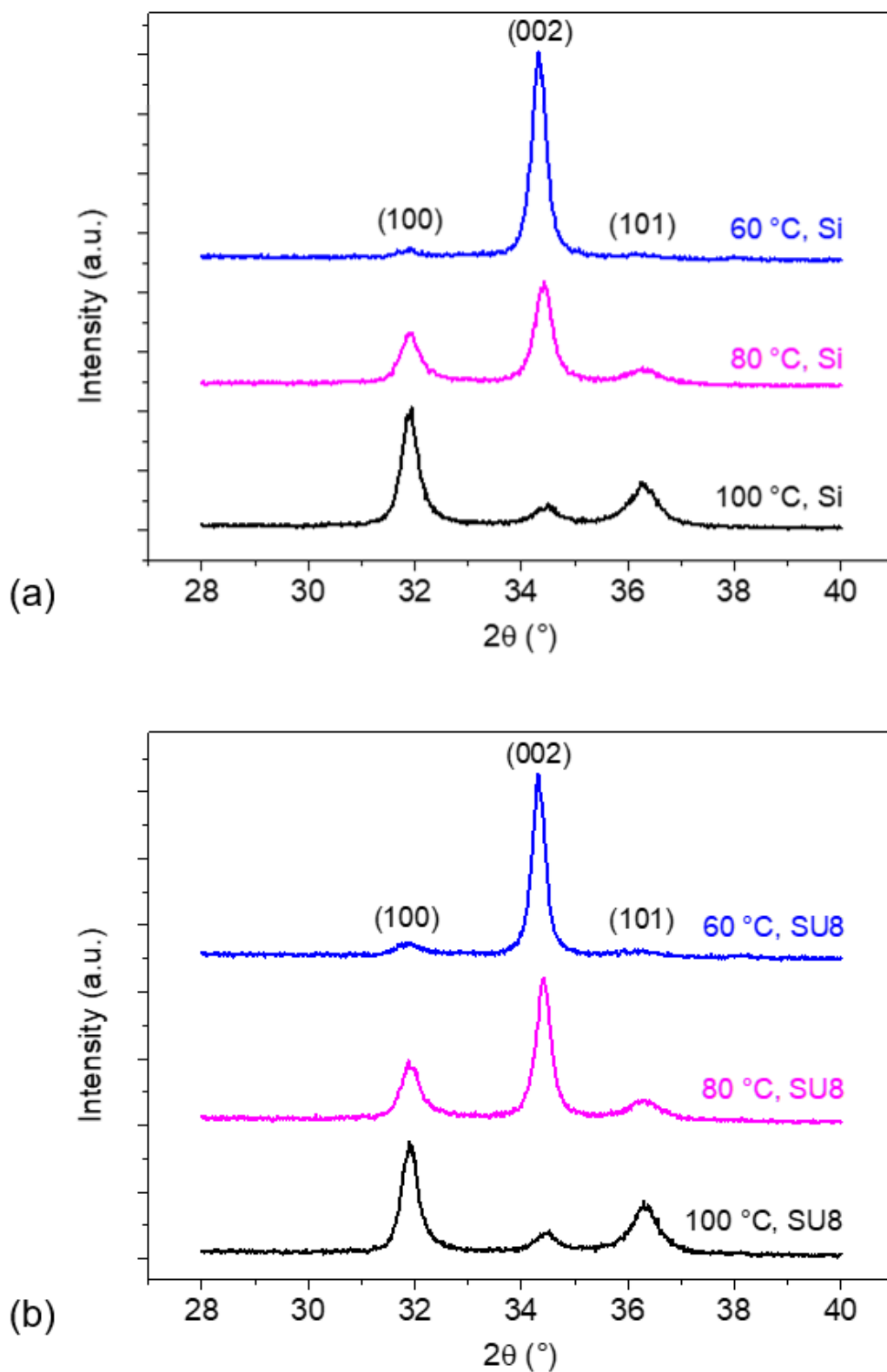


Figure 5.7. GI-XRD diffraction patterns ($\omega=0.3^\circ$) of ZnO thin films grown on (a) Si wafer substrates and on (b) a thin layer of SU8.

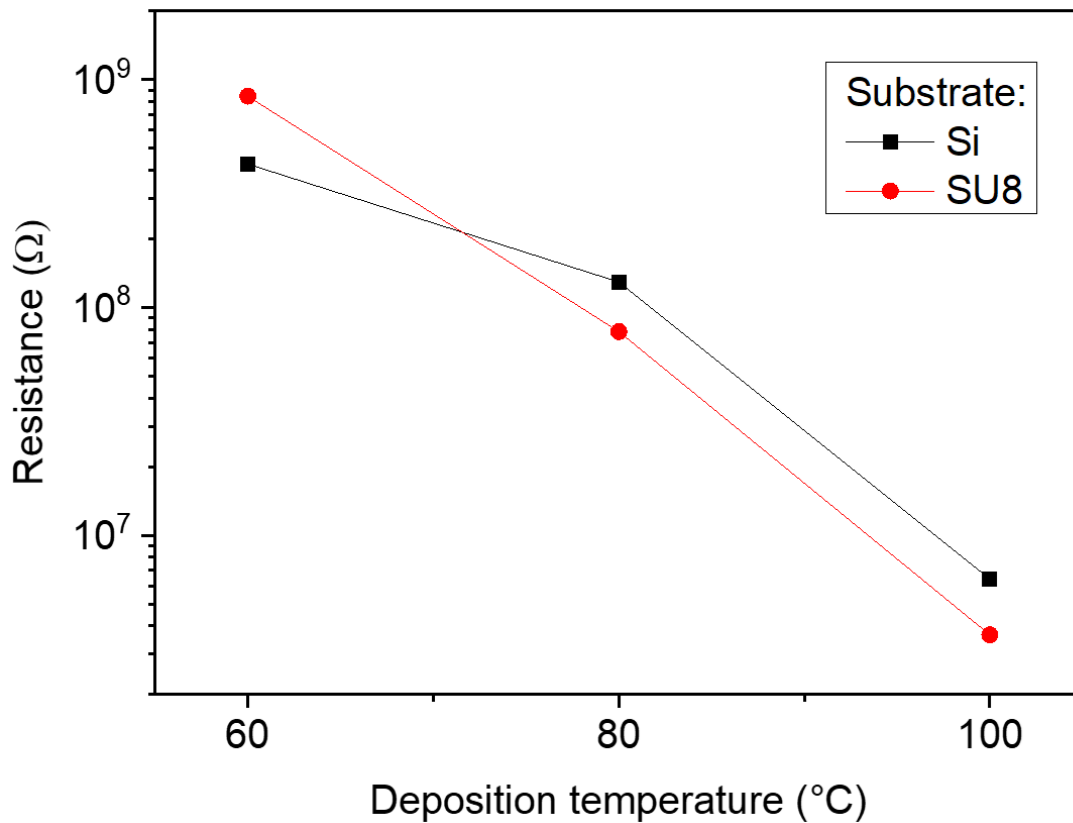


Figure 5.8. Evolution of the resistance of ZnO thin films grown by ALD for different deposition temperatures on Si wafer substrates and on SU8 surfaces.

As observed on the figures above, both the structural and electrical properties of the ZnO thin films deposited on silicon and SU8 are extremely similar, which validates the transfer on the zinc oxide growth by ALD on the polymeric SU8 substrate.

5.1.3. Design

As mentioned earlier, this new generation of sensors relies on the miniaturization of the sensitive area composed of the Pt metal electrodes, the ALD-grown ZnO thin film and the SU8 cantilever. It should be noted that the dimensions of the chip body remained unchanged compared to the polyimide strain sensors, to allow for an easy manipulation. A comparison between the SU8 and polyimide sensors is provided in Fig. 5.9, which illustrates the substantial reduction in their respective cantilevers' dimensions.



Figure 5.9. Visual comparison between the full-SU8 body (left) and the polyimide (right) piezotronic strain microsensors. The white arrows indicate the two microcantilevers integrated in the full-SU8 body. The scale bar represents 2 mm.

The miniaturization of the strain sensors' cantilevers makes them more prone for AFM scanning probe operations with higher strain sensitivity. The designed SU8 microcantilevers have dimensions comparable with commercial Si cantilevers [16], as depicted in Fig. 5.10(a). Additionally, a sketch of the sensitive area, consisting of the Pt interdigitated electrodes and the ZnO pad embedded at the clamped area of the SU8 cantilever is shown in Fig. 5.10(b). It should be noted that the sensor displayed in Fig. 5.10(a) was processed at an early stage of this project, where the sensor design, and more precisely the positioning of the Pt IDE and the ZnO thin film was further modified. As the whole SU8 structure is defined by maskless laser photolithography processes and further released by the etching of a sacrificial layer, no manual operation is performed that could induce mechanical damage to the structure. Consequently, the sensitive area was displaced entirely on the cantilever after the clamped area.

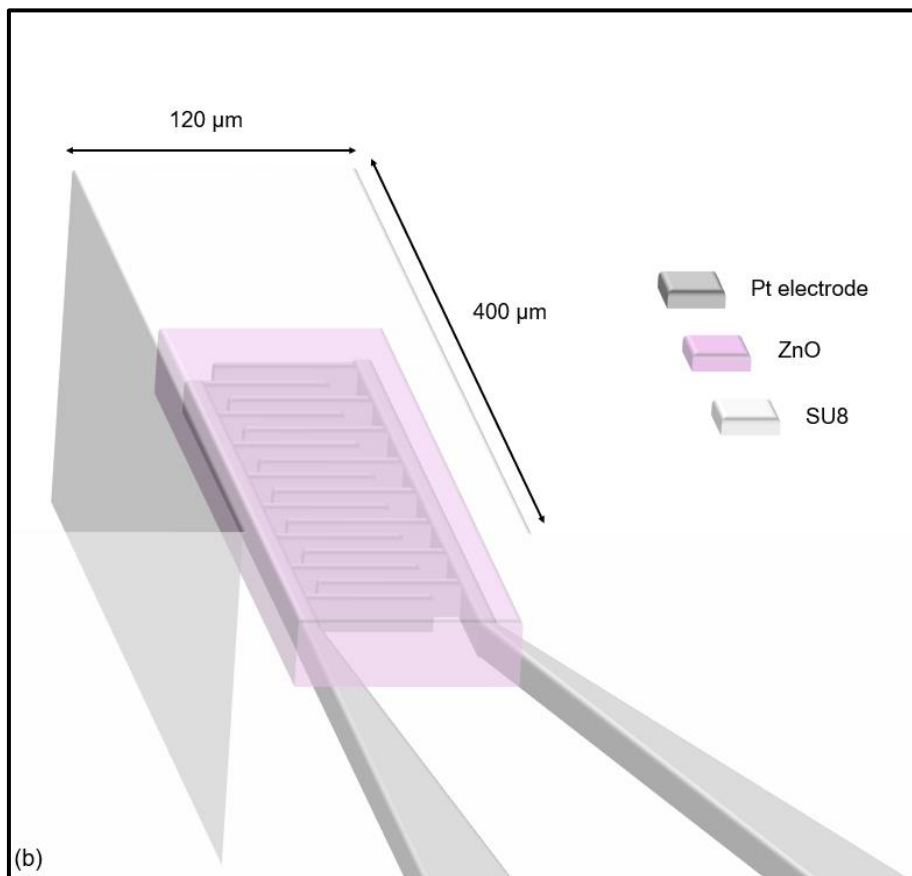
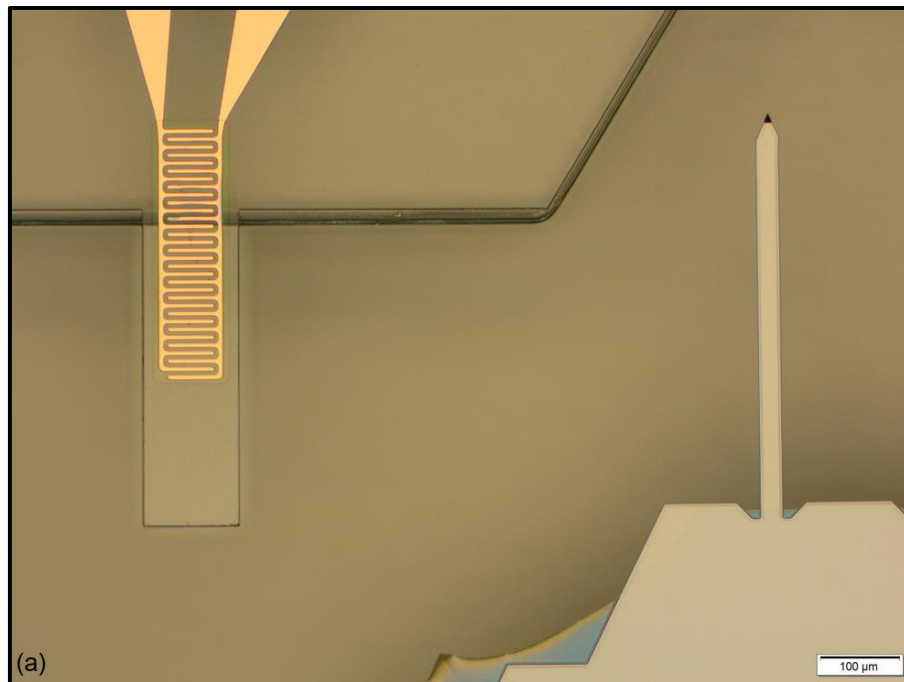


Figure 5.10. (a) Enclosed view on the micro-cantilever (on the left of the picture), where the Pt metal electrodes and the ZnO deposited by ALD are embedded within the SU8 polymer body. The SU8 cantilever dimensions are comparable with a commercial Si cantilever [16] (on the right of the picture). (b) Sketch of IDE electrode configuration at the sensitive area, embedded within the SU8 cantilever. Not to scale.

Similar to the polyimide cantilevers, the dimensioning of the SU8 cantilevers must be considered carefully to maintain their stiffness inferior to 10 N.m^{-1} close to standard silicon-based cantilevers used for AFM operation. The same method described in the previous chapter was applied to the SU8 cantilevers, where the stiffness k of a cantilever is denoted as follows:

$$k = \frac{Y \cdot w \cdot t^3}{4 \cdot L^3} \quad (5.1)$$

Where Y is the Young's modulus of the SU8 cantilever, L is the length, w is the width and t is the thickness of the cantilever. With the corresponding numerical values linked with the SU8 cantilevers properties ($Y = 4.95 \text{ GPa}$) and dimensions detailed on Fig. 5.10(b), with a body thickness of $12.5 \mu\text{m}$, the numerical application yields:

$$k = \frac{(4.95 \times 10^9) \cdot (120 \times 10^{-6}) \cdot ((12.5 \times 10^{-6})^3)}{4 \cdot ((400 \times 10^{-6})^3)} = 4.53 \text{ N.m}^{-1}$$

The obtained stiffness value for the SU8 cantilevers is thus adapted for AFM scanning probe applications in contact mode such as force spectroscopy or imaging [16].

Additionally, the strain ε generated in the clamped area of the cantilevers was calculated using the following equation [17] :

$$\varepsilon = \frac{3}{2} \cdot \frac{(t - t_s)(2L - L_s)}{L^3} \cdot d \quad (5.2)$$

With t and L having the same meaning as before, t_s being the sensor thickness, L_s the sensor length, and d the deflection imposed on the cantilever relative to the contact point (at length L). Consequently, the strain ε generated in the clamped area of the SU8 cantilevers has been calculated with equation 5.2 as a function of deflections values ranging between 1 nm and 1 cm . Due to the miniaturization of the SU8 cantilevers' dimensions, a deflection imposed at the tip of the SU8 cantilever at a length $L = 400 \mu\text{m}$ was considered. The resulting values are presented in Fig. 5.11, using t_s

as 400 nm and L_s as 350 μm , and compared to the strain ε generated at the tip end of the polyimide cantilevers introduced in the previous chapter 4 for the same imposed deflections.

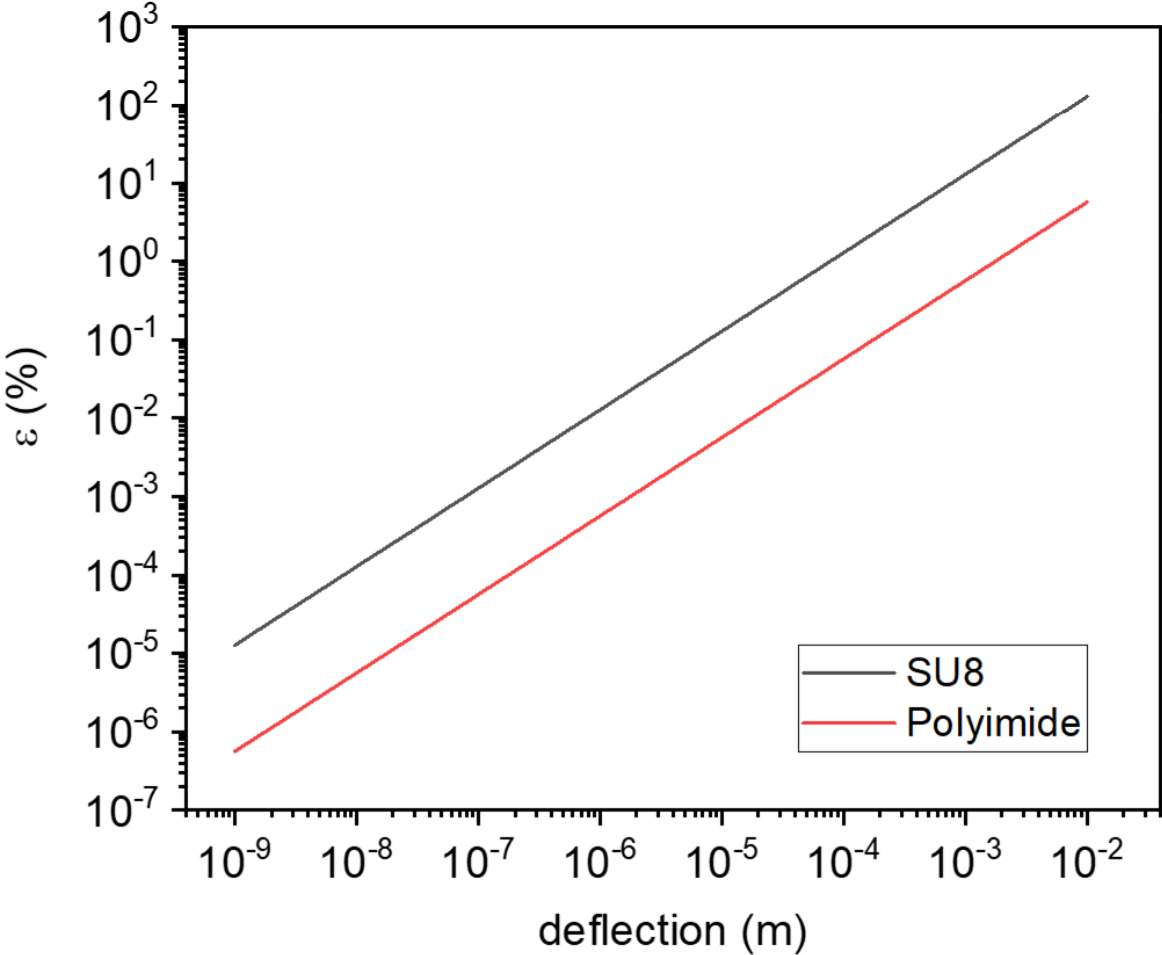


Figure 5.11. Log-log plot of the calculated strain ε generated in the clamped area of SU8 and polyimide cantilevers as a function of deflections values imposed at the cantilever's tip, ranging between 1 nm and 1 cm.

As observed from Fig. 5.11, the miniaturization of the SU8 cantilevers dimensions substantially increases by more than one order of magnitude the strain generated at the clamped area when compared to the polyimide cantilevers, for the same imposed deflections. This results in an enhancement of the strain sensitivity, as the full-SU8 body piezotronic strain microsensors are more prone to detect and to be actuated by lower cantilever's deflection.

5.1.4. Process flow

The microfabrication process flow of the full-SU8 body piezotronic strain microsensors, with the interdigitated platinum electrodes and the ALD-grown ZnO thin film depositions is illustrated in Fig. 5.12.

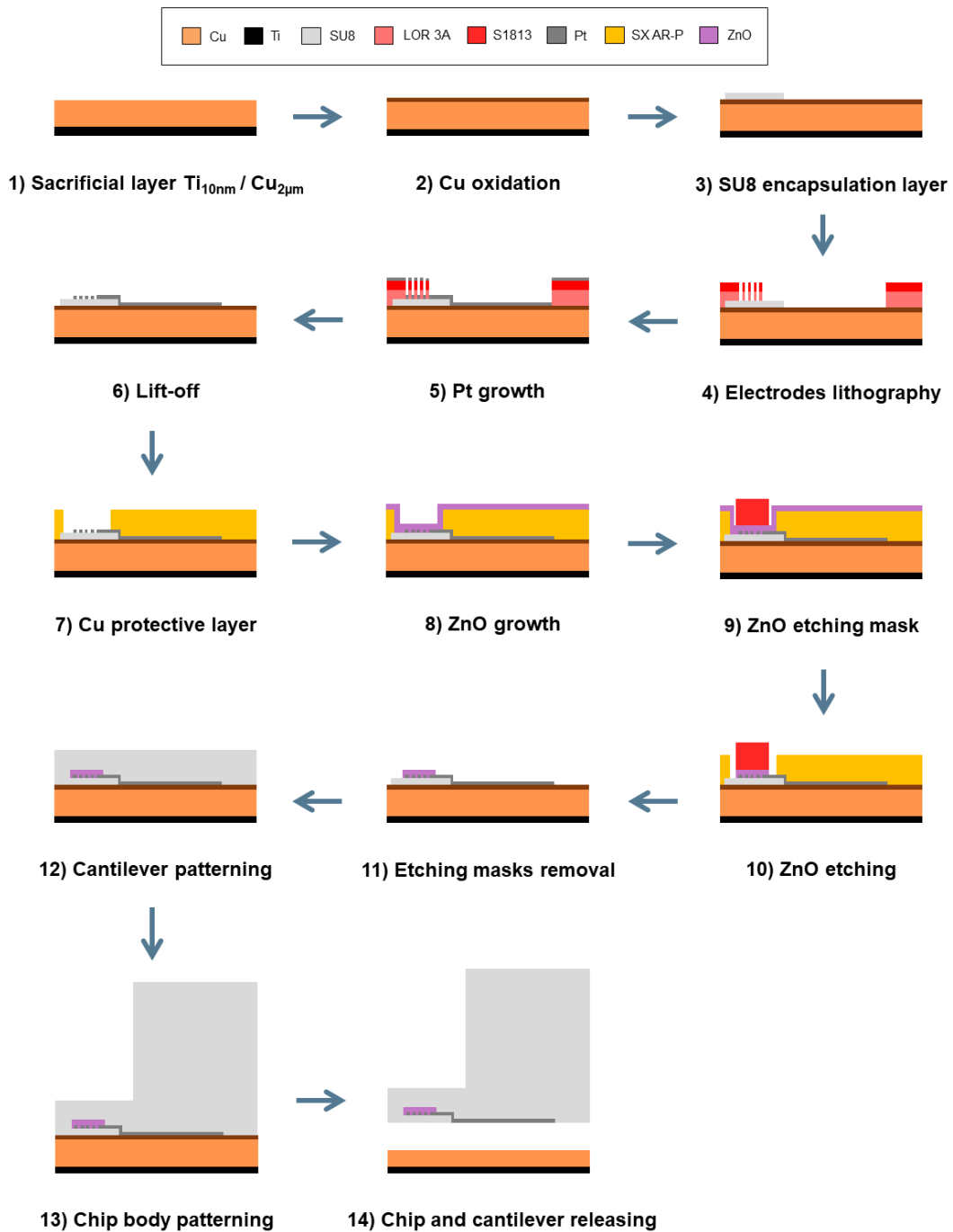


Figure 5.12. Microfabrication process flow chart corresponding to the full-SU8 body piezotronic strain microsensors.

The approach taken for the microfabrication process flow of the full-SU8 body piezotronic strain microsensors is completely different from the polyimide sensors, with a reversed processing. The whole structure is built upon a copper sacrificial layer, where the release is performed via the wet etching of this sacrificial layer. Consequently, the full-SU8 body sensors' microfabrication is performed upside down, starting from the SU8 cantilever and ending with the chip body processing prior to the structure release. The different processing steps are further detailed with the corresponding experimental parameters employed and specific guidelines to follow.

- Sacrificial Cu layer: The full sensor structure was built upon silicon 2 inches wafer (Siegert Wafer, Germany) coated with the sacrificial layer. The wafer is composed of a 279 μm ($\pm 25 \mu\text{m}$) Si substrate, with a 10 nm ($\pm 10 \%$) Ti adhesion layer and the 2 μm ($\pm 5 \%$) Cu sacrificial layer.
- Cu oxidation: A soft thermal oxidation was performed on the Cu surface on a hotplate at 180 °C, for a duration ranging from 2 minutes up to 5 minutes. Copper oxide (CuO) presents a roughened surface morphology, increasing the wettability and the adhesive strength at its interface with subsequent material deposition [18]. This oxidation of the Cu sacrificial layer thus allows for a better adhesion of the SU8 encapsulation layer deposition. The oxidation was assessed visually and stopped when the Cu sacrificial layer was turning to a brown/orange colour, as depicted in Fig. 5.13.

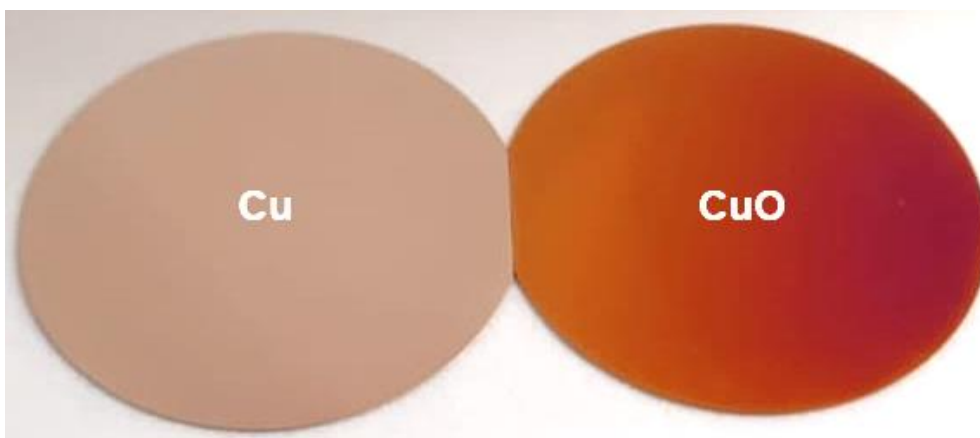


Figure 5.13. 2 inches Si wafers used within the microfabrication processing. The bare Cu sacrificial layer and its oxidized surface are displayed on the left and right-hand side of the picture, respectively.

- SU8 encapsulation layer: A first SU8 500 nm thin layer, acting as a ZnO passivation layer, was patterned upon the sacrificial layer. As described in the previous chapter, it should be noted that the different bakes described in the following microfabrication steps were performed with temperature ramps to avoid thermal shocks and subsequent cracking, ramping from room temperature up to the desired value and vice-versa. SU8 2000.5 photoresist was thus spin coated on the sacrificial layer (step 1: 500 rpm, 300 rpm.s⁻¹, 5 s - step 2: 10000 rpm, 500 rpm.s⁻¹, 45 s), followed by the photoresist soft baking (95 °C, 60 s, 350 °C.h⁻¹). The SU8 layer was then UV-exposed by direct laser lithography (dose: 6000 mJ.cm⁻², defocus: +25). Subsequently, the post exposure baking was performed (same conditions as the soft baking), followed by the development (60 s) with SU8 developer (PGMEA), rinsing in IPA (15 s) and the hard baking (180 °C, 30 min, 350 °C.h⁻¹).
- Electrodes lithography: Interdigitated electrodes and contact pads were patterned by lift-off lithography, by using a LOR 3A (MicroChem™) / S1813 (Microposit®) photoresist bi-layer. The 350 nm thick LOR 3A layer was spin coated (6000 rpm, 4000 rpm.s⁻¹, 30 s) and baked (140 °C, 6 min) on the both the Cu sacrificial layer and the SU8 encapsulation layer. Thereafter, the 1.3 μm thick S1813 layer was spin coated (6000 rpm, 4000 rpm.s⁻¹, 60 s) and baked (115 °C, 60 s, 350 °C.h⁻¹), followed by its UV-exposure and patterning (dose: 91 mJ.cm⁻², defocus: -3) by direct laser writing lithography and the bi-layer development (60 s) in a MF-319 (Microposit®) solution.
- Pt growth: Prior to the Pt metal electrodes deposition, the substrate and resist bi-layers were exposed to a plasma treatment (45 mTorr, Ar - 20 sccm, 50 W, 5s) to improve the adhesion of metal to SU8. The duration of the plasma was purposely set to a few seconds to avoid the etching of the SU8 encapsulation layer. The electrodes and contact pads of platinum (100 nm) were evaporated by EBME. The metal evaporations were performed in the 10⁻⁸ mbar range, with an average current of 580 mA, while maintaining a constant deposition rate of 1.5 Å.s⁻¹.

- Lift-off: The lift-off process was carried out by immersing the wafer in a bath of Remover PG (MicroChem™) solvent for approximately 10 minutes. It was then rinsed with Remover PG, acetone and isopropanol.

A highly critical point of the process described in the flow chart is to keep the subsequent evaporated platinum continuity between the sensing interdigitated electrodes located on the SU8 encapsulation layer and the large bounding pads on the copper sacrificial layer, for subsequent access to wire bonding. This difficulty is similar as the one faced for the top-bottom electrode configuration described in chapter 4, where the 500 nm abrupt step at the SU8 encapsulation layer edge might induce a rupture of the electrical continuity of the stepped electrode, as illustrated in Fig. 5.14(a). Furthermore, it should be noted that the exposure of the SU8 photoresist is different from the situation illustrated in Fig. 5.2, as the exposure is performed without a mask by the means of a laser, typically focused on the top surface of the SU8 layer. This issue was thus solved by taking advantage of the maskless aligner capabilities to shift the laser focalisation point by several microns from the resist surface (indicated by the defocus value in the description of the different microfabrication steps). More precisely, the defocus value allows to shift the focus position of the write head with respect to the defocusing range. When defined as zero, the focus is performed on the top surface of the photoresist layer. A positive defocus value will consequently shift the focalisation downwards (i.e. inside the photoresist), where a defocus value of 1 corresponds to an approximate shift of 500 nm. Some minor changes of the defocus values might be necessary to adapt the focus distance depending on the photoresist thickness. However, in our case, the defocus value was set to a large positive value of +25 for the exposure of the SU8 encapsulation layer, consequently shifting the focus position to several microns downwards inside the Si substrate. This shift of the focus position changes the exposure conditions compared to the initial computer-aided design, especially at the edges of the exposed patterned areas. This results in less defined edges of the SU8 encapsulation layer, where the bottom surface of the SU8 layer will form an area of higher cross-link density compared to its top surface, as illustrated in Fig. 5.14(b).

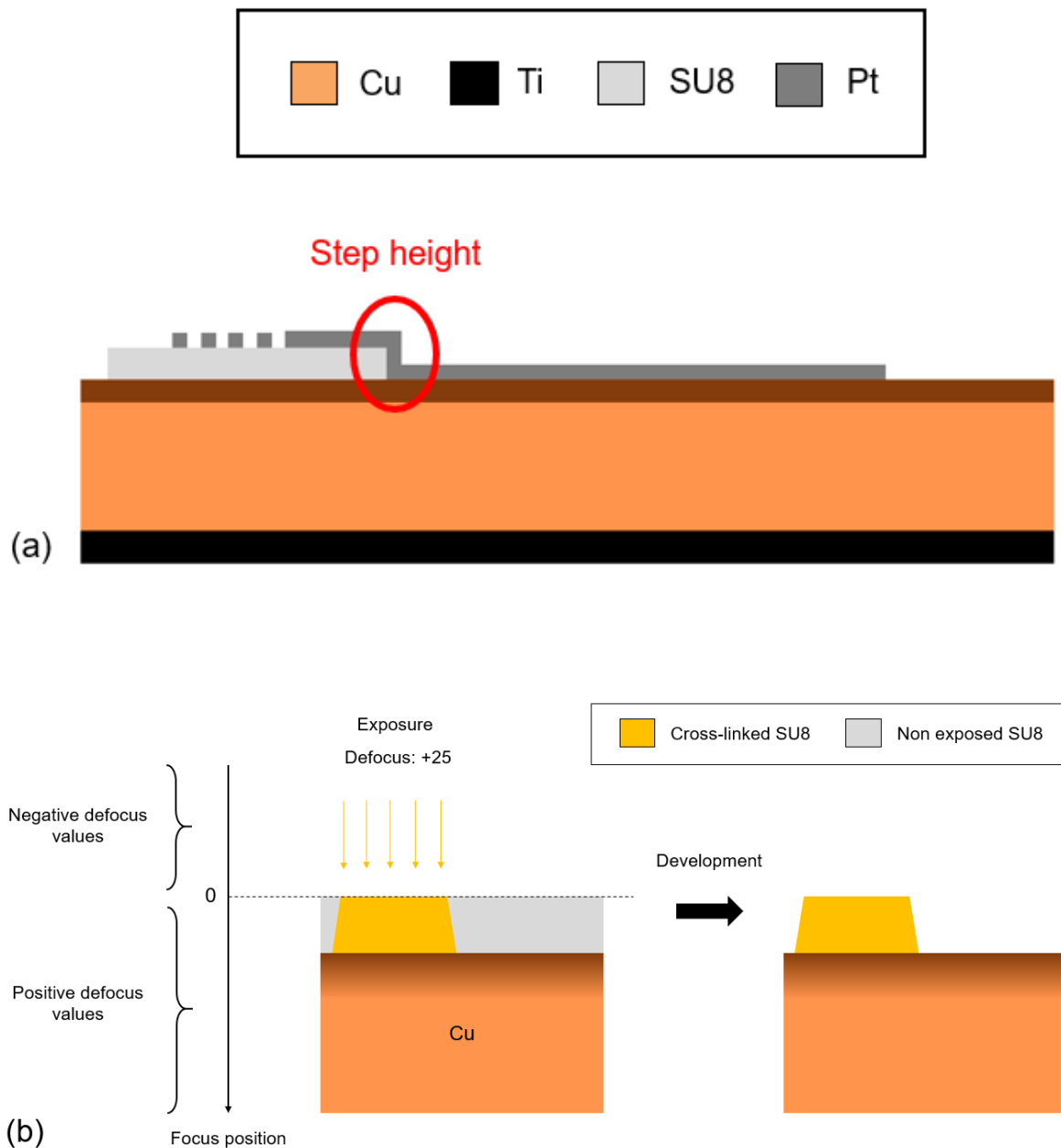


Figure 5.14. (a) Cross-sectional representation of the sensor after lift-off, highlighting the localization of the step height at the SU8 encapsulation layer edge. (b) Illustration of the SU8 trapezoidal edges obtained after development and exposure with a large defocus value. The focus position relative to the defocus values is represented along the vertical axis.

Therefore, this diverted use of the MLA 150 laser lithography defocusing capabilities makes it possible to obtain SU8 trapezoidal edges with high positive slopes, favouring platinum continuity, as shown in Fig. 5.15(a) and Fig. 5.15(b).

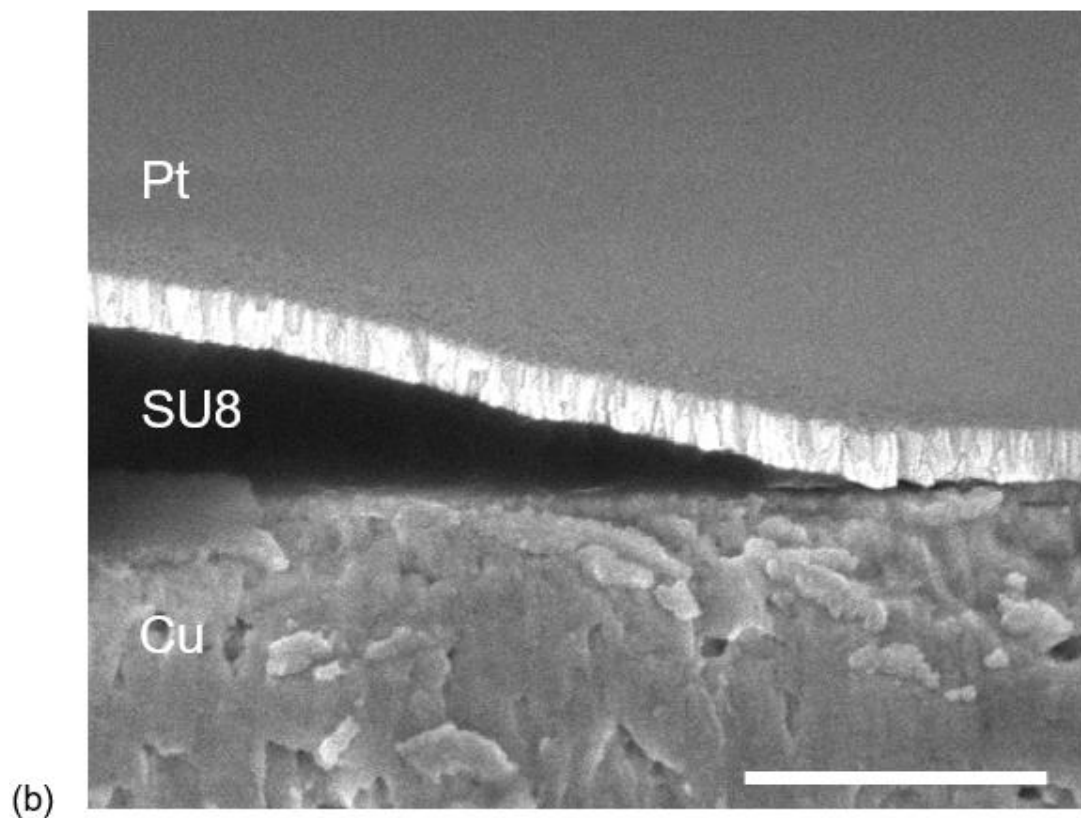
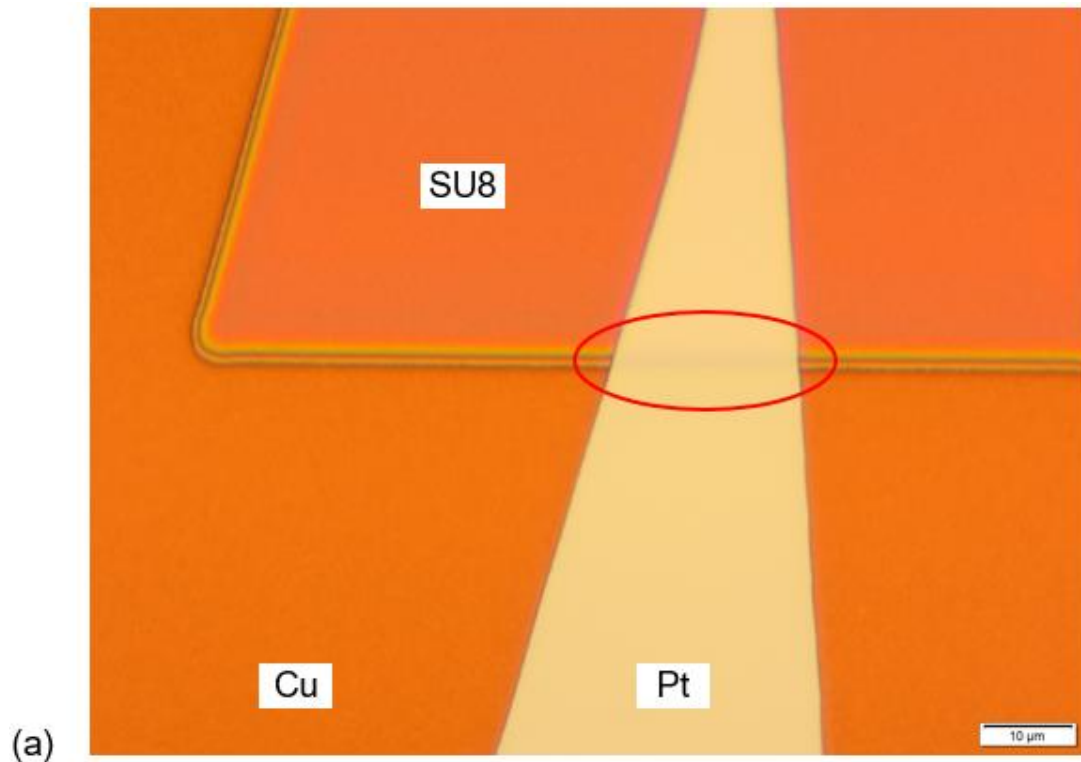


Figure 5.15. (a) Top view showing the continuity of the deposited Pt metal electrodes after lift-off on the SU8 encapsulation layer edge. The obtained high positive slopes via the maskless aligner defocus can be observed at the edge of the SU8 encapsulation layer. (b) Cross-sectional SEM picture, showing the Pt continuity on the SU8 trapezoidal edge. The scale bar corresponds to 500 nm.

- Cu passivation layer: As the copper sacrificial layer is sensitive to the chemical solution used during the subsequent ZnO etching, its surface must be protected. A layer of positive photoresist SX AR-P 3500/8 (Allresist) was thus spin coated (4000 rpm, 2000 rpm.s⁻¹, 60 s) on the entire wafer. Prior to the exposure, the photoresist was left to dry for a day, thus allowing for a natural solvent evaporation of the photoresist, to avoid the generation thermal shocks induced by baking operations. The photoresist was patterned and exposed by direct UV laser writing photolithography (dose: 100 mJ.cm⁻², defocus: -3). Patterns were finally developed in AR 300-35 (Allresist) developer (40 s) and rinsed in deionized water (60 s), thus creating an opening for subsequent ZnO deposition on the area surrounding the Pt IDE, as shown in Fig. 5.16.

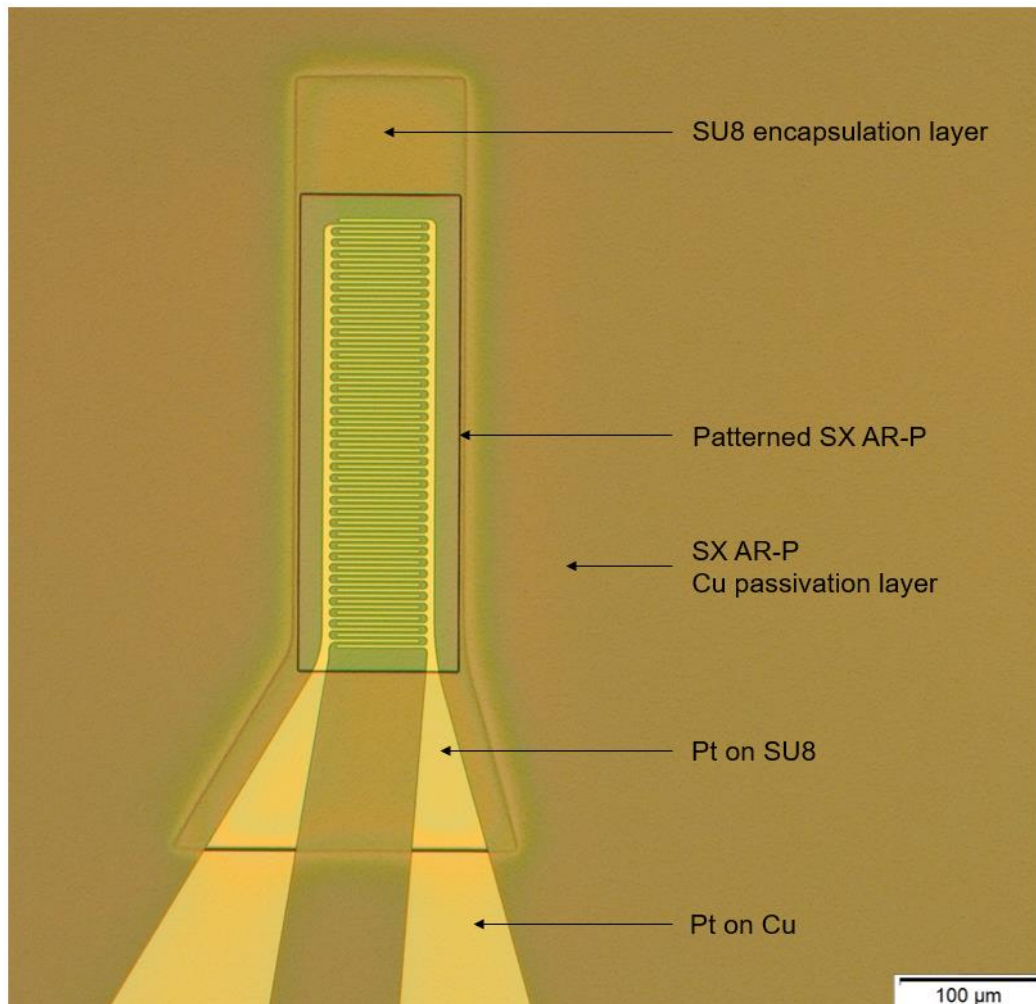


Figure 5.16. Top view showing the sensor structure prior to ZnO deposition by ALD. The SX AR-P photoresist was deposited on the entire wafer to protect the Cu passivation layer from subsequent ZnO chemical etching, while it was etched away as a box around the Pt IDE.

- ZnO growth: Prior to the ZnO thin film deposition by ALD, the wafers were exposed to a soft oxygen/argon plasma pre-treatment (60 mTorr, O₂ - 38 sccm, Ar - 2 sccm, 50 W, 20 s) to remove organic residues from the electrode surface and ensure good ZnO/Pt and ZnO/SU8 interfaces quality. As illustrated in Fig. 5.16, on the one hand, the ZnO thin film will be deposited on the entire wafer onto the SX AR-P photoresist. This area of the ZnO thin film deposited onto the SX AR-P photoresist will be further etched away by wet chemical etching. On the other hand, the ZnO thin film will be deposited on the patterned area of the Cu passivation layer, directly on the Pt IDE and the SU8 encapsulation layer, which corresponds to the sensitive area of the sensors. A 300 nm layer of ZnO was then grown by ALD on the whole substrate surface, at deposition temperatures of 60 °C and 80 °C. Temperature ramps of 50 °C.h⁻¹ were imposed during the heating of the ALD reactor up to the desired deposition temperature value and cooling down to room temperature, in order to avoid the generation of thermal shocks.
- ZnO etching mask: ZnO micropads in the sensitive area were defined by chemical wet etching through a resist mask. The resist mask consisted of a spin coated 1.3 μm S1813 photoresist layer (step 1: 100 rpm, 300 rpm.s⁻¹, 5 s - step 2: 2000 rpm, 2000 rpm.s⁻¹, 30 s), left to dry for a day to avoid baking operation. Thereafter, the photoresist was exposed and patterned on the sensitive area by direct laser writing photolithography (dose: 200 mJ.cm⁻², defocus: -3) and developed (60 s) in a MF-319 solution.
- ZnO etching: The ZnO thin films were selectively etched with a FeCl₃:H₂O 740 mmol solution for 1 minute and 30 seconds at room temperature, using a 400 rpm magnetic agitation. In these conditions, we observed a lateral under etching of 12 μm for the ZnO thin films grown at 80 °C and 15 μm for the ZnO thin films grown at 60 °C.

- Etching masks removal: The S1813 etching mask as well as the SX AR-P passivation layer were removed in acetone (2 min). The different microfabrication steps dedicated to the ZnO etching are illustrated in Fig. 5.17.

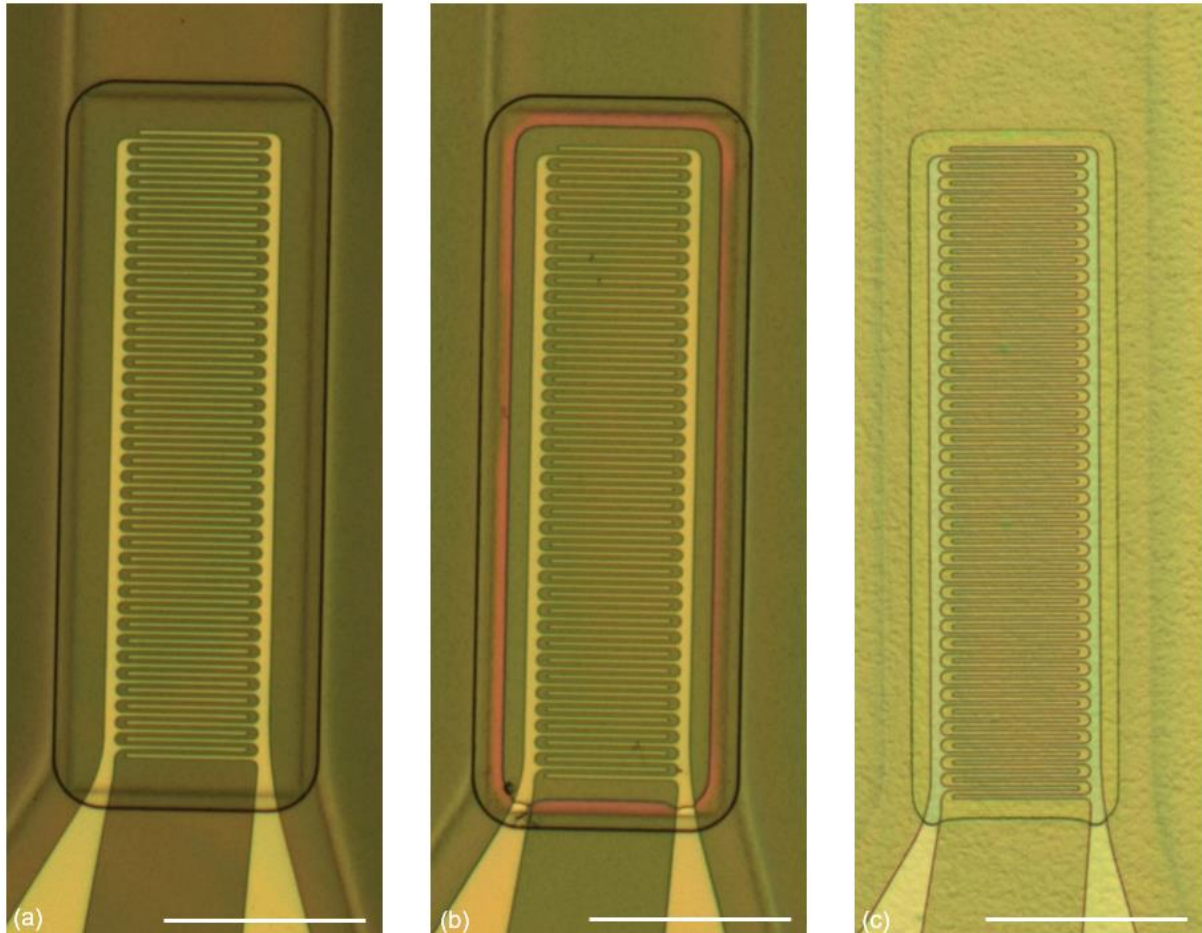


Figure 5.17. (a) S1813 etching mask and underlying ZnO pad patterned around the IDE structure prior to wet etching. (b) S1813 etching mask and underlying ZnO pad patterned around the IDE structure after wet etching. (c) ZnO pad after etching masks (S1813 and SX AR-P) removal by acetone. The scale bar corresponds to 100 μm .

Nonetheless, at the current stage of this work, the sensor structure is still extremely sensitive to the ALD processing of the ZnO thin film, which led to the generation of several cracks concentrated in the Pt metal electrodes at the SU8 encapsulation edge due to the presence of the step height. These difficulties will be detailed within the next section with adopted solutions. Consequently, it should be noted that the following microfabrication steps concerning the cantilever and chip body patterning are not optimized yet and might be subject to further changes.

- Lithography - cantilever patterning: The cantilevers were subsequently patterned by direct laser writing photolithography from a 10 μm thick SU8 epoxy photoresist layer. This SU8 layer presents a two-fold interest, used both for the complete encapsulation of the sensitive area as well as for the cantilever body patterning. Prior to the SU8 spin coating, the wafers were exposed to a soft oxygen/argon plasma pre-treatment (60 mTorr, O_2 - 38 sccm, Ar - 2 sccm, 50 W, 30 s) to improve the SU8 wettability on the substrates. The SU8 3010 layer was then spin coated in two consecutive steps (step 1: 500 rpm, 300 $\text{rpm}\cdot\text{s}^{-1}$, 5 s - step 2: 2600 rpm, 500 $\text{rpm}\cdot\text{s}^{-1}$, 30 s), followed by the photoresist soft baking (step 1: 65 $^\circ\text{C}$, 5 min, 50 $^\circ\text{C}\cdot\text{h}^{-1}$ - step 2: 95 $^\circ\text{C}$, 4 min, 50 $^\circ\text{C}\cdot\text{h}^{-1}$). The SU8 layer was then UV-exposed by direct laser lithography (dose: 1015 $\text{mJ}\cdot\text{cm}^{-2}$, defocus: +3). Subsequently, the post exposure baking was performed (step 1: 65 $^\circ\text{C}$, 2 min, 50 $^\circ\text{C}\cdot\text{h}^{-1}$ - step 2: 95 $^\circ\text{C}$, 4 min, 50 $^\circ\text{C}\cdot\text{h}^{-1}$), followed by the development using two baths (bath 1: 2 min 15 s - bath 2: 15 s) of SU8 developer (PGMEA) and rinsing in IPA (15 s). The aim of the second PGMEA bath is to remove the developed SU8 without surface contamination by the redeposits from the large patterned areas removed. Finally, the hard baking was performed (95 $^\circ\text{C}$, 60 min, 50 $^\circ\text{C}\cdot\text{h}^{-1}$) on the SU8 layer to complete crosslinking and release strain in the structure.
- Lithography - chip body patterning: The chip body was patterned by direct laser writing photolithography from a 200 μm thick SU8 epoxy photoresist layer. Prior to the SU8 spin coating, the wafers were exposed to a soft oxygen/argon plasma pre-treatment (60 mTorr, O_2 - 38 sccm, Ar - 2 sccm, 50 W, 20 s) to improve the SU8 wettability on the substrates. The SU8 100 layer was then spin coated in two consecutive steps (step 1: 500 rpm, 300 $\text{rpm}\cdot\text{s}^{-1}$, 10 s - step 2: 1250 rpm, 500 $\text{rpm}\cdot\text{s}^{-1}$, 80 s). As the deposited SU8 layer is particularly thick, it was left to dry for a day to allow for the flattening of the photoresist on the underlying substrates. Thereafter, the photoresist soft baking was performed (step 1: 65 $^\circ\text{C}$, 30 min, 180 $^\circ\text{C}\cdot\text{h}^{-1}$ - step 2: 95 $^\circ\text{C}$, 100 min, 120 $^\circ\text{C}\cdot\text{h}^{-1}$), followed by the UV-exposure by direct laser lithography (dose: 500 $\text{mJ}\cdot\text{cm}^{-2}$, defocus: +20) and the post exposure baking (step 1: 65 $^\circ\text{C}$, 5 min, 180 $^\circ\text{C}\cdot\text{h}^{-1}$ - step 2: 95 $^\circ\text{C}$, 25 min, 120 $^\circ\text{C}\cdot\text{h}^{-1}$). Due to the important thickness of the SU8 100 layer, large development times are required,

an orbital shaker with an agitation of 100 rpm.s^{-1} was thus used to substitute the manual agitation during the development. Patterns were developed using three baths (bath 1: 45 min - bath 2: 5 min – bath 3: 1 min) of SU8 developer (PGMEA) and rinsing in IPA (30 s). Finally, the hard baking was performed ($60 \text{ }^\circ\text{C}$, 18 h, $50 \text{ }^\circ\text{C.h}^{-1}$) on the SU8 layer to complete crosslinking and release strain in the structure. It should be noted that the hard baking of SU8 is usually performed at higher temperatures (typically higher than 150°C) during a shorter amount of time. However, in order to avoid the presence of thermal shocks and subsequent generation of cracks, the temperature of the hard baking was decreased to $60 \text{ }^\circ\text{C}$ and the baking time increased to 18 hours.

- Chip and cantilever releasing: The chip body together with the microcantilevers were finally released from the silicon wafer via the chemical etching in $\text{FeCl}_3\text{:H}_2\text{O}$ 740 mmol of the oxidized copper sacrificial layer for several hours.

5.1.5. Troubleshooting

Major difficulties appeared concerning the choice of appropriate materials in the sensor's composite structure stacking of organic and inorganic materials, in terms of mechanical adhesion, thermal stability, or chemical amenability within the different microfabrication processing steps. This section aims at reporting some specific issues faced during the different microfabrication processing steps and detailing the solutions adopted.

- Choice of the sacrificial layer for cantilever releasing

The choice of the sacrificial layer material is one of the key parameters for this fabrication process. The chosen material must be easily etched for the structures releasing step but inert to the chemicals involved during the different fabrication steps. Moreover, the sacrificial layer must present a good adhesion with the other materials involved, i.e. platinum and SU8 photoresist. Different materials were investigated such as gold, aluminium and copper. The lithography developer based on TMAH etches the

aluminium sacrificial layer, which prevented the use of this material within the microfabrication process. Additionally, thick SU8 layers present a very poor adhesion to gold, leading to a delamination of the SU8 200 μm thick layer during their development, as shown in Fig. 5.18.

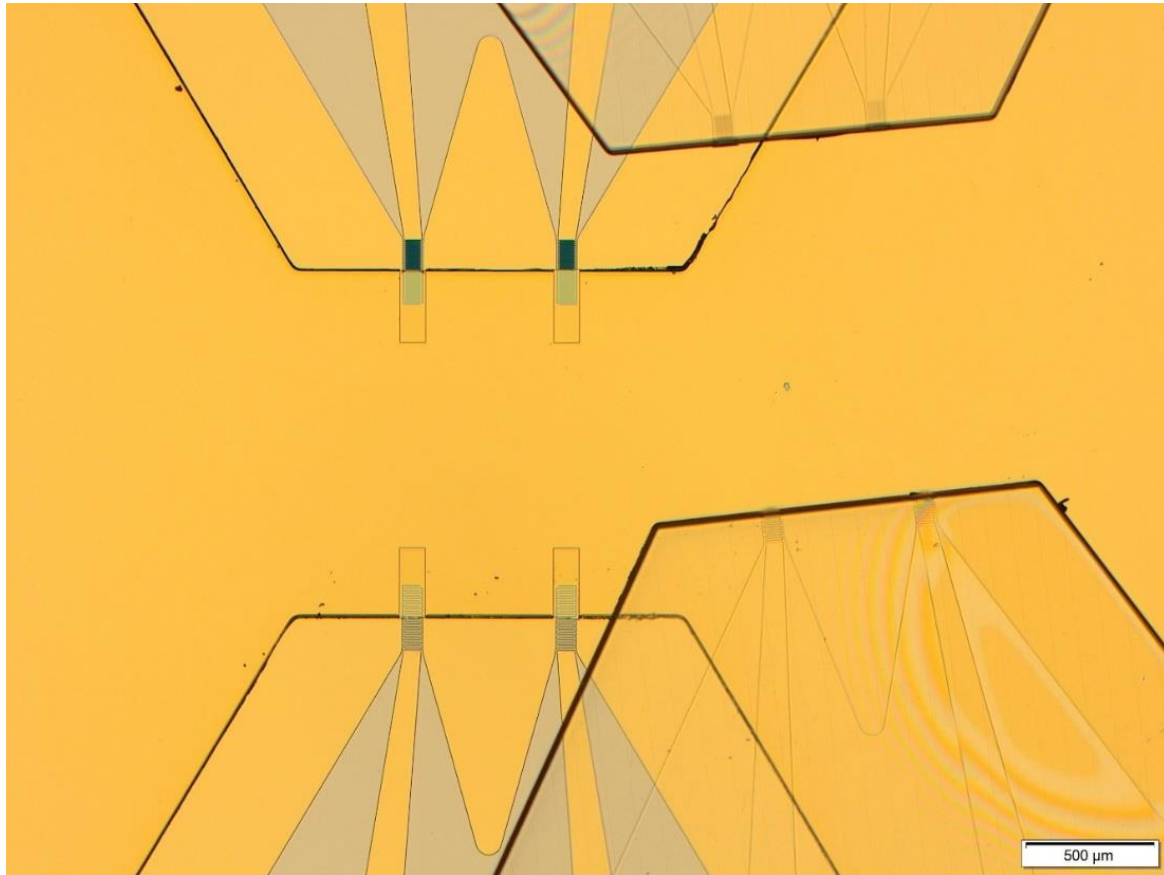


Figure 5.18. Delamination of thick SU8 layers on a gold sacrificial layer.

Consequently, a sacrificial layer of copper with a thickness of 2 μm has been found as the best compromise, copper being chemically inert to the lithography developer and showing a good adhesion with platinum electrodes and SU8 photoresist.

- Choice of the Cu passivation layer

A S1813 photoresist layer was initially used as the Cu passivation layer, in order to protect the Cu sacrificial layer during the ZnO wet chemical etching. The Cu passivation layer was spin coated on the wafer prior to ALD processing. As the

thickness of the ZnO thin film is particularly important for the ALD technique (i.e. 300 nm, corresponding to ~ 2000 loops and a corresponding deposition time of ~ 7 hours), the S1813 photoresist layer was thus exposed during a substantial amount of time to the deposition temperatures of 80 °C and 60 °C within the ALD reactor. This led to a degradation and cracking of the S1813 photoresist layer resulting from the ALD processing, as illustrated in Fig. 5.19.

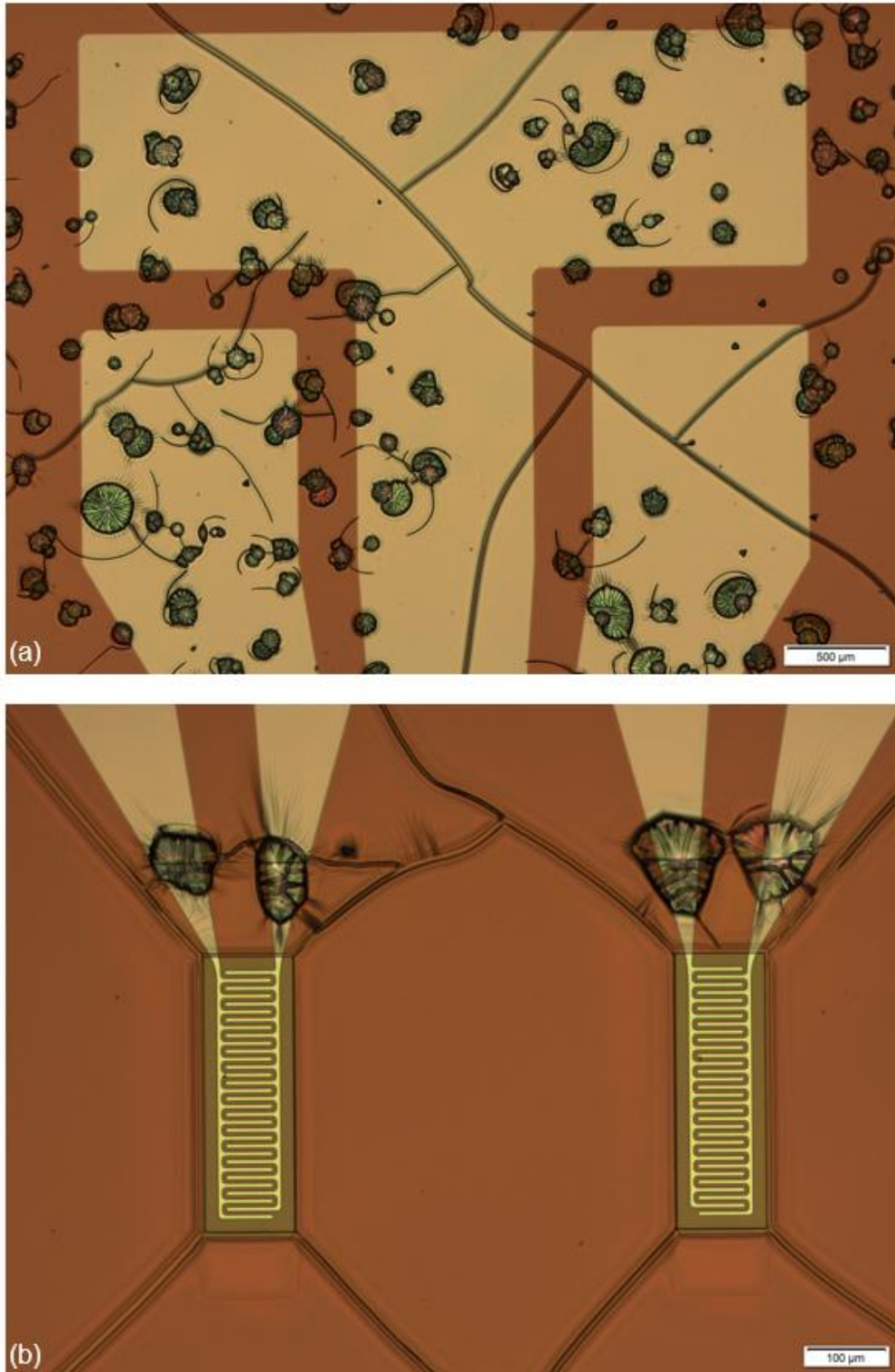


Figure 5.19. Thermal degradation and cracking of the S1813 passivation layer resulting from ALD processing at a deposition temperature of 80 °C. (a) Top view showing the impact of the thermal degradation induced on the S1813 photoresist in the area of the bounding pads. (b) Enclosed top view showing the impact of the thermal degradation induced on the S1813 photoresist in the area of the Pt IDE.

This thermal degradation of the S1813 photoresist layer is critical as it prevented a successful wet etching of the ZnO thin film, due to the FeCl₃:H₂O solution reaching the Cu sacrificial through the S1813 defects and cracks. These difficulties emphasized the need for a thermostable photoresist which could withstand an exposition of several hours to temperatures up to 80 °C without degradation, to avoid any cracking of the photoresist. Within this scope, the SX AR-P 3500/8 photoresist was selected to substitute the S1813 passivation layer. The SX AR-P 3500/8 is a positive photoresist particularly adapted for high-temperature applications, thermally stable up to 300 °C [19]. Concomitantly, slow temperatures ramps (50 °C.h⁻¹) were imposed during the heating and cooling steps of the ALD reactor to the deposition temperature to avoid the generation of thermal shocks in the sensor's structure. As depicted in Fig. 5.17, the SX AR-P layer remained undegraded after the ALD processing of the ZnO thin film, thus validating its thermal stability and its further integration within the microfabrication process.

- Platinum continuity at the SU8 encapsulation layer edge

As mentioned previously, the platinum continuity between the sensing interdigitated electrodes located on the SU8 encapsulation layer and the large bounding pads on the copper sacrificial layer is a highly critical point of the microfabrication process. The platinum continuity at the SU8 encapsulation edge prior to ALD processing was greatly improved via the maskless aligner laser defocus leading to high positive slopes of the SU8 pattern edges. Moreover, it was observed experimentally that increasing the evaporation rate of Pt from 1.0 Å.s⁻¹ to 1.5 Å.s⁻¹ was substantially reducing the generation of cracks at the encapsulation layer edge. As an increase of the evaporation rate is concomitant with an increase in the thermal energy of the evaporated atoms, it could be stated that the Pt structure results in a higher grain size with less surface roughness, thus mitigating the cracks initiation and propagation. Nonetheless, further studies need to be performed to confirm the above-mentioned statement.

Furthermore, the ALD processing consistently caused the apparition of cracks in the Pt layer, originating and propagating from the SU8 encapsulation layer edge, as illustrated in Fig. 5.20(a). As the encapsulation edge originally consisted in a straight

patterned line, the cracks could thus easily propagate along this line and induce a rupture of the electrical continuity of the stepped electrode. Consequently, the encapsulation layer edge was tentatively patterned as several circular segments to mitigate the cracks propagation of the stepped electrode, as depicted in Fig. 5.20(b).

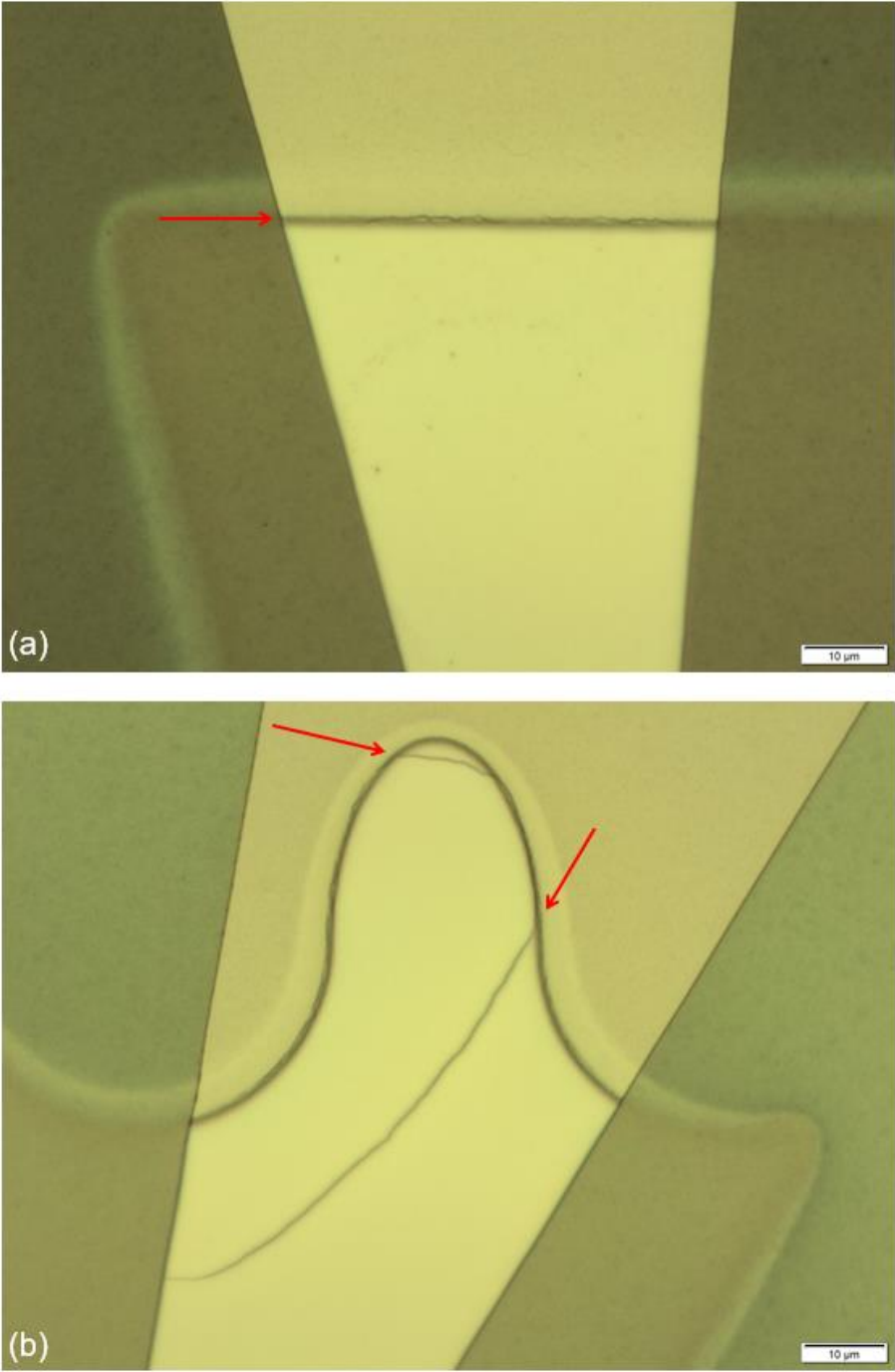


Figure 5.20. (a) Cracks generated in the Pt layer at the SU8 encapsulation layer edge after ALD processing. (b) SU8 encapsulation layer edge patterned as several circular segments to tentatively mitigate the cracks propagation of the stepped electrode. The red arrows indicate the propagation lines of the cracks.

However, the patterning of this peculiar shape at the encapsulation layer edge proved to be ineffective, as cracks were still induced from the stepped electrode and propagating towards the Pt IDE. Consequently, a completely different approach was considered, involving the deposition of silver on top of the stepped electrode to ensure its electrical continuity. A CeraPrinter X-Serie [20] was thus used for the inkjet printing of silver ink (SI-J20x, Agfa) on top of the encapsulation edge. This technique allows for a precise deposition of silver ink droplets with controlled diameters. The silver inkjet printing was performed after the ZnO wet chemical etching and the etching masks removal (i.e. between steps 11 and 12 within the microfabrication process detailed in Fig. 5.12). In order to protect the ZnO thin film from environmental exposure, a 2 μm thick SU8 2002 layer was spin coated on top of the sensitive area directly after the etching masks removal and prior to the inkjet printing. This additional SU8 layer will be referred as the “top” encapsulation layer to avoid confusions with the underlying encapsulation layer where the stepped electrodes are located. The SU8 2002 layer was spin coated in two consecutive steps (step 1: 500 rpm, 300 rpm.s⁻¹, 5 s - step 2: 2000 rpm, 500 rpm.s⁻¹, 45 s), followed by the photoresist soft baking (step 1: 65 °C, 2 min, 50 °C.h⁻¹ - step 2: 95 °C, 3 min, 50 °C.h⁻¹). The SU8 layer was then UV-exposed by direct laser lithography (dose: 3000 mJ.cm⁻², defocus: +25). Subsequently, the post exposure baking was performed (step1: 65 °C, 2 min, 50 °C.h⁻¹ - step 2: 95 °C, 3 min, 50 °C.h⁻¹), followed by the development (60 s) with SU8 developer (PGMEA) and rinsing in IPA (15 s). Finally, the hard baking was performed (95 °C, 60 min, 50 °C.h⁻¹) on the SU8 top encapsulation layer. Furthermore, every SU8 cantilever consists of two interdigitated Pt sets, each one leading to a step height with the SU8 encapsulation layer edge where the silver inkjet printing needs to be performed. Therefore, the length of the SU8 top encapsulation layer was extended as a separating wall towards the stepped electrodes to avoid short-circuiting during the liquid silver ink printing and spreading at both edges, as illustrated in Fig. 5.21.

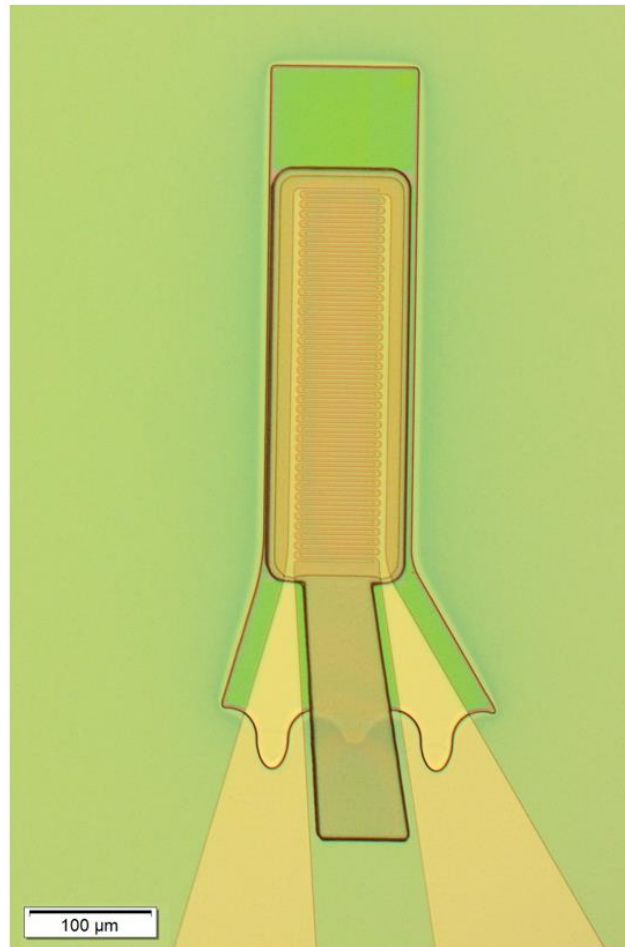


Figure 5.21. Top view showing the sensor structure prior to inkjet printing. A SU8 2002 photoresist layer was spin coated on top of the sensitive area to encapsulate the ZnO thin film and extended as a separating wall towards the stepped electrodes to avoid short-circuiting during the silver ink printing at both edges.

The printing strategy consisted of the deposition of six successive silver layers, each layer involving the inkjet printing of three silver droplets (whose diameter is $\sim 75 \mu\text{m}$), as depicted in Fig. 5.22(a). It should be noted that the printed silver droplets serve the unique purpose of ensuring the electrical continuity of the Pt stepped electrodes. These silver layers are not in contact with the ALD-grown ZnO thin films, they thus have no influence on the electrical properties of the Pt/ZnO/Pt Schottky junctions at the sensitive area. Following the inkjet printing, the silver layers were cured ($90 \text{ }^\circ\text{C}$, 4 h, $50 \text{ }^\circ\text{C}\cdot\text{h}^{-1}$) to decompose stabilizing agents and polymeric additives contained within the silver ink formulation [21]. The resulting silver layers printed at the SU8 encapsulation layer edges are illustrated in Fig. 5.22(b) and Fig. 5.22(c).

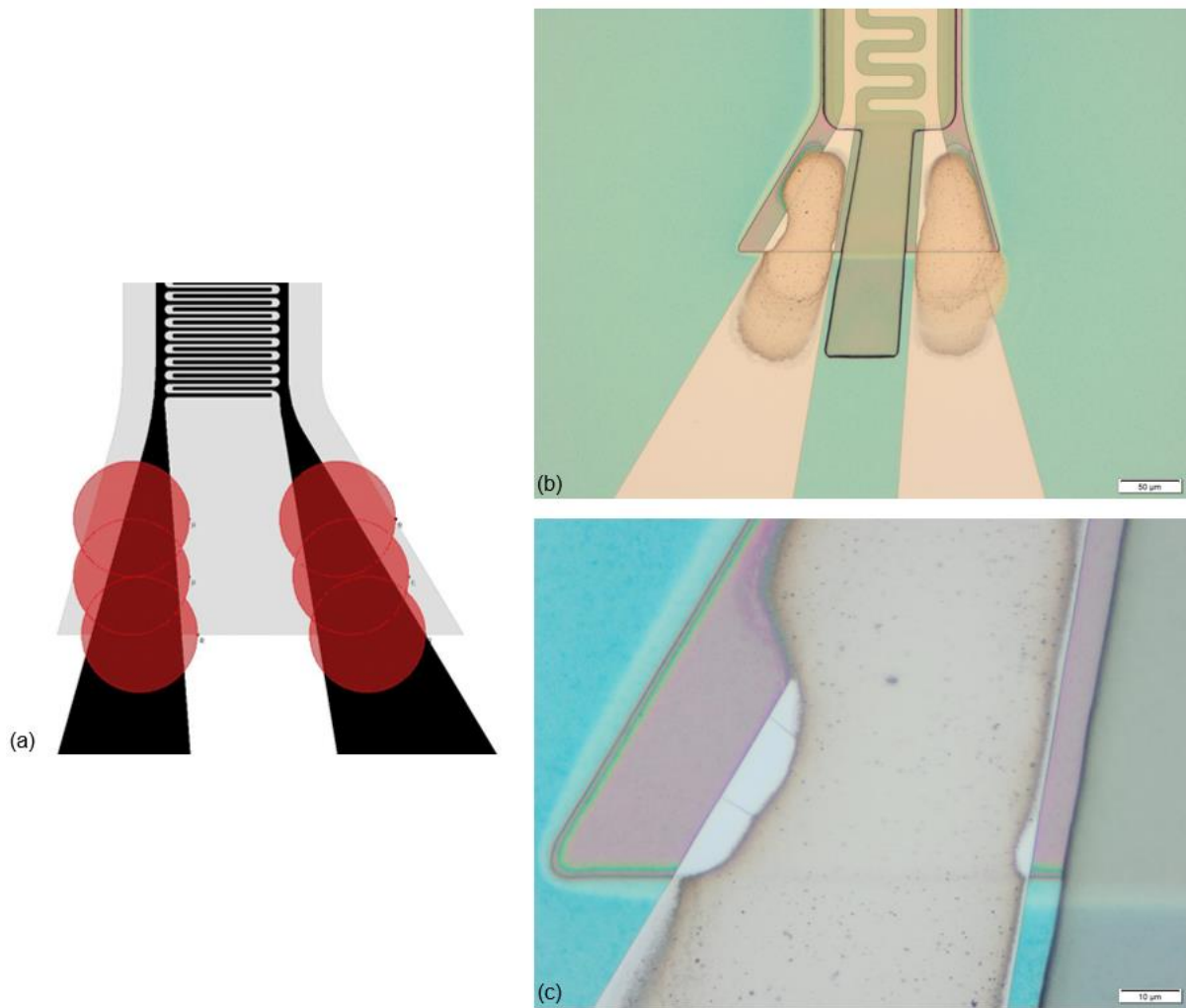


Figure 5.22. (a) Printing strategy, where the red circles represent the silver ink droplets deposited by inkjet printing. (b) Silver layers obtained at the SU8 encapsulation layer edges. (c) Enclosed view at the encapsulation layer edge, showing the continuity of the printed silver layer.

As observed from Fig. 5.22(b) and 5.22(c), the printed silver layers on the stepped Pt electrodes are continuous. Nonetheless, as the whole structure is contacted by the Cu sacrificial layer, it is impossible to probe the local electrical continuity of a stepped electrode before releasing the chip body.

5.2. Electromechanical transduction

At the current stage of this work, the printing of the silver layers was recently performed, while the last microfabrication steps dedicated to the cantilever and chip body patterning are still being optimized. Upon validation of the final steps of the

microfabrication process, the remaining course of action of this project will be dedicated to the full-SU8 body piezotronic strain microsensors integration and testing. The electrical and electromechanical transducing properties of these devices will be analysed and compared to the benchmark polyimide strain sensors described in the previous chapter.

5.3. Conclusion

The study carried out in this chapter illustrates well the difficulties linked with the composite integration of inorganic thin films within a full-SU8 body. Several critical steps of the microfabrication process were successfully overcome via a careful choice of materials with appropriated interfacial compatibilities. Furthermore, the progress of the microfabrication processing recently had to be halted due to severe technical issues faced with the maskless laser aligner. The remaining steps of the microfabrication process and subsequent electromechanical transduction analysis will thus be resumed upon resolution of these technical difficulties.

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6. Conclusions and Perspectives

This chapter aims at summarizing the most important findings and achievements reported within the frame of this work. The present and forthcoming challenges are discussed as well, with a particular focus on a few promising perspectives further detailed in this chapter.

The microfabrication of strain-sensitive microsensors integrated in millimetre-sized cantilevers on flexible polymeric substrates was successfully achieved by means of maskless laser lithography. Pt/ZnO/Pt back-to-back Schottky diode junctions have been shaped in interdigitated microelectrodes to get piezotronic strain sensing on the clamp area of the cantilever structure. This work consists in the first successful integration of strain self-sensing sensors based on piezotronic diode junction inside plastic cantilevers, which paves the way towards the processing of ultrasensitive strain microsensors on MEMS structures. In order to illustrate the great potential of the developed piezotronic strain sensors for scanning probe applications, we performed atomic force microscopy (AFM) imaging measurements with the polyimide cantilevered sensors terminated by a tip.

Capabilities of piezotronic probes for AFM imaging operation

The piezotronic strain sensors ability to monotonously convert the polyimide cantilevers' mechanical deformation in current modulation was used for imaging surface topography in a similar way as atomic force microscopy (AFM) in contact mode. The first step consisted in the integration of a probe on the sensor's cantilever. A silica colloid with a diameter of 15 μm was used for that purpose. The reference

sicastar C18 [1] (Micromod Partikeltechnologie GmbH, Germany) has been selected, owing to its strong hydrophobic octadecyl (C18) surface limiting its adhesion to surfaces. Prior to the probe's integration, the cantilever's length was halved with a bevel cut to a length of ~ 2.5 mm. This resulted in a triangular shape at the cantilever's tip, which allowed for an easier localisation of the probe as well as to reduce the torsion-induced interactions of the cantilever with its vicinity. The silica sphere was stuck to the cantilever under binocular microscope with a sub-micrometric XYZ movement (Renishaw, United Kingdom), using an epoxy resin (EpoFix, Strueurs) previously spread on the cantilever's surface. The sensor was then placed on a drying oven at 70 °C during 24 hours for the resin hardening. The resulting integration of the silica colloid sphere on the cantilever's tip is represented in Fig. 6.1.



Figure 6.1. Integration of the silica colloid sphere on the polyimide cantilever tip.

Following the tip's addition on the polyimide cantilever, the piezotronic sensor was mounted on the AFM Nanonics head described in chapter 4 for its subsequent integration into the measurement and imaging chain, as illustrated in Fig. 6.2.

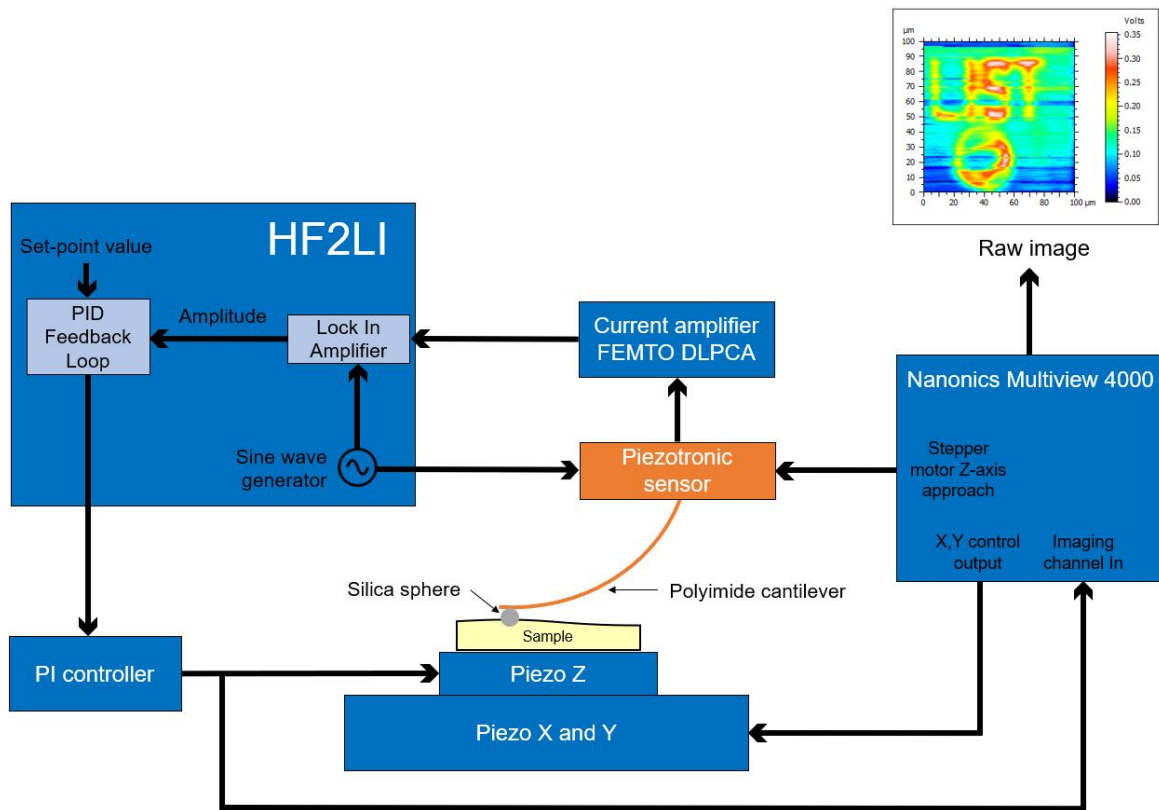


Figure 6.2. Illustration of the measurement and imaging chain used for AFM imaging.

This instrumentation detailing the measurement and imaging chain used for AFM imaging is detailed within Appendix D.

The imaging was realized on a hard baked SU8 surface patterned by lithography to represent the « LIST » name and logo with a 10 μm depth, followed by the deposition of a 50 nm Pt layer. This thin Pt layer was used to limit triboelectric charges induced by the sweeping of the probe tip to the polymeric SU8 surface. The patterned surface was subsequently scanned by using the conditions described in Appendix D. A top view picture of this pattern with the corresponding image obtained after scanning and conversion to metric coordinates are presented in Fig. 6.3(a) and Fig. 6.3(b), respectively.

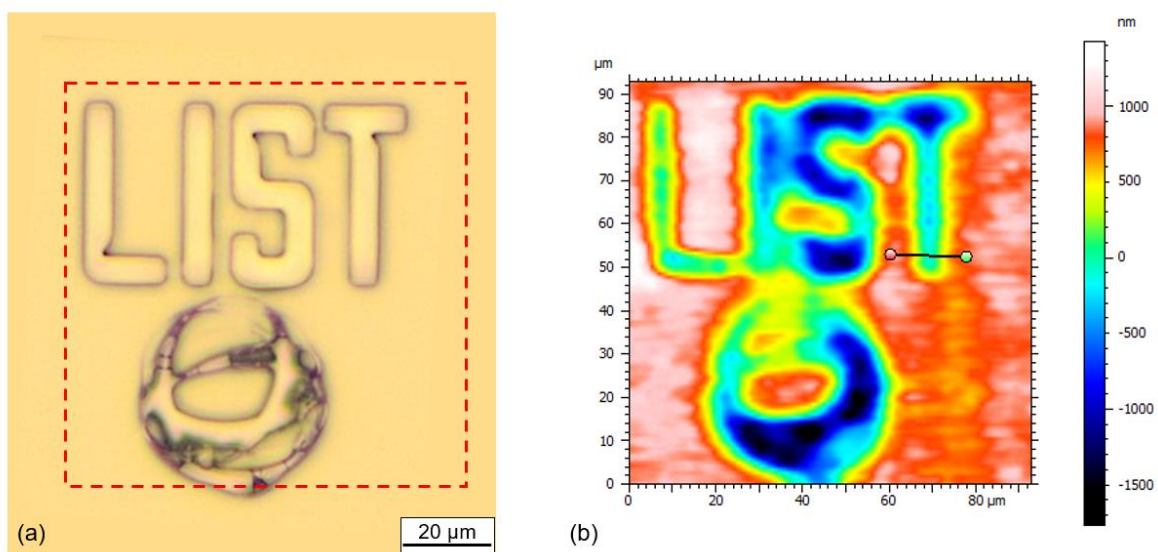


Figure 6.3. (a) Microstructure sample's surface representing the LIST logo (optical microscopy). The outlined dashed red box represents the scanned surface area by the polyimide cantilever with the silica sphere tip end. (b) AFM image obtained by the piezotronic probe after scanning on the $100 \times 100 \mu\text{m}^2$ surface and conversion to metric coordinates, with the corresponding scale representing the Z-axis value for every pixel.

Furthermore, the impact of the measurement with the corresponding footprints of the lines scanned on the probed surface area is shown in Fig. 6.4.



Figure 6.4. Footprints of cantilever's lines scanning on the surface area probed.

The image obtained after scanning in Fig. 6.3(b) is further displayed in Fig. 6.5(a), with a depth profile realized as a line on the letter "T" of the LIST logo, depicted in

Fig. 6.5(b). The rounded profile reveals the convolution effect of the sphere at the tip end with the microstructure of the surface.

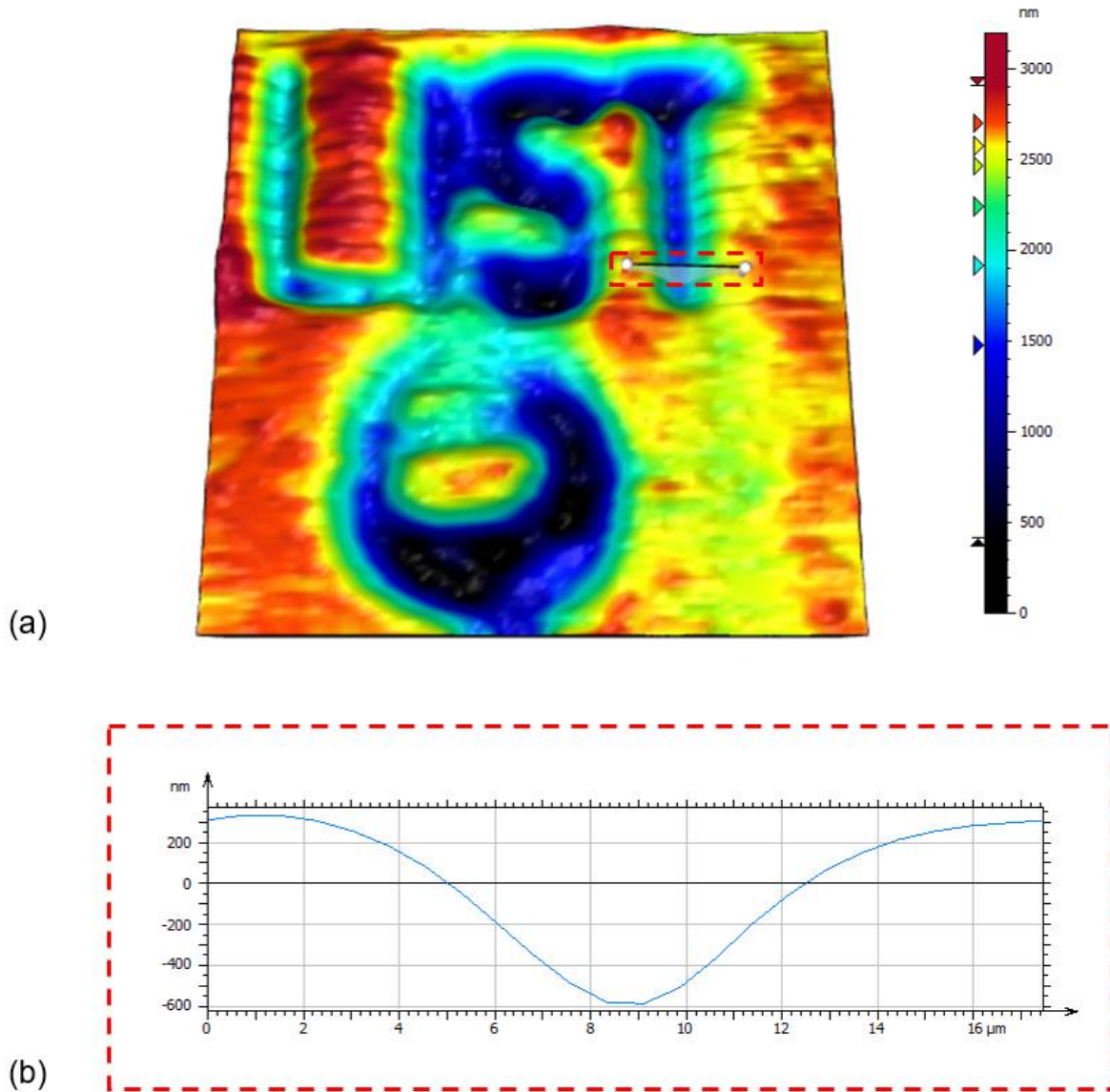


Figure 6.5. (a) AFM image obtained with the piezotronic probe after measurement on the $100 \times 100 \mu\text{m}^2$ surface and conversion to metric coordinates, with the corresponding scale representing the Z-axis value for every pixel. The red dashed lines highlight the area where the depth profile was realized on the letter "T" of the LIST logo. (b) Depth profile obtained on the above-mentioned area, showing the variation of the Z-axis value as a function of the lateral distance.

As displayed in Fig. 6.3 and Fig. 6.5, the piezotronic strain sensors are able to accurately represent the axial surface topography of the patterned surface, showing a sensitivity down to the hundreds of nanometers. These results consist in the first successful integration of strain self-sensing sensors based on piezotronic diode

junction inside polymeric cantilevers addressing AFM operation. They further confirm the high electromechanical sensitivity of the piezotronic strain sensors as well as their great potential for scanning probe operations. Therefore, upon validation of the microfabrication processing of the full-SU8 body piezotronic strain microsensors, similar measurements shall be performed to assess the expected sensitivity improvement linked with the sensors' miniaturization.

Moreover, transducing capability was demonstrated for applied strains inferior to 1% for both DC and AC bias modulation, with a measured gauge factor as high as 150, leading to the expected Schottky barrier height modulation by the piezotronic effect. We performed noise analysis for the first time on piezotronic strain sensors, revealing the presence of the Johnson-Nyquist noise background level, as well as the appearance of the shot noise and the flicker noise when the bias voltage imposed on the sensors was increased. These new insights about noise amplitudes and origins are promising matter of optimization to improve the signal-to-noise ratio of the sensor.

The question of the gauge factor, the peculiar case of piezotronic sensing

Nevertheless, the field of piezotronics is a relatively new area of study, where several aspects remain to be improved. Most importantly, the gauge factor (GF) is typically used in order to characterize the sensitivity of strain sensors. As detailed previously in equation (4.44), the expression commonly used in the literature for the field of piezotronics is based on the absolute value of the ratio of relative change in the electrical current I to the mechanical strain ε , as:

$$GF = \left| \frac{\Delta I}{I_0} \cdot \frac{1}{\varepsilon} \right|$$

With I_0 being the steady state current for a given bias, and ΔI the change in current under a given strain ε for the same applied bias. Nonetheless, this equation has been originally derived from piezoresistive sensing, assuming a linear dependency between the current and the strain. However, for the piezotronic effect, due to the modulation of the Schottky barrier height by piezoelectric polarization charges at the metal-

semiconductor interfaces, there is an exponential dependency between the current and the strain. Therefore, the analytical expression of the gauge factor used to describe sensors' sensitivity needs to be adapted to piezotronic sensing in order to account for that exponential dependence of the current against the strain. Additionally, the polarity of the semiconducting materials is most often disregarded and should be considered more carefully to anticipate how the strain-induced electrical properties will be modulated at the M-S Schottky interfaces via the piezotronic effect.

Besides, an electrical model based on the thermionic emission was developed to describe the conduction mechanisms occurring within the piezotronic strain microsensors. The electron concentration was determined from non-linear fittings of the experimental (I-V) curves, yielding appropriated values for the formation of a Schottky junction. However, several estimations or assumptions had to be implemented concerning electrical parameters involved within the conduction model. This illustrates the complexity of the peculiar back-to-back Schottky diodes configuration, where both the forward and reverse biased M-S interfaces contribute in a different way to the electrical characteristics of the device. Most importantly, the presence of the interface trap states at the M-S junctions, often disregarded in the field of piezotronics, was found to have a prominent impact on the electrical properties and should be considered more carefully. Therefore, a careful investigation of the forward and reverse biased M-S interfaces shall be performed in order to better understand and assess their respective impact on the electrical properties of the M-S-M structures. In the continuation of this work, this could be achieved as instance by depositing a low work function metal in one of the interdigitated finger set, to obtain ohmic junctions so that single Pt-ZnO Schottky junctions could be locally probed.

Towards new material processing to increase the sensitivity

Additionally, further improvements of the developed piezotronic strain microsensors can be foreseen in terms of electromechanical sensitivity, by considering a modification of the materials involved within the device.

More precisely, the transduction properties could be improved by directly acting on the ZnO semiconducting material properties via a doping with transition metals. A substantial improvement of the piezoelectric response can be achieved by substituting Zn^{2+} ions by smaller size ions corresponding to transition metals [2,3]. Among transition metals, vanadium appears as a promising candidate for the doping of ZnO thin films. Reportedly, P. Feng et al. [2] measured a value of 170 pC.N^{-1} corresponding to the piezoelectric coefficient d_{33} in $\text{Zn}_{0.975}\text{V}_{0.025}\text{O}$ thin films, while Y. C. Yang et al. [3] obtained a d_{33} value of 110 pC.N^{-1} in vanadium-doped ZnO films. These results thus consist in a major enhancement of the piezoelectric response when compared to the undoped ZnO piezoelectric coefficient value of 12 pC.N^{-1} for d_{33} [4]. The authors stated that the substitution of transition metals ions with small ionic size on Zn^{2+} sites result in an easier rotation of the bonds between oxygen and transition metals atoms along the c-axis [2]. Consequently, larger piezoelectric displacements are generated upon the application of a strain on the wurtzite structure, subsequently leading to an improvement of the semiconductor piezoelectric response. As the doping of ZnO thin films by ALD is extending to a growing number of materials [5], this perspective could be foreseen in the near future via an appropriate choice of materials' precursors. This also demonstrates the need for a quantitative determination of the semiconductor's piezoelectric coefficients. Within the frame of this work, the piezoelectric response of the ALD-grown ZnO thin films was tentatively measured by piezoelectric force microscopy (PFM), unsuccessfully. Therefore, another technique shall be used to estimate the piezoelectric response of the ZnO thin films.

Finally, the electromechanical sensitivity of the piezotronic strain microsensors could be improved by considering the deposition of a tunnelling barrier by an ultrathin insulating oxide layer between the Pt metal electrodes and the ZnO thin films. As detailed within chapter 1, metal-insulator-semiconductor (M-I-S) junctions making use of the piezotronic effect were recently reported in the literature [6–8]. Noticeably, S. Liu et al. [8] reported a gauge factor value of 2.6×10^8 by using a 0.95 nm thick Al_2O_3 oxide layer at the interface between Pt electrodes and wurtzite GaN. The addition of a thin oxide insulating layer at the junction between the metal and the semiconductor leads to the creation of a piezotronic tunnelling junction. This leads to an exponential dependence between the sensor's current and a tunneling probability term,

proportional to the effective Schottky barrier height formed at the insulating oxide layer [8]. This phenomenon of quantum tunnelling through the insulating layer can be controlled and tuned by the applied mechanical stimuli, which results in a substantial increase of the current and the resulting electromechanical transducing efficiency. Therefore, within LIST cleanroom facilities, the controlled deposition of Al₂O₃, HfO₂ or AlN mastered by ALD as a thin insulating oxide layer could be foreseen to pursue this promising perspective.

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A. Microfabrication of the polyimide body piezotronic cantilever

The different microfabrication processing steps are detailed within this Appendix, with the corresponding experimental parameters employed and specific guidelines to follow.

- Substrate pre-treatment: 75 μm thick polyimide sheets (Kapton® HN, Dupont [1]) were used as a substrates. The pre-treatment performed consisted in a first cleaning in acetone, isopropanol (IPA) and deionized water, followed by a dehydration for 30 min at 150 °C. A plasma activation was then performed on the polyimide sheets' surface (65 mTorr, Ar - 20 sccm, 55 W, 4 min). The interest of this pre-treatment is twofold, as the dehydration removes the adsorbed moisture from the atmosphere (i.e. to avoid blistering and delamination during subsequent coatings) while the plasma treatment increases the polyimide surface energy and wettability for the following lithography process.
- Lithography - metal electrodes: Interdigitated electrodes and contact pads were patterned by lift-off lithography, by using a LOR 3A / S1813 (MicroResist technology GmbH) photoresist bi-layer. LOR 3A is a non-photosensitive resist commonly used in bi-layer lift-off processing, based on polydimethylglutarimide. It is insoluble in typical photoresists solvents, thus avoiding intermixing with the subsequent S1813 photoresist coating. Additionally, LOR 3A develops isotropically and has a relatively low dissolution rate, which allows a great control of the undercut during the development [2]. S1813 is a positive photoresist with excellent adhesion and coating uniformity [3], used as the photosensitive resist on top of the bi-layer. The

LOR 3A layer was spin coated (6000 rpm, 4000 rpm.s⁻¹, 30 s) and baked (160 °C, 5 min) on the polyimide sheet shortly after the plasma treatment. Thereafter, the S1813 layer was spin coated (6000 rpm, 4000 rpm.s⁻¹, 60 s) and baked (115 °C, 60 s), followed by its UV exposure (88 mJ.cm⁻²) by direct UV laser lithography and the bi-layer development (60 s) in a MF-319 solution.

- **Platinum growth:** Prior to metal deposition, the polyimide substrates and resist bi-layers were exposed to a plasma treatment (60 mTorr, O₂ - 38 sccm, Ar - 2 sccm, 50 W, 3 min) to improve the adhesion of metal to polyimide [4]. The electrodes and contact pad layers of titanium (5 nm) / platinum (200 nm) were evaporated by electron beam metal evaporation (EBME). The metal evaporations were performed in the 10⁻⁸ mbar range, with a current of 90 mA and 550 mA for the titanium and the platinum, respectively, while maintaining a constant deposition rate of 1 Å.s⁻¹.
- **Lift-off:** The lift-off process was completed in Remover PG solvent during 5 to 10 minutes. The impact of this process on the IDE structure is highlighted in Fig. A1.

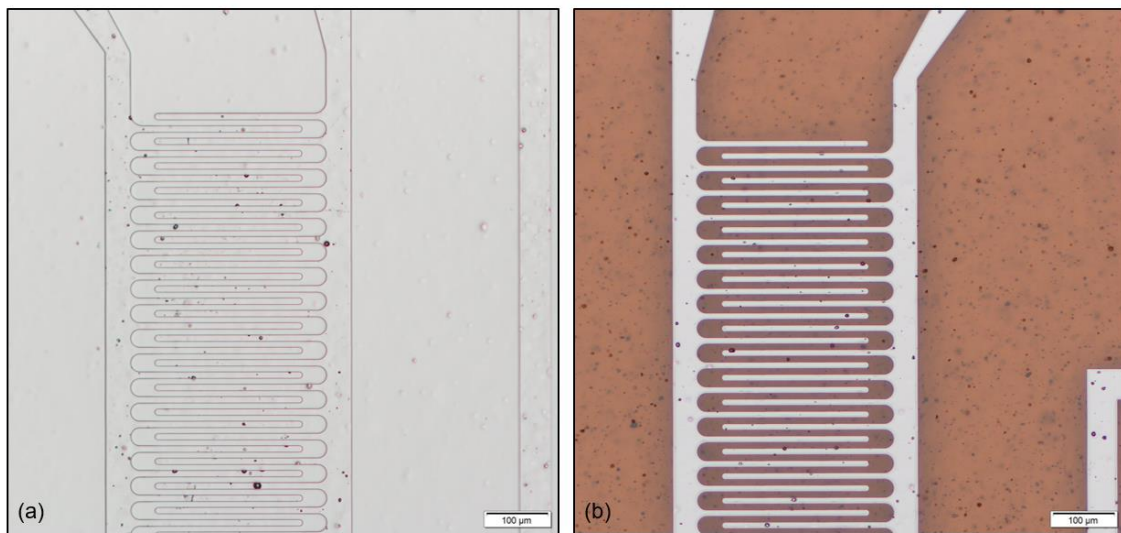


Figure A1. (a) Before lift-off, where Ti and Pt metals are deposited both on the polyimide substrate and on the LOR 3A/S1813 resist bi-layer. (b) After lift-off, where the resist is stripped away on the non-patterned areas.

- **ZnO growth:** A 300 nm thin film of ZnO was then grown by ALD at deposition temperatures of 80 °C and 60 °C, on both the polyimide substrate and the interdigitated platinum electrodes. The substrates were cleaned in acetone, IPA

and deionized water, followed by dehydration for 30 min at 200 °C with a ramp of 150 °C.h⁻¹. Before being introduced into the ALD reactor, an additional plasma cleaning (60 mTorr, O₂ - 38 sccm, Ar - 2 sccm, 50 W, 5 min) was performed on the substrates.

- Lithography - etching mask: Subsequently, ZnO was patterned by lithography and wet etching in order to obtain pads covering the IDE area. Prior to lithography, a pre-treatment of the sensors was performed, consisting in a cleaning by acetone, IPA and deionized water, followed by a dehydration for 30 min at 150 °C with a ramp of 150 °C.h⁻¹. A S1813 etching mask was then spin-coated (step 1: 100 rpm, 300 rpm.s⁻¹, 5 s - step 2: 2000 rpm, 2000 rpm.s⁻¹, 30 s), baked (115 °C, 60 s, 150 °C.h⁻¹), UV-exposed by direct laser lithography (200 mJ.cm⁻²) and developed (60 s) in MF319 developer.
- ZnO etching: The ZnO thin films were selectively etched with a FeCl₃:H₂O 740 mmol solution for 2 minutes at room temperature, with a 400 rpm magnetic agitation. In these conditions, we observed a lateral under etching of 20 μm (± 5 μm). The photoresist etching mask was then removed in acetone for 5 minutes. These different steps are illustrated in Fig. A2.

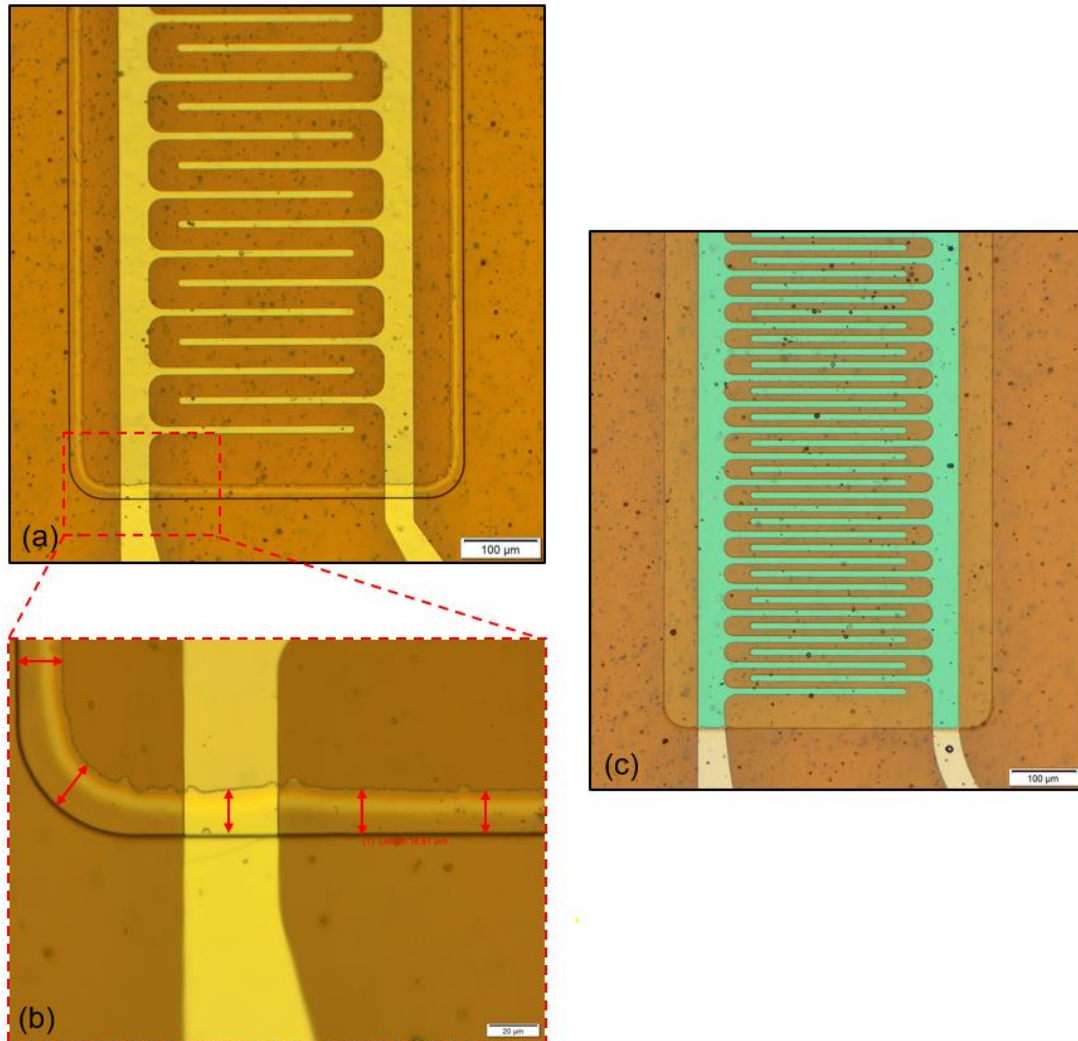


Figure A2. (a) S1813 etching mask and underlying ZnO pad patterned around the IDE structure after wet etching. (b) Enclosed view on the border of the etching mask, where the red arrows indicate the length of the under etching. (c) ZnO pad after etching mask (S1813 photoresist) removal by acetone.

- ZnO passivation: Following ZnO patterning by wet etching, the ZnO pad was passivated with an SU8 coating to prevent its well-known ageing in air [5]. As described in section 2.2.2 of chapter 2, the processing of the SU8 photoresist includes several steps to meet appropriate chemical and mechanical properties. Prior to lithography, a pre-treatment of the sensors was performed, similar as the one described for the lithography of the etching mask. A 2 μm layer of SU8 2002 (MicroResist technology GmbH) was then spin coated (step 1: 500 rpm, 100 rpm.s⁻¹, 5 s - step 2: 2600 rpm, 500 rpm.s⁻¹, 30 s), followed by the photoresist soft baking (step 1: 65 °C, 60 s, 150 °C.h⁻¹ - step 2: 95 °C, 3 min, 150 °C.h⁻¹). The SU8 layer was then UV-exposed by direct laser lithography (1200 mJ.cm⁻²). Subsequently,

the post exposure baking was performed (same conditions as the soft baking), followed by the development (60 s) with SU8 developer (PGMEA), rinsing in IPA (30 s) and the hard baking (150 °C, 15 min, 150 °C.h⁻¹). An enclosed view on the interdigitated electrodes following the SU8 passivation layer lithography can be seen in Fig. 4.1 within the main body of the Chapter 4. Additionally, a sketch of the sensitive area, consisting in the stacking of the Pt interdigitated electrodes, the ZnO pad and the SU8 passivation layer deposited at the clamped area of a polyimide cantilever is shown in Fig. A3.

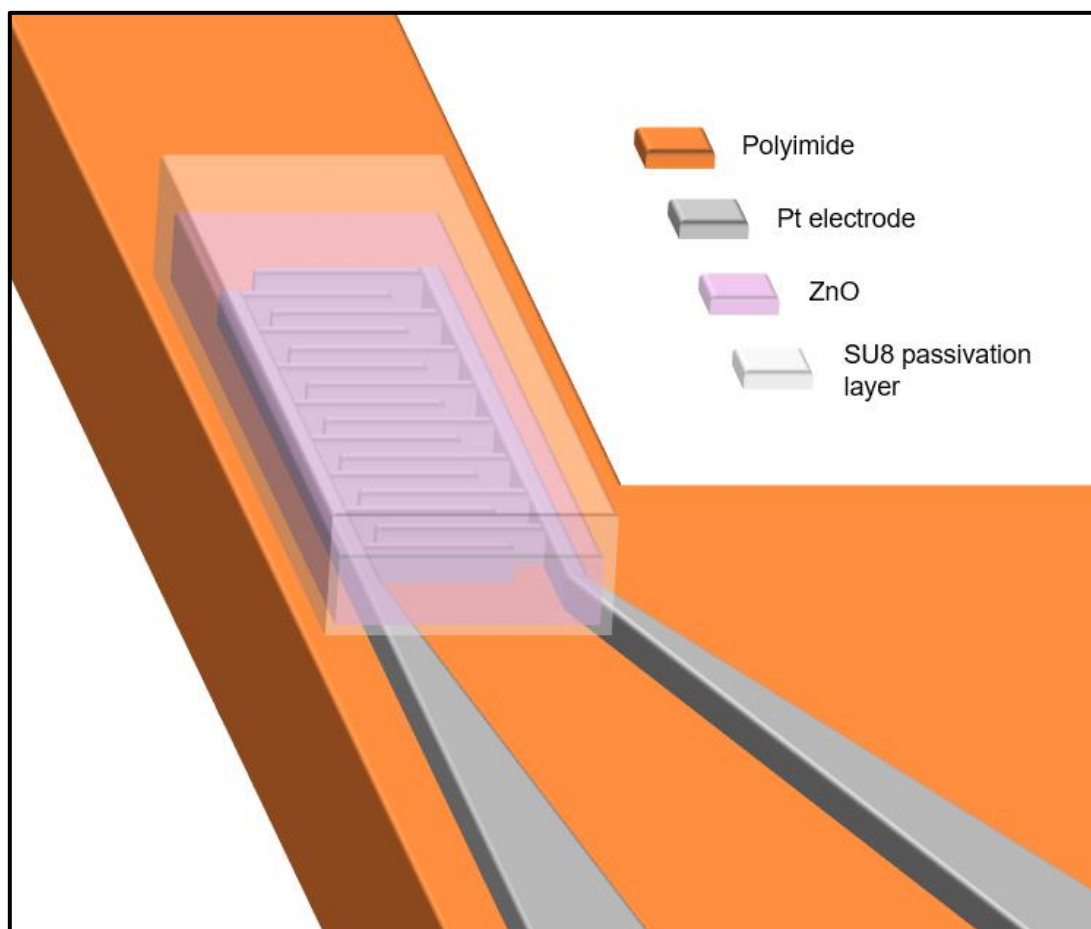


Figure A3. Sketch of IDE electrode configuration at the sensitive area. Not to scale.

- Chip and cantilever releasing: The chip and cantilever were finally released by manual dicing, by the mean of a precision scalpel blade under optical microscope. IDE electrodes were subsequently connected via large Pt contact pads for wire bonding with gold wires to an interfacing printed circuit board (PCB), thus providing

electrical contacting to the measurement setup, following the method provided in section 2.2.5. The sensors were stuck to the PCB using double-sided polyimide heat resistant tape [6]. A general view of the piezotronic strain sensors wire bonded on an interfacing PCB is shown in Fig. A4.

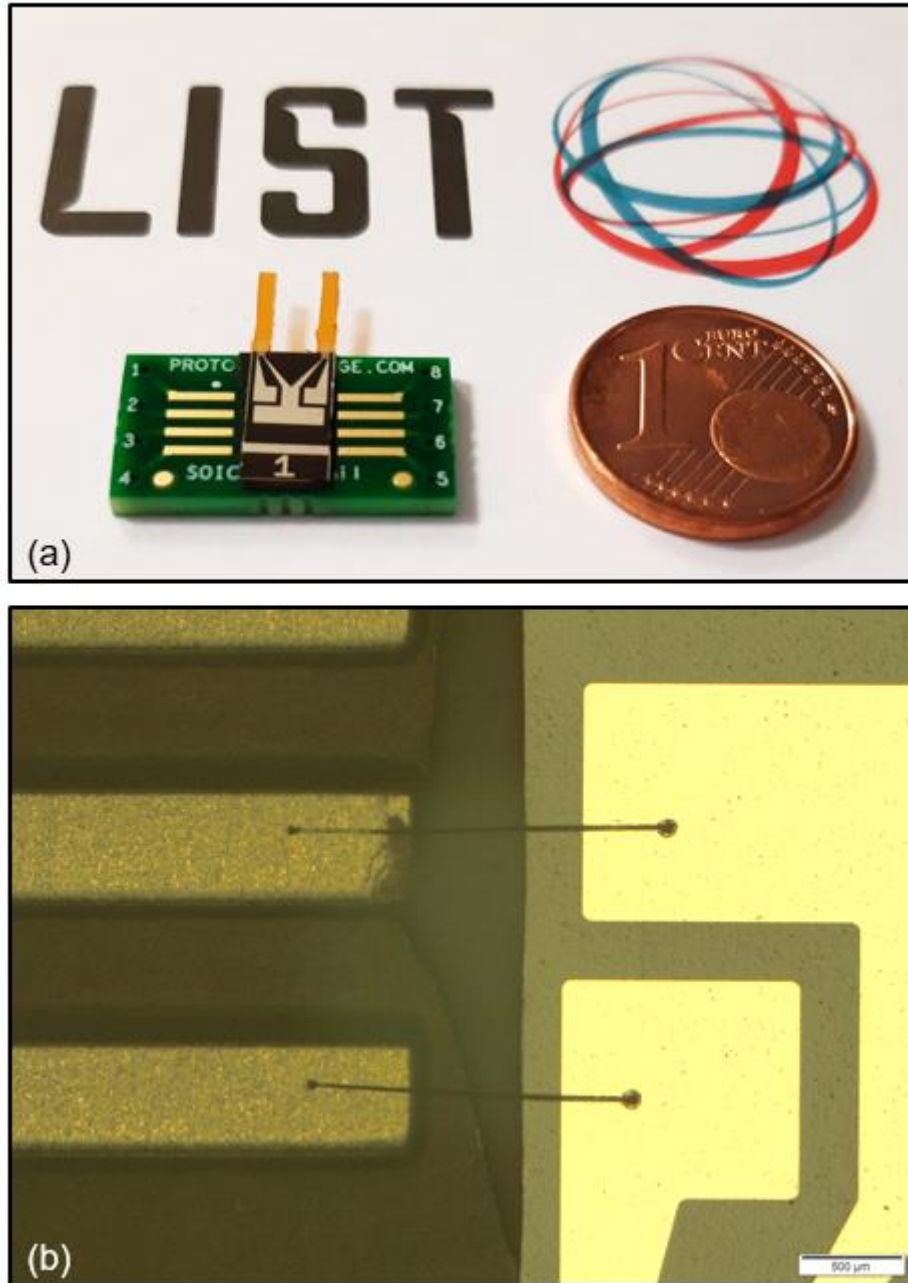


Figure A4. (a) General view of the piezotronic strain sensors integrated on polyimide cantilevered structures and wire bonded on an interfacing PCB. (b) Ball bonding connections between the sensors' Pt pads and the corresponding Au pads on the PCB.

- Mitigation of cracks propagation

Due to the overlaying of several materials during the different stages of the microfabrication process flow, the involved materials are particularly sensitive to the apparition and the propagation of microcracks, thus threatening the structural integrity and the electrical contact continuity of the sensors. These cracks are principally induced by thermal shocks during the baking and cooling operations of the microfabrication process, where materials with different thermal expansion coefficients are involved, as shown in Table A1.

Material	Coefficient of thermal expansion (CTE) at 20 °C [ppm °C ⁻¹]
Polyimide	60
SU8 (hard baked)	52
Platinum	9
Zinc oxide	5

Table A1. Values of coefficient of thermal expansion for polyimide, SU8 (hard baked), platinum and zinc oxide.

Additionally, it was observed that the initialization and propagation of cracks was favoured by the presence of right angles in the microstructures, where the stress concentration is particularly important. Furthermore, ZnO deposited with oxygen gas has been found more sensitive to abrupt thermoplastic deformation. This phenomenon can be explained by its well-defined columnar crystallites structure perpendicular to the substrate. Fig. A5(a). illustrates these different phenomena, with the presence of cracks both at the right angles of the interdigitated platinum electrodes and on the ZnO thin films deposited with molecular oxygen. Consequently, all baking operations succeeding the Pt metal deposition were performed by adding a temperature ramp of 150 °C.h⁻¹, ramping from room temperature up to the desired value and vice-versa. The application of these temperature ramps thus avoided any sudden temperature change and effectively limited cracks propagation in the multi-layered structure. Moreover, a simple design change was implemented on the Pt IDE, where the right angles were rounded to avoid the presence of any sharp angle, resulting in a crack-free structure, as shown in Fig. A5(b).

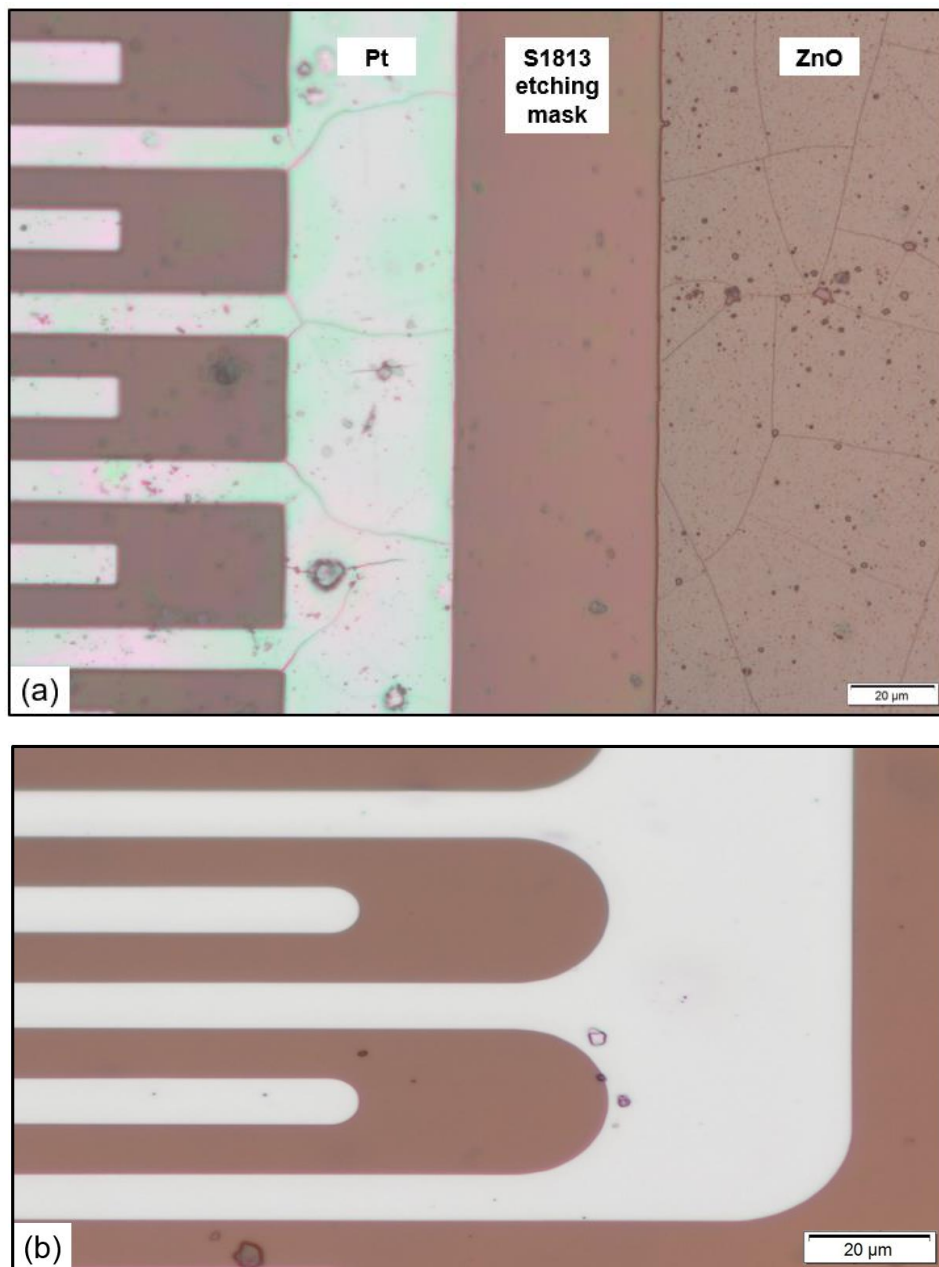


Figure A5. (a) Cracking of the Pt metal electrodes and ZnO thin films (processed by ALD with molecular oxygen gas) due to thermal shocks induced by the process. (b) Design change implemented to limit cracks propagation at the interdigitated Pt electrodes.

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Appendix B

B. Article: Evidence of negative capacitance and capacitance modulation by light and mechanical stimuli in Pt/ZnO/Pt Schottky junctions

Article

Evidence of Negative Capacitance and Capacitance Modulation by Light and Mechanical Stimuli in Pt/ZnO/Pt Schottky Junctions

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Abstract: We report on the evidence of negative capacitance values in a system consisting of metal-semiconductor-metal (MSM) structures, with Schottky junctions made of zinc oxide thin films deposited by Atomic Layer Deposition (ALD) on top of platinum interdigitated electrodes (IDE). The MSM structures were studied over a wide frequency range, between 20 Hz and 1 MHz. Light and mechanical strain applied to the device modulate positive or negative capacitance and conductance characteristics by tuning the flow of electrons involved in the conduction mechanisms. A complete study was carried out by measuring the capacitance and conductance characteristics under the influence of both dark and light conditions, over an extended range of applied bias voltage and frequency. An impact-loss process linked to the injection of hot electrons at the interface trap states of the metal-semiconductor junction is proposed to be at the origin of the apparition of the negative capacitance values. These negative values are preceded by a local increase of the capacitance associated with the accumulation of trapped electrons at the interface trap states. Thus, we propose a simple device where the capacitance values can be modulated over a wide frequency range via the action of light and strain, while using cleanroom-compatible materials for fabrication. These results open up new perspectives and applications for the miniaturization of highly sensitive and low power consumption environmental sensors, as well as for broadband impedance matching in radio frequency applications.

Keywords: zinc oxide; negative capacitance; capacitance modulation; strain sensor; Schottky junction



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1. Introduction

Despite being observed experimentally for several years [1–3], negative capacitance (NC) phenomena recently aroused substantial interest due to the growing demand for miniaturized electronic devices and applications. Negative capacitance has already been widely studied in ferroelectric-dielectric structures [4–7] to improve the subthreshold swing and internal voltage amplification of transistors [8,9]. Moreover, achieving negative capacitance for inductors over a large frequency range would constitute a breakthrough for broadband impedance matching in radio frequency applications [10]. Therefore, planar and easy to process capacitors with negative capacitance values could be used to replace bulky inductors in such applications [11]. The presence of NC phenomena is often accompanied by an increase in capacitance above the conventional geometrical values, localized in a peak preceding the NC values at low frequencies [12,13]. Recent works have reported a significant increase in capacitance in the presence of a light source, where light-generated carriers, e.g., photoexcited electrons, contribute to the conduction mechanisms [14–16], while further increasing the peak of positive capacitance values preceding the negative capacitance values [17].

Within this scope, a wide range of materials and structures were investigated to further develop the current understanding of NC-associated phenomena. Among them, semiconductor devices, including Schottky diodes [12,18], p-n junctions [19], heterojunctions [20] or metal-insulator-semiconductor structures [21], are well-known for exhibiting such behaviour [22]. Schottky junctions are one of the simplest rectifying systems, which can easily be processed between a metal and a semiconductor. NC is typically observed when a Schottky diode is forward biased at low frequencies, but its exact origin is still a matter of discussion [23]. An additional metallic contact is needed to integrate Schottky junctions into electronic devices, thus forming a metal-semiconductor-metal (MSM) system. This additional contact can either be ohmic or rectifying, the latter leading to the formation of two back-to-back Schottky diodes in the MSM structure. A common cause of NC in MSM diodes is related to the high-level injection of minority carriers from the forward biased metal-semiconductor (MS) junction into the bulk of the semiconductor for intimate Schottky contacts [24]. Another explanation is attributed to an impact-loss process, with a mechanism similar to the impact ionization process. As the electric field is increased and the interface trap states are filled up, electrons acquire excess energy and collide with electrons trapped at the interface states below the Fermi level [1] at the metal-semiconductor junction, moving them into the metal electrode. The interface states can thus play a major role in the obtention of NC in MS systems and typically present dispersive behaviour depending on their ability to follow the frequency of the applied AC driving voltage [12,18,25].

Among semiconducting materials, zinc oxide (ZnO) has attracted considerable attention in the field of semiconductor devices due to several of its features, such as its material compatibility with cleanroom facilities, low temperature processing or its amenability to wet chemical etching [26]. The resulting physical and chemical properties of the material make it viable and appealing for micro and nanotechnology applications, including the fields of biomedical, energy, sensors and optics [27]. The intrinsic n-type electrical behaviour of ZnO is usually linked to the presence of native point defects [26], such as zinc interstitials and oxygen vacancies, with the latter being the most frequently cited reason [28]. The formation of a Schottky junction between ZnO and a high work function metal leads to the generation of localized interface states at the MS junction, at energies corresponding to point defects native to the bulk semiconductor [29]. Oxygen vacancies have been shown to play a major role at the MS interface by pinning the Fermi level close to their defect level, which increases their density at the interface and makes the junction almost insensitive to the Schottky barrier height [30]. Furthermore, negative capacitance phenomena have been linked to the presence, accumulation and migration of oxygen vacancies at the MS interface in various structures [31–34]. Oxygen vacancies have also been shown to be responsible for the observation of memristive behaviour in ZnO thin films [35]. However, few articles report on the observation of negative capacitance with ZnO-based materials or structures [32,36,37]. The observation of NC phenomena in these works is limited to low frequency domains (i.e., below 1 kHz), while the impact of a light source on the capacitive properties has not been considered. Moreover, the investigation of NC phenomena with ZnO thin films grown by Atomic Layer Deposition (ALD) is not present in the literature.

In the present work, we report on the evidence of negative capacitance values in a system consisting of piezotronic strain microsensors, where Pt/ZnO/Pt Schottky junctions are integrated at the clamped area of millimetre-sized polyimide cantilevers [38]. The Schottky junctions are made of zinc oxide thin films deposited by ALD on top of a polyimide substrate with bottom platinum interdigitated electrodes (IDE). A complete study was carried out by measuring the capacitance and conductance characteristics under the influence of both dark and light conditions, over an extended range of applied bias voltage and frequency. We report on the observation of negative capacitance values over a wide frequency range, studied between 20 Hz and 1 MHz. The negative capacitance values are preceded by a local increase in the capacitance of the device, which is further marked in

the presence of a light source. Additionally, we propose a modulation via the mechanical strain of the capacitive response of the sensors by imposing controlled compressive strain steps to the polyimide cantilevers.

2. Materials and Methods

2.1. ZnO Thin Films and Pt Metal Electrodes Deposition

The ZnO thin films were synthesized by ALD using precursors of diethylzinc [DEZ, $\text{Zn}(\text{C}_2\text{H}_5)_2$] (Strem Chemicals, Inc., Bischoheim, France) and deionized (DI) MilliQ water (resistivity of 18.2 M Ω .cm at 25 °C), in a commercial ALD reactor (TFS-200, Beneq, Espoo, Finland) with a thermal configuration. On the one hand, the supporting surfaces for the ZnO thin film deposition consisted of $1 \times 1 \text{ cm}^2$ pieces of pristine single crystal Si(100) wafer (grade Monitor, Siebert GmbH, Aachen, Germany), some of them coated with a 200 nm thick Platinum (Pt) layer (deposited by Electron Beam Metal Evaporation) for comparative thicknesses and structural measurements with the polymeric substrates. On the other hand, 75 μm thick polyimide films (Kapton[®] HN, DuPont de Nemours, Mechelen, Belgium) were used for the subsequent processing of piezotronic strain microsensors. The substrates were cleaned in acetone, isopropanol and DI water, followed by dehydration for 30 min at 200 °C (ramp: 150 °C/h) prior to the ALD growth of ZnO films. Before being introduced into the ALD reactor, an additional plasma cleaning (Plasma Therm 790 RIE, 50 W, 5 min, in Ar:O₂ gases environment at 60 mTorr) was performed on the substrates. Alphagaz 2 Argon gas was used for the purging steps during the ALD process, with a global purity $\geq 99.9999\%$ mol and less than 0.5 H₂O ppm.mol impurity. The ZnO thin films were elaborated at a substrate temperature varying between 60 °C and 100 °C for structural and electrical characterization, while the deposition of ZnO thin films integrated in MSM Schottky junctions was carried out for a substrate temperature of 80 °C. The following sequence of four steps was used: DEZ pulse (0.1 s), Ar purge (6 s), DI water pulse (0.1 s) and Ar purge (6 s). Thermocouples located inside the ALD reaction chamber are controlling and monitoring the reactor and substrate temperatures to the desired value. The depositions were performed under a constant pressure of 2 mbar, controlled by pressure gauges. A number of loops between 1000 and 2000 was set based on the growth rate of the created ZnO thin films at the different temperatures, in order for the ZnO thin films to obtain a thickness ranging between 150 nm for the structural characterization and 300 nm for the piezotronic strain sensors. A higher thickness of the ZnO thin films contributed to an increased electrical stability response of the Schottky junctions by limiting the apparition of memristive phenomena [39].

Prior to thin film metal deposition, used also as supporting conductive bottom layer to fabricate the interdigitated (IDE) electrodes by lithography and lift-off process [38], the polyimide substrates were exposed to a plasma treatment (60 mTorr, O₂—38 sccm, Ar—2 sccm, 50 W, 3 min) to improve the adhesion of metal to polyimide [40]. The electrodes and contact pad layers of titanium (5 nm)/platinum (200 nm) were evaporated by Electron Beam Metal Evaporation. The metal evaporations were performed in the 10^{-8} mbar range, with a current of 90 mA and 550 mA for the titanium and the platinum, respectively, while maintaining a constant deposition rate of $1 \text{ \AA} \cdot \text{s}^{-1}$.

2.2. Structural and Electrical Characterization of ZnO Thin Films

The thickness of ZnO thin film samples was estimated on silicon substrates by ellipsometry (J. A. Woollam M2000 Ellipsometer) by measurements carried out for wavelengths between 300 nm and 1000 nm, with three different incident angles of 65°, 70° and 75°. X-ray diffractometry (XRD) (Diffractometer Bruker D8 Discover with Cu K α radiation and a 5-axis Eulerian cradle) was conducted in a grazing incidence configuration ($\omega = 0.3^\circ$) to estimate the crystalline quality and the preferred crystalline orientation of the ZnO thin films deposited by ALD at various low temperatures deposition (i.e., between 60 °C and 100 °C), on different substrates (i.e., silicon, platinum and polyimide). The microstructure of the ZnO thin films was analysed by scanning electron microscopy (SEM) on a Helios 650

FIB-SEM instrument (FEI Technologies Inc., Hillsboro, OR, USA). Cross-sectional configurations were carried out to further confirm the thickness of the ZnO thin films measured by ellipsometry as well as its conformality on the polyimide and platinum substrates. The resistivity of the ZnO thin films was measured by the four-points probe technique on glass substrates using a sourcemeter (2400 Series SourceMeter, Keithley Instruments, Solon, OH, USA) coupled with a cylindrical four-point probe head and a probe station (Jandel Multiheight Probe Station, Jandel Engineering, Linslade, United Kingdom).

2.3. Strain Sensor and Equivalent Circuit Model

Schottky junctions were made from ALD growth of 300 nm thick ZnO thin films at a deposition temperature of 80 °C, on top of a polyimide substrate with 200 nm thick Pt IDE. The width and the spacing of the fingers of the comb electrodes were fixed to 10 µm. The bottom Pt IDE were patterned by a lift-off process while the ZnO thin films were selectively etched on top of the Pt electrodes by a FeCl₃:H₂O solution. The peculiar ALD features (e.g., low temperature processing, self-limiting nature and stoichiometric control at the nanoscale level) allow for a reliable microfabrication processing on flexible polymeric substrates. More details concerning the microfabrication process flow and the sensors' electrical and transducing behaviour are available in our previous work [38].

As previously mentioned, the back-to-back Schottky diodes formed in our devices are defined by two sets of interdigitated platinum electrodes within the area defined by the ZnO pad, as shown in Figure 1a. The equivalent circuit model involving the interdigitated electrodes is presented in Figure 1c. This leads to the creation of several parallel back-to-back Schottky diodes arranged along the length of the cantilever. The total current *I* of the device corresponds to the sum of each individual back-to-back Schottky diode current, following the equation:

$$I = I_1 + I_2 + I_3 + \dots + I_n = \sum_{i=1}^n I_i \quad (1)$$

where *n* corresponds to the number of back-to-back Schottky diodes created by the two sets of interdigitated platinum electrodes within the area defined by the ZnO pad. Since all the sets of back-to-back diodes were processed in a similar way, the current flowing out of every metal-semiconductor-metal (MSM) structure is considered to be equal ($I_1 = I_2 = I_3 = \dots = I_n$).

The equivalent circuit model can thus be represented by a single back-to-back Schottky diode corresponding to the sum of every MSM diode. This is linked to the use of the same planar metal bottom electrode layer, as well as to the uniformity of the ZnO coating and the reproducibility of its electrical properties by means of the ALD process. When a bias voltage is applied, either with a positive or negative value, one of the Schottky diode junctions will necessarily be reversely biased, while the other will be forward biased. In the following analysis, the reverse and forward biased Schottky junctions will be designated as 1 and 2, respectively. V_1 and V_2 are the voltage drops occurring at the reverse and forward biased Schottky diodes, respectively, while R_S represents the series resistance in the bulk of the ZnO thin film. Even if most of the voltage drop occurs at the reversely biased diode, a small voltage drop is necessary to bias the forward biased diode, as well as to take into account the series resistance of the semiconductor.

Equivalent circuit models of Schottky MS diodes are presented in Figure 1d, taking into account the different capacitive and conductive contributions from both Schottky MS diodes [41]. C_S is the capacitance corresponding to the Schottky depletion region, C_{it} is the capacitance induced by interface trap states, and G_p is the equivalent parallel conductance.

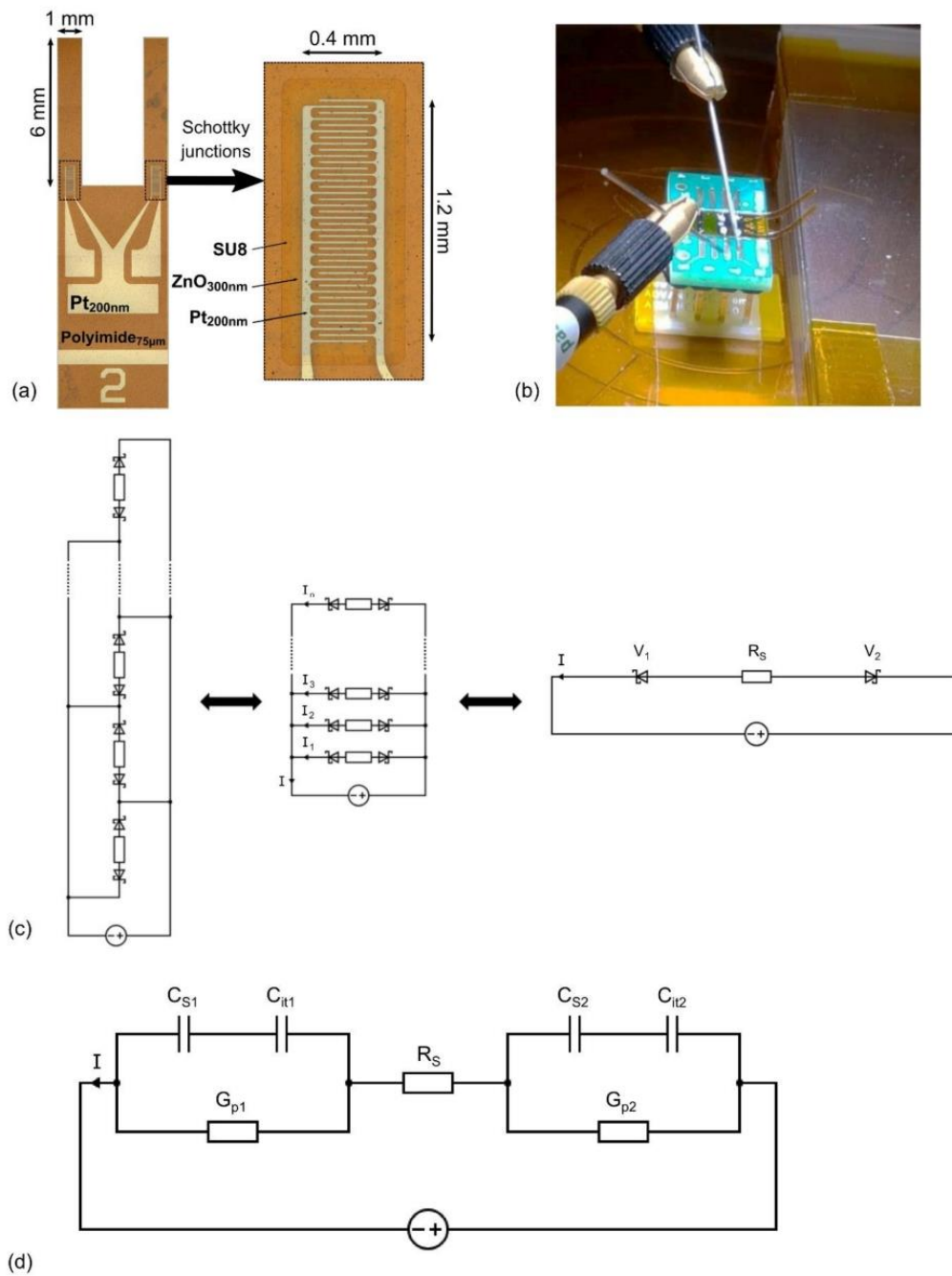


Figure 1. (a) Top view representation of a piezotronic strain microsensor. The black dashed line boxes represent a detailed view of the area of the interdigitated electrodes; (b) Piezotronic strain microsensor mounted and bonded on a printed circuit board (PCB), contacted with tungsten tips. The polyimide cantilevers are bent upwards, leading to the generation of a compressive strain; (c) Equivalent circuit model of the metal-semiconductor-metal structure with interdigitated electrodes; (d) Constitutive capacitance and conductance contributions from each Schottky diode.

2.4. Electrical Characterization of the Pt/ZnO/Pt Schottky Junctions

A complete electrical characterization of the Pt/ZnO/Pt Schottky junctions was carried out by means of capacitance-voltage (C-V), capacitance-frequency (C-f), conductance-voltage (G-V) and conductance-frequency (G-f) measurements. These measurements were performed with an impedance analyser (E4990A Impedance Analyzer, Keysight Technologies, Santa Rosa, CA, USA). A constant AC modulation with an amplitude of 500 mV was superimposed on to a DC bias voltage swept over the defined tension range. The devices were contacted with tungsten tips of the PM8 probe station either completely in the dark, or under a microscope light (EasyLED Ringlights, SCHOTT North America Inc., Rye Brook, NY, USA) incident to the measured devices at a distance of 10 cm. The light characteristics were estimated using a photodiode (PM100D, Thorlabs, Newton, NJ, USA) and are presented in Figure 2. The junctions were let under bias voltage for 30 min either completely in the dark or under the microscope light to stabilize the output current value and to prevent signal drift before performing the (I-V) cycles.

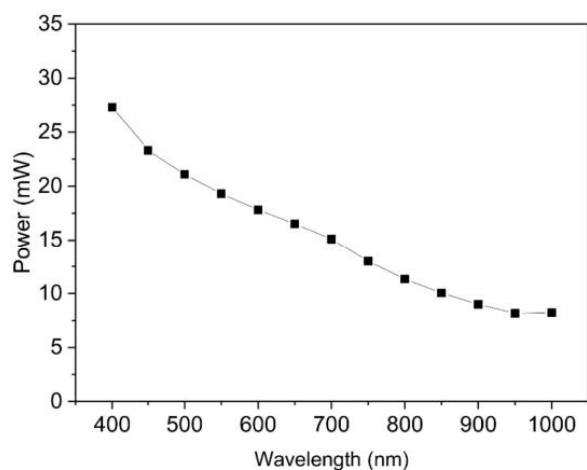


Figure 2. Characteristics of the microscope light between a wavelength of 400 nm and 1000 nm inducing light conditions during the electrical measurements. The Pt/ZnO/Pt cantilevered chip is placed at a distance of 10 cm from the light source.

The open and short calibration of the impedance analyser was realized prior to the measurements to remove the contribution of the cables and connections related to the device. Concerning the (C-V) and (G-V) measurements, the voltage was linearly swept between -10 V and 10 V, with a step voltage of 100 mV, for defined frequency values of 20 Hz, 60 Hz, 100 Hz, 500 Hz, 1 kHz, 10 kHz, 100 kHz and 1 MHz. Additional measurements were realized at lower frequencies where the above-mentioned NC phenomena are more prone to appear. Regarding the (C-f) and (G-f) measurements, the frequency was varied with a logarithmic sweep between 20 Hz and 1 MHz, for defined bias voltage values of 0 V, 500 mV, 1 V, 2 V, 4 V, 6 V, 8 V and 10 V. The (I-V) measurements were performed with an electrometer (6517B Electrometer/High Resistance Meter, Keithley Instruments, Solon, Ohio, USA) controlled by software (Labber, Lab Control Software Scandinavia AB, Vaxjo, Sweden). Additional (C-V) and (G-V) measurements were performed by bending the polyimide cantilevers upwards with a precise displacement, leading to the generation of controlled compressive strain steps calculated in the clamped area of the sensors. The upward bending of the polyimide cantilevers is shown in Figure 1b. The method of strain calculation is detailed in our previous work [38].

3. Results and Discussion

3.1. Structural and Electrical Properties of ZnO Thin Films

The growth rates per cycle (GPC) obtained for temperatures ranging from 60 °C to 120 °C, as well as the related cross-sectional micrographs depending on the growth temperature are illustrated on Figures 3 and 4, respectively.

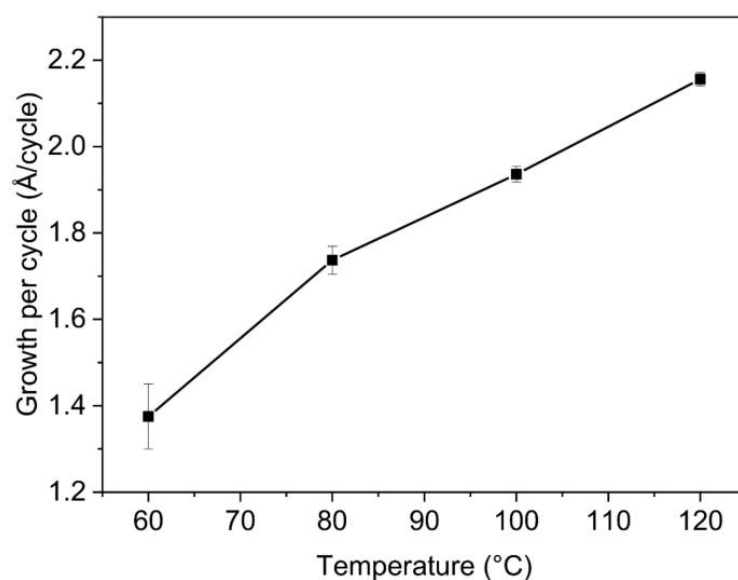


Figure 3. Growth rate per cycle (Å/cycle) of ZnO thin films by ALD for different deposition temperatures.

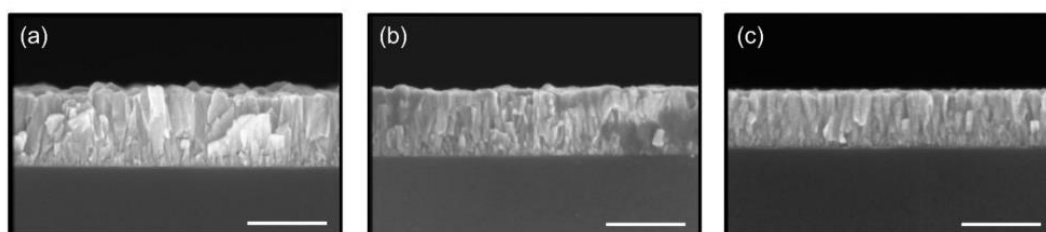


Figure 4. SEM cross-sectional images of ZnO thin films grown on Si substrates at (a) 100 °C, (b) 80 °C and (c) 60 °C. Each ZnO thin film was obtained with 1000 Atomic Layer Deposition (ALD) loops. The scale bar corresponds to 200 nm.

The GPC values obtained increase as deposition temperatures increase, indicating that the growth of ZnO thin films is outside the ALD temperature window for temperatures below 100 °C. This behaviour is typical of low reactivity reactions due to insufficient kinetic energy activation for the ligand exchange reactions, where low temperatures prevent complete reactions from occurring [42].

The SEM top view images of ZnO thin films grown by ALD on reference Si substrates with the associated grazing incident X-ray diffraction (GI-XRD) at a deposition temperature of (a) 100 °C, (b) 80 °C and (c) 60 °C are presented in Figure 5.

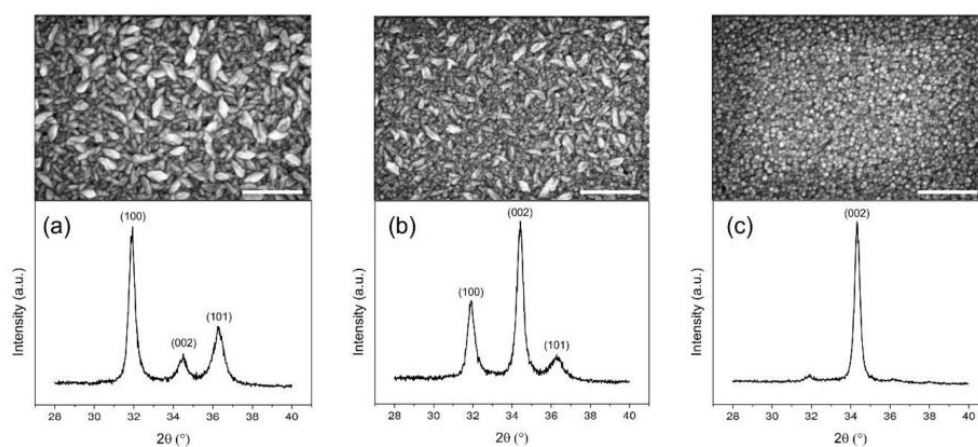


Figure 5. SEM top view images and associated GI-XRD diffraction patterns ($\omega = 0.3^\circ$) of ZnO thin films grown on Si substrates at a deposition temperature of (a) 100 °C, (b) 80 °C and (c) 60 °C. The obtained ZnO thin films were deposited with the same number of ALD loops (1000). The scale bar corresponds to 300 nm.

The ZnO thin films deposited are polycrystalline. At a temperature of 100 °C, a different distribution of grain orientations can be observed, split between the (100), (002) and (101) crystalline orientations. This is further confirmed by SEM top view images showing a distribution of wedge-like shaped crystallites parallel to the substrate and of fine columnar crystallites perpendicular to the substrate at this temperature. However, a transition occurs as the deposition temperature decreases, with the (002) crystalline substantially increasing at 80 °C and becoming dominant at 60 °C. This is consistent with the appearance of fine columnar crystallites considerably increasing as deposition temperatures decrease. This results in a significant change in the morphology of the ZnO thin films obtained at lower temperatures, where grains are predominantly oriented in the (002) direction perpendicular to the substrate, along the c-axis, which is especially important for piezoelectric applications in order to maximize the collective piezoelectric participation of ZnO grains with a similar piezoelectric strain coefficient value and orientation [43–45]. The same observations can be applied to the growth of ZnO thin films on the sensors' substrates, polyimide and platinum, as can be observed in Figures 6 and 7, respectively.

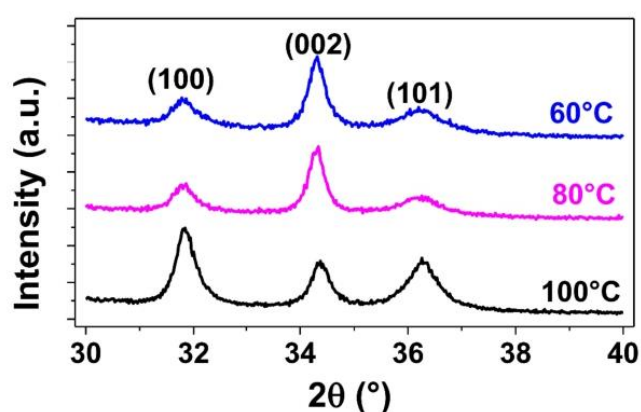


Figure 6. GI-XRD diffraction patterns ($\omega = 0.3^\circ$) of ZnO thin films grown on top of 75 μm thick polyimide substrates at 100 °C, 80 °C and 60 °C.

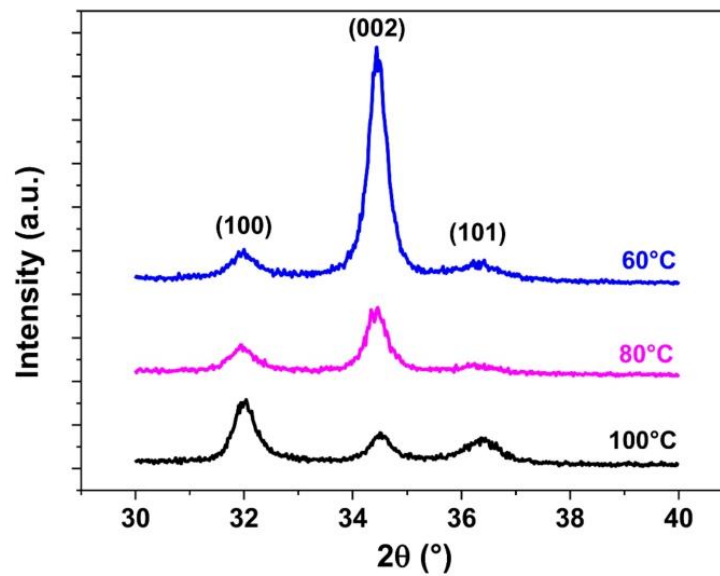


Figure 7. GI-XRD diffraction patterns ($\omega = 0.3^\circ$) of ZnO thin films grown on Si substrates coated with a 200 nm thick Pt layer at 100 °C, 80 °C and 60 °C.

Furthermore, the conformality of the ALD technique is demonstrated in Figure 8, where a ZnO layer is deposited on a polyimide substrate as well as on the top of Pt electrodes. An encapsulation layer of SU8 resin is deposited on top to protect the ZnO/Pt junction against the environmental conditions and to maintain the electrical performance.

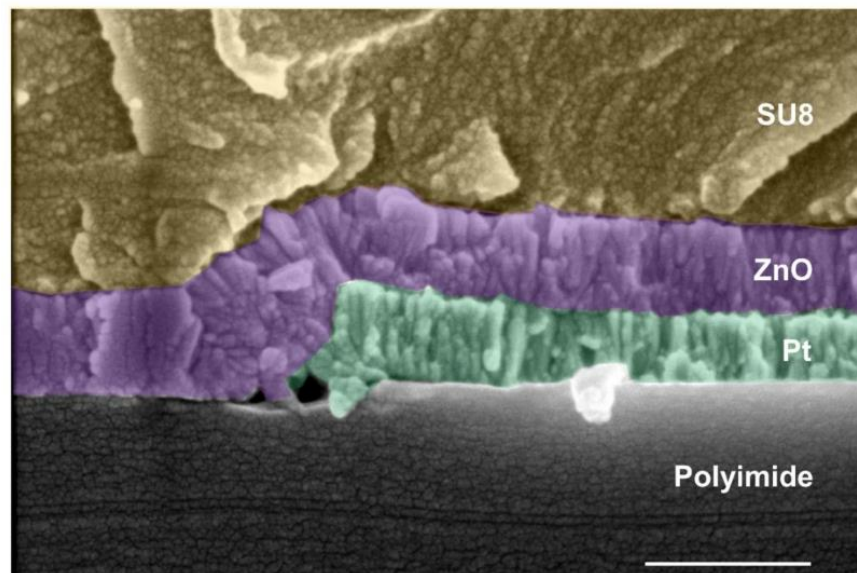


Figure 8. Cross-section showing the conformality of the ZnO thin film deposited by ALD on the polyimide substrate and the platinum metal electrodes. A SU8 resin top layer is deposited to protect the ZnO/Pt junction. The scale bar corresponds to 500 nm.

The resistivity of the ZnO thin films created was measured by the conventional four-points probe method on glass substrates [46]. The resistivity values obtained as a function of the deposition temperature are presented in Figure 9.

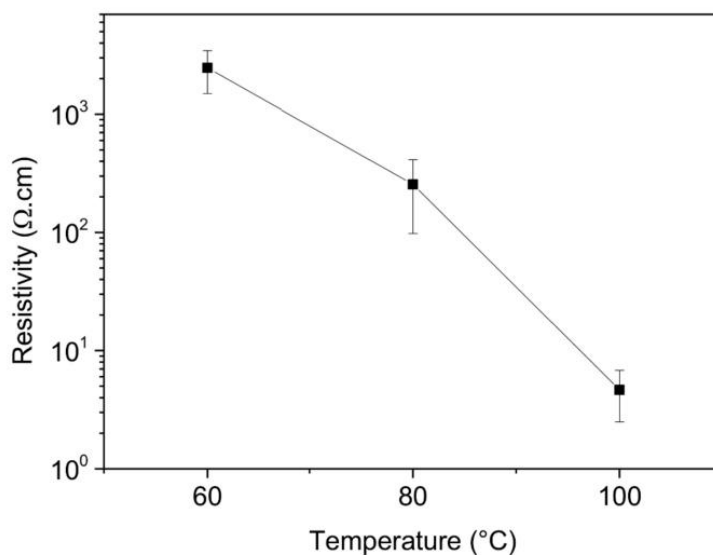


Figure 9. Evolution of the resistivity as a function of the deposition temperature for 150 nm thick ZnO thin films deposited at 60 °C, 80 °C and 100 °C on glass substrates, measured by the four-points probe method.

The resistivity increases from average values of 4.7 Ω·cm at 100 °C to 255.3 Ω·cm at 80 °C, reaching 2473.4 Ω·cm at 60 °C. These results confirm the increase of the resistivity for lower deposition temperatures by ALD. This last statement is well documented in the literature [47–49] and is linked to the reduction of ZnO defects (i.e., oxygen vacancies and zinc interstitials) at lower temperatures, as reported in our previous work [38]. This reduction in the defects contributes in turn to decrease the intrinsic n-type carrier concentration of the ZnO thin films at lower temperatures, within the aim of reaching appropriate values for a Schottky barrier formation with the Pt metal electrodes. The electrical and structural characteristics of the ZnO thin films deposited at 80 °C are thus well appropriated for their integration in MSM Schottky junctions.

3.2. Capacitance Modulation by Light

The capacitance-voltage (C-V) and capacitance-frequency (C-f) results of the Pt/ZnO/Pt Schottky junctions under the influence of dark and light conditions are presented in Figures 10 and 11, respectively.

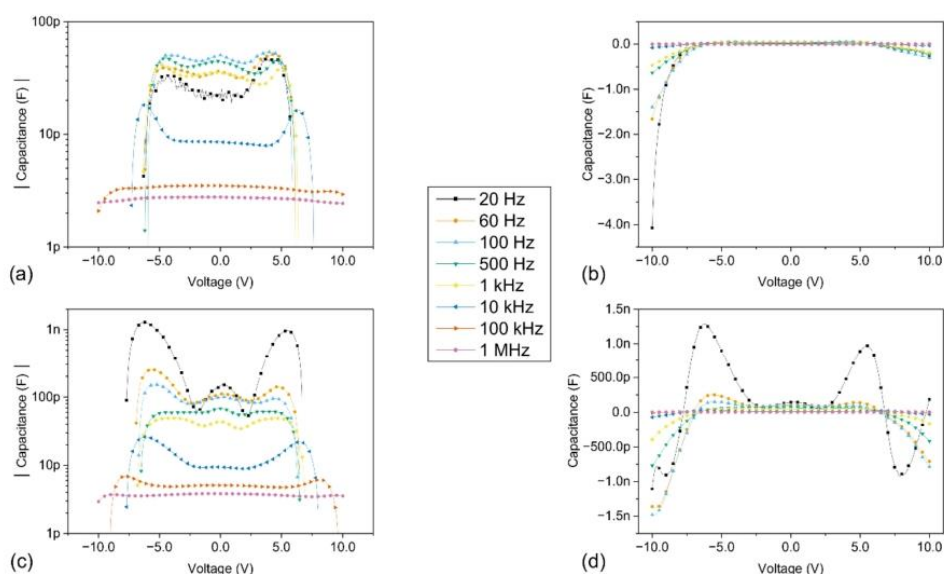


Figure 10. (C-V) characteristics under dark and light conditions, for different fixed frequencies of the AC modulation superimposed to the DC bias and ranging between 20 Hz and 1 MHz. The voltage was swept between -10 V and 10 V , with a step voltage of 100 mV ; (a) log scale under dark conditions; (b) linear scale under dark conditions; (c) log scale under light conditions; (d) linear scale under light conditions. Only the positive capacitance values are displayed in the graphs (a,c) with a log scale.

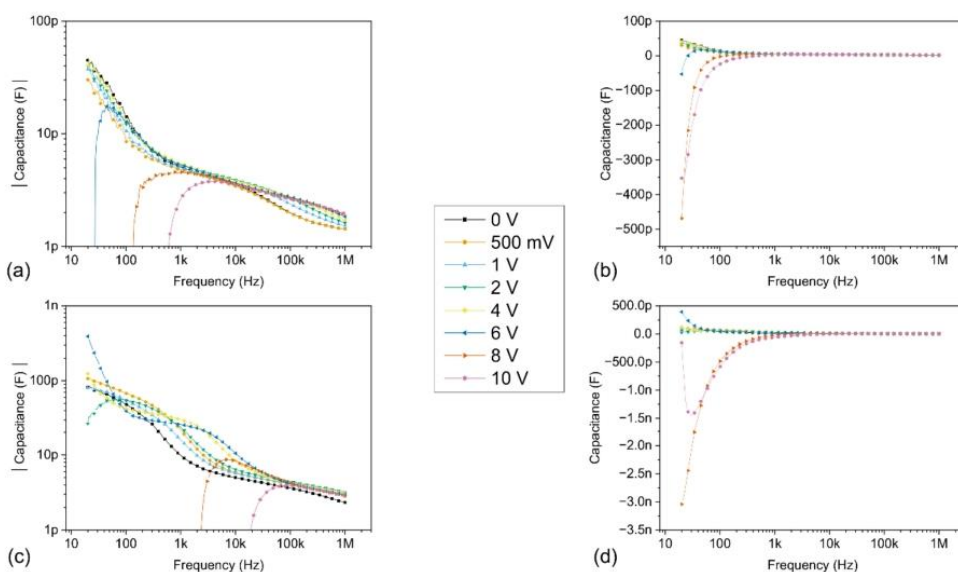


Figure 11. (C-f) characteristics under dark and light conditions for different fixed bias voltages ranging between 0 V and 10 V . The frequency was varied with a logarithmic sweep between 20 Hz and 1 MHz ; (a) log scale under dark conditions; (b) linear scale under dark conditions; (c) log scale under light conditions; (d) linear scale under light conditions. Only the positive capacitance values are displayed in the graphs (a,c) with a log scale.

From Figures 10 and 11, it can be clearly observed that the values of capacitance and conductance are dependent on both the frequency and the applied DC bias voltage.

Most noticeably, the measured capacitance values at lower frequencies are very different from the Schottky junction capacitance values, which predict a gradual decrease of the capacitance as the bias voltage and the depletion region are increased [50]. This dispersive behaviour of the measured capacitance values as a function of the frequency depends on the ability of the charge carriers to follow the AC signal and is directly linked with the interface trap states at the forward biased Schottky junction. At lower frequencies, the charges localized at the interface trap states are able to follow the AC signal and yield an excess capacitance, corresponding to C_{it} , whose value depends on the relaxation time of the interface trap states, and increases with decreasing frequencies. However, as the applied frequency is increased, the charges at the interface trap states are less and less able to follow the AC signal, which results in a decrease in the observed capacitance values, linked to the decrease of C_{it} . The capacitance values are reduced to a few pF at 1 MHz, effectively converging towards the value of the Schottky depletion region C_S .

Negative capacitance values are reported under the influence of both dark and light conditions, after reaching a threshold voltage value located above 5 V, which typically increases as the applied frequency is increased. Interestingly, no NC values are observed either for frequencies of 100 kHz and 1 MHz under dark conditions or for a frequency of 1 MHz under light conditions in the considered bias voltage range. The NC values are preceded by an increase in capacitance, localized in a peak with a positive capacitance value. Both the value and the broadening of this peak are significantly increased at lower frequencies, as well as in the presence of a light source. Furthermore, the positive capacitance values consistently increase in the presence of light over the entire bias voltage and frequency range explored. These results strongly suggest that both the presence of light and low frequencies favour the increase of the capacitance and the subsequent apparition of NC values in our devices, via the action of charges at the interface trap states. Additionally, the conductance-frequency (G-f) results under the influence of dark and light conditions are presented in Figure 12. These results reveal that the conductance values significantly increase in the presence of light over the entire bias voltage and frequency range explored.

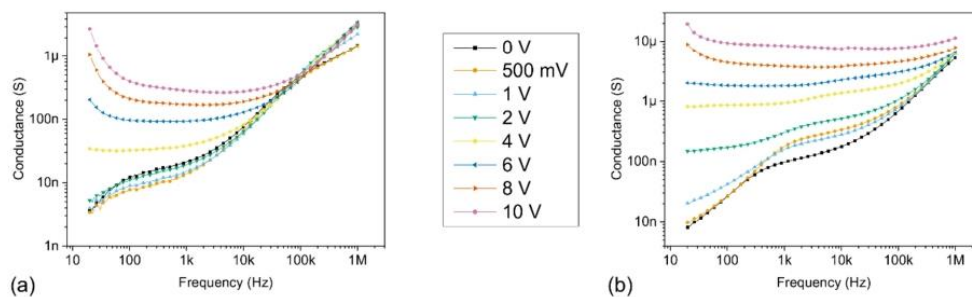


Figure 12. (G-f) characteristics under dark and light conditions for different fixed bias voltages ranging between 0 V and 10 V. The frequency was varied with a logarithmic sweep between 20 Hz and 1 MHz; (a) log scale under dark conditions; (b) log scale under light conditions.

The light source generates electron-hole pairs in the bulk of the semiconductor, which actively contribute to the conduction mechanisms of the MSM diodes. This is further confirmed by the (I-V) characteristics of the devices shown in Figure 13, where the current values measured with a DC bias increase by over two orders of magnitude in the presence of light.

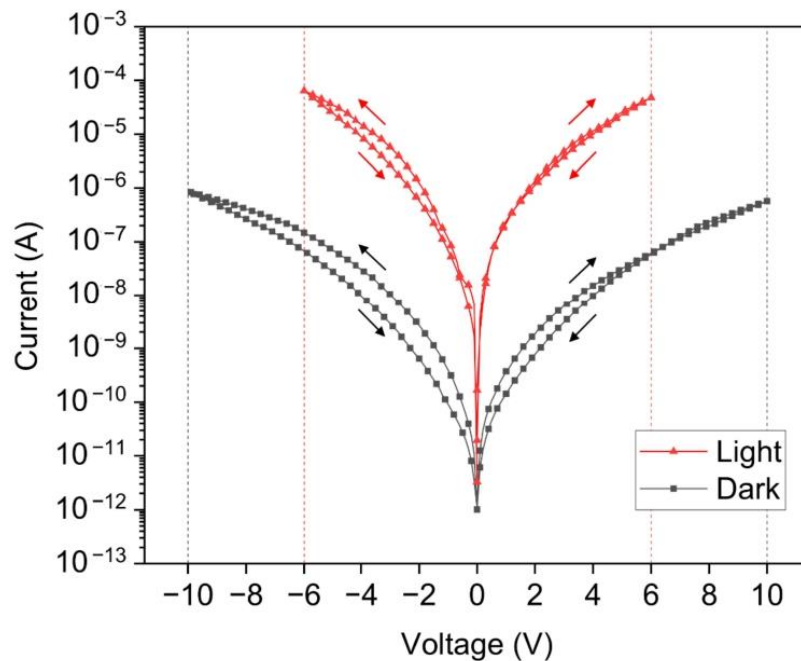


Figure 13. (I-V) characteristics under both dark and light conditions, measured with DC bias modulation. The current is represented on a logarithmic scale with absolute values. The current measurements were performed with an integration time of 200 ms, a step length of 100 mV, a sweep speed of $200 \text{ mV}\cdot\text{s}^{-1}$ and a delay of 300 ms between the step and the measurement. The voltage was swept for dark characteristics between -10 V and 10 V . The voltage was swept for light characteristics between -6 V and 6 V . The arrows indicate the parts of the curves corresponding to the forward and backward sweeps.

The hysteresis between the forward and backward sweep observed in the (I-V) curves in Figure 13 is linked to the filling of the interface trap states at the metal-semiconductor (MS) junctions. Indeed, during the forward sweeping (i.e., from zero bias to a higher bias voltage), the interface trap states are gradually filled up as the current and the bias voltage are increased. However, during the backward sweep (i.e., from a high bias voltage to zero bias), the initial high bias voltage is directly filling up the interface trap states. Some of these trap states remained filled up during the rest of the backward sweep to 0 V , which led to a lower density of interface trap states actively involved in the current conduction mechanism, reducing the current in the devices. This is linked to the different capture and re-emission charge carriers' dynamics at the MS junctions, resulting in the hysteresis observed in the (I-V) curves. When the frequency is increased with an AC bias voltage modulation, the density of the interface trap states that respond is further reduced, leading to an increase in the hysteresis, as reported in our previous work [38]. A similar phenomenon can explain the discrepancy in the (C-V) characteristics presented in Figure 10 between the negative and positive bias voltage domains. Interestingly, the negative capacitance (NC) values reached higher values in the backward sweep than in the forward sweep. As the voltage is swept from a negative value up to a positive voltage value (i.e., from -10 V to 10 V), the different re-emission and capture charge carrier time constants are respectively involved in the negative and positive bias voltage regions of the (C-V) curves. As more charge carriers remain trapped during the re-emission process (i.e., from -10 V to zero bias), the capacitance values are slightly increased, especially in the presence of a light source.

As previously mentioned, the exact origin of the NC phenomena is still a matter of discussion in the literature. When a sufficiently large bias is applied, the drift component of the minority carriers (i.e., holes in our devices with n-type ZnO) becomes increasingly important, which can lead to an increase of their injection efficiency. However, the injection of minority carriers remains limited in wide bandgap semiconductors [41,51], such as zinc oxide with a bandgap of 3.3 eV [47]. Moreover, it is well known that the current transport in metal-semiconductor contacts is mainly due to majority carriers (i.e., electrons in our devices with n-type ZnO). Furthermore, a significant excess capacitance can be observed at lower frequencies even when small bias voltages are applied. Based on these considerations and the above-mentioned results, the NC phenomena observed have been linked with electrons that are captured and re-emitted at the interface trap states. The origin of NC values can be understood in terms of the variation of the interface charge density, by considering a continuous distribution of energy levels at the interface as proposed by Bardeen [52]. An increase in the capacitance values is thus linked to an increase in the interface charge density—or, in other words, in the electron capture process. In contrast, a decrease in the capacitance means that a loss of charges occurs at the interface, i.e., that electrons are being re-emitted or ejected from the interface trap states. Ultimately, negative capacitance values mean that the loss of electrons prevails over their capture at the MS interface. This simple model can be applied to explain the variation of the (C-V) curves in our devices for both dark and light conditions. As stated by Wu et al. [1], an impact-loss process has to be accounted for. When the electric field is increased, more and more hot electrons with higher energy are injected at the occupied interface trap states below the Fermi level, colliding with trapped electrons and creating empty states, which is linked to the loss of charges. Consequently, upon reaching a threshold voltage value, the capacitance values start to increase until they reach a peak of positive capacitance value. In this part of the curves, the electrons acquire enough energy to overcome the Schottky barrier and are captured at the interface trap states. As the bias voltage increases, more and more electrons are involved in the conduction mechanism. This results in an accumulation of charges at the interface, which leads to the increase of the capacitance values.

In the presence of a light source, supplementary electrons are photogenerated in the bulk of the semiconductor and injected at the MS interface, which significantly increases the accumulated charges at the interfaces, thus increasing the capacitance and its peak value. This is confirmed by the increase of both the capacitance and conductance values in the presence of light occurring at a lower bias voltage when compared to the dark characteristics. After reaching its peak value, the capacitance quickly decreases, indicating that the impact-loss process is growing, as electrons are being ejected from the interface trap states. Subsequently, negative capacitance values appear in the devices, meaning that the loss of electrons due to the impact-loss process exceeds the capture of electrons at the interface trap states. These phenomena are further marked at low frequencies, as more electrons are able to follow the AC signal through the interface trap states. A detailed comparison between the dark and light characteristics for every frequency and bias voltage in the study is provided in the Supplementary Materials, with Figures S1–S3 corresponding to the (C-V), (C-f) and (G-f) characteristics, respectively.

3.3. Capacitance Modulation by Light and Mechanical Strain

Additional capacitance and conductance were performed by taking advantage of the piezotronic nature of our devices. The upward bending of the polyimide cantilevers leads to the generation of controlled compressive strain steps at the clamped area of the piezotronic sensors, where the Pt/ZnO/Pt Schottky junctions are located. The strain induces the creation of localized piezoelectric polarization charges at the MS interfaces, which, in turn, effectively modulate the height of the Schottky barriers [53]. This has a direct impact on the electrical behaviour of the sensors by exponentially tuning the electrical current [38] and thus the flow of electrons passing through the MSM junctions. As the electrons are directly involved in the capacitive response of our devices at the MS interface, the capacitance is

thus expected to be modulated with the strain accordingly. For a better visualization of the impact of the strain on the peak capacitance and on the NC values, measurements were performed at 20 Hz, after extended exposure to a light source. The results are presented in Figure 14.

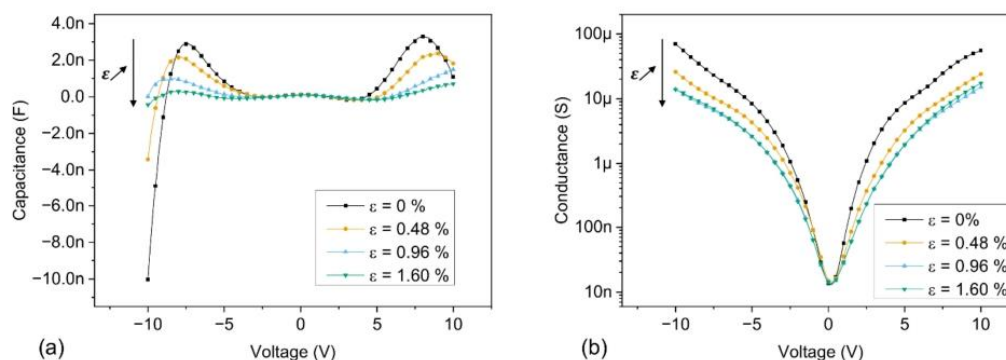


Figure 14. (C-V) and (G-V) characteristics under light conditions, for a fixed frequency of 20 Hz, with controlled compressive strain steps imposed on the junctions. The voltage was swept between -10 V and 10 V, with a step voltage of 100 mV; (a) (C-V) characteristics, linear scale; (b) (G-V) characteristics, log scale.

Due to the application of a compressive strain, negative piezoelectric polarization charges are generated at the MS interfaces, increasing the height of the Schottky barrier. In turn, the electrical current is reduced, which reduces as well the flow of electrons passing through the MSM junctions. Consequently, the capacitance and conductance values are both reduced as the compressive strain imposed to the devices gradually increases, as can be seen in Figure 14. Most noticeably, the peak capacitance values decrease significantly as the strain is increased, while the apparition of NC values is delayed due to higher bias voltages. However, the impact of strain on the capacitance modulation becomes less and less significant both as the frequency increases and in dark conditions, as shown in Figure S4 in the Supplementary Materials. This simple method thus allows for an effective modulation of the capacitance by tuning the flow of electrons involved in the NC associated phenomena.

4. Conclusions

In conclusion, we report on the evidence of negative capacitance phenomena occurring at the interface of Schottky junctions made from the ALD growth of 300 nm thick ZnO thin films deposited on top of 200 nm thick Pt interdigitated electrodes. These metal-semiconductor-metal junctions are integrated at the clamped area of millimetre-sized polyimide cantilevers in piezotronic strain microsensors. The capacitance and conductance characteristics of the devices were studied over an extended bias voltage and frequency range, in the dark, as well as in the presence of a light source. We report on the observation of negative capacitance values over a wide frequency range, namely between 20 Hz and 1 MHz. The origin of the apparition of negative capacitance values has been linked to the injection of hot electrons due to an impact-loss process at the interface trap states of the metal-semiconductor junction. The NC values are preceded by a peak increase of the positive capacitance value, linked to the accumulation of trapped electrons at the interface trap states. These phenomena significantly increase at lower frequencies, as well as in the presence of a light source. Additionally, we propose an original way to modulate the capacitance and conductance characteristics by applying a mechanical strain to the devices, which effectively tunes the flow of electrons involved in the NC-associated phenomena. Thus, we propose a device that is simple to process by conventional microfabrication facilities and where the capacitance values can be modulated over a wide frequency range

via the action of light and strain, while using easy-to-process materials. These results open up new perspectives and applications in the miniaturization of highly sensitive and low power consumption environmental sensors, as well as for broadband impedance matching by tank circuit in radio frequency applications. The inductance-like behaviour of capacitors with negative capacitance values is particularly interesting for the possibility of replacing bulky inductors that are challenging to process.

Supplementary Materials: The following are available online at <https://www.mdpi.com/1424-8220/21/6/2253/s1>, Figure S1: (C-V) characteristics under both dark and light conditions, for different fixed frequencies of the AC modulation superimposed on the DC bias and ranging between 20 Hz and 1 MHz. The voltage was swept between -10 V and 10 V, with a step voltage of 100 mV; (a) 20 Hz, log scale; (b) 20 Hz, linear scale; (c) 60 Hz, log scale; (d) 60 Hz, linear scale; (e) 100 Hz, log scale; (f) 100 Hz, linear scale; (g) 500 Hz, log scale; (h) 500 Hz, linear scale; (i) 1 kHz, log scale; (j) 1 kHz, linear scale; (k) 10 kHz, log scale; (l) 10 kHz, linear scale; (m) 100 kHz, log scale; (n) 100 kHz, linear scale; (o) 1 MHz, log scale; (p) 1 MHz, linear scale. Figure S2: (C-f) characteristics under both dark and light conditions for different fixed bias voltages ranging between 0 V and 10 V. The frequency was varied with a logarithmic sweep between 20 Hz and 1 MHz; (a) 0 V, log scale; (b) 0 V, linear scale; (c) 500 mV, log scale; (d) 500 mV, linear scale; (e) 1 V, log scale; (f) 1 V, linear scale; (g) 2 V, log scale; (h) 2 V, linear scale; (i) 4 V, log scale; (j) 4 V, linear scale; (k) 6 V, log scale; (l) 6 V, linear scale; (m) 8 V, log scale; (n) 8 V, linear scale; (o) 10 V, log scale; (p) 10 V, linear scale. Figure S3: (G-f) characteristics under both dark and light conditions for different fixed bias voltages ranging between 0 V and 10 V. The frequency was varied with a logarithmic sweep between 20 Hz and 1 MHz; (a) 0 V, log scale; (b) 500 mV, log scale; (c) 1 V, log scale; (d) 2 V, log scale; (e) 4 V, log scale; (f) 6 V, log scale; (g) 8 V, log scale; (h) 10 V, log scale. Figure S4: (C-V) characteristics under dark and light conditions for different fixed frequencies, with controlled compressive strain steps imposed on the junctions. The voltage was swept between -10 V and 10 V, with a step voltage of 100 mV; (a) dark conditions, 20 Hz; (b) under light conditions, 20 Hz; (c) dark conditions, 1 kHz; (d) under light conditions, 1 kHz; (e) dark conditions, 1 MHz; (f) under light conditions, 1 MHz.

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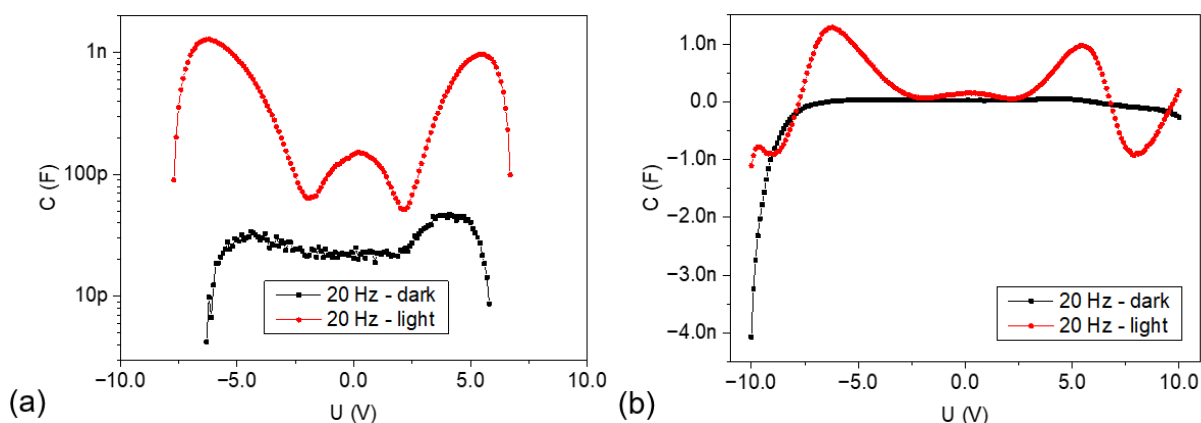
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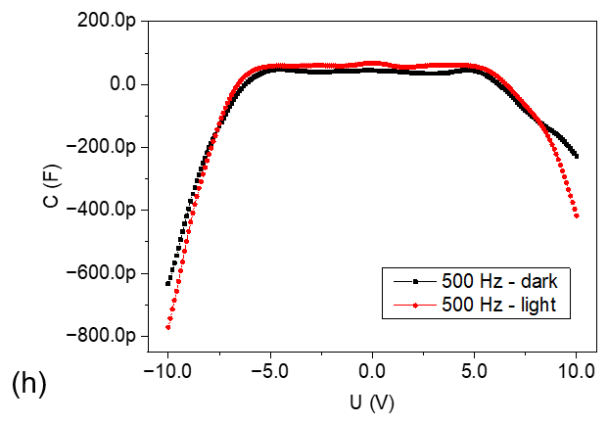
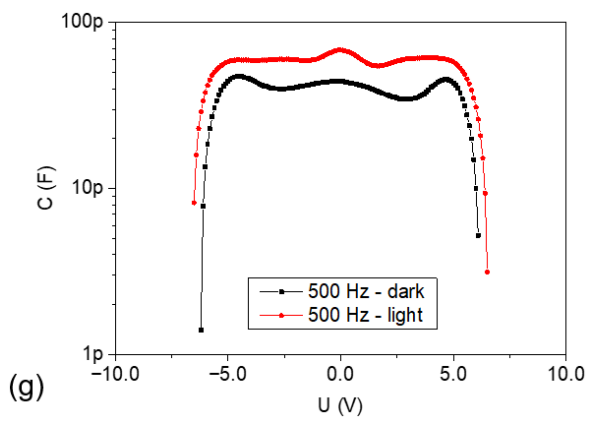
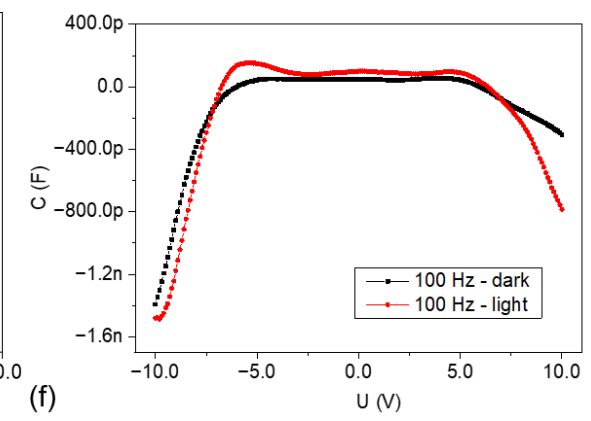
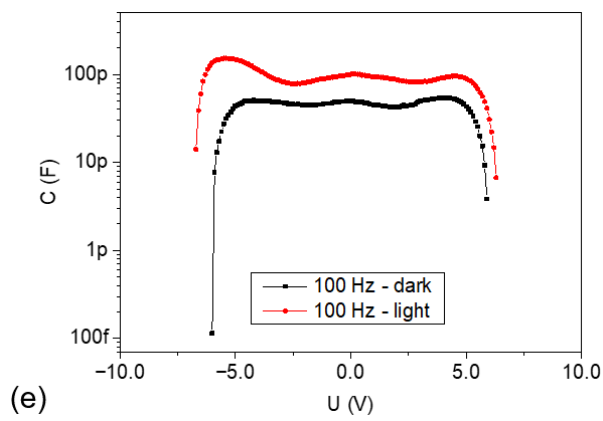
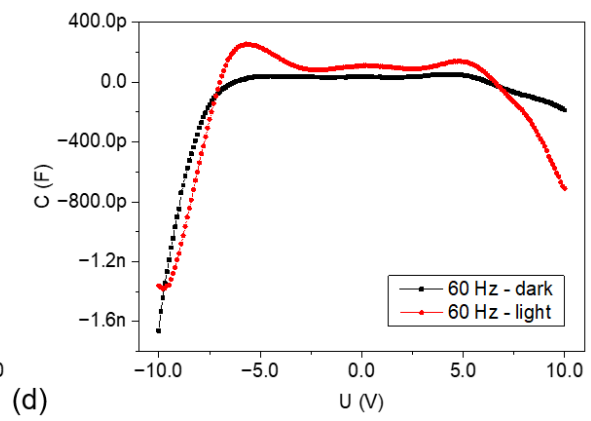
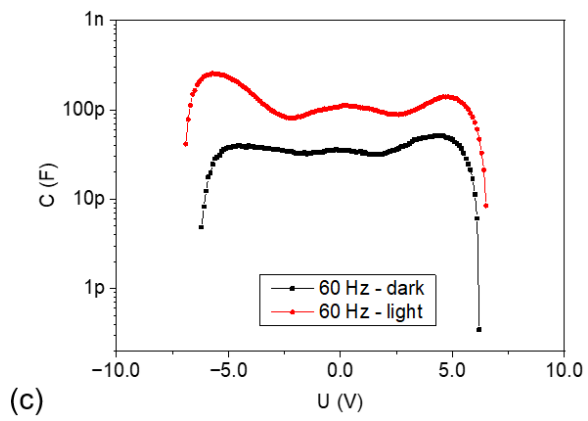
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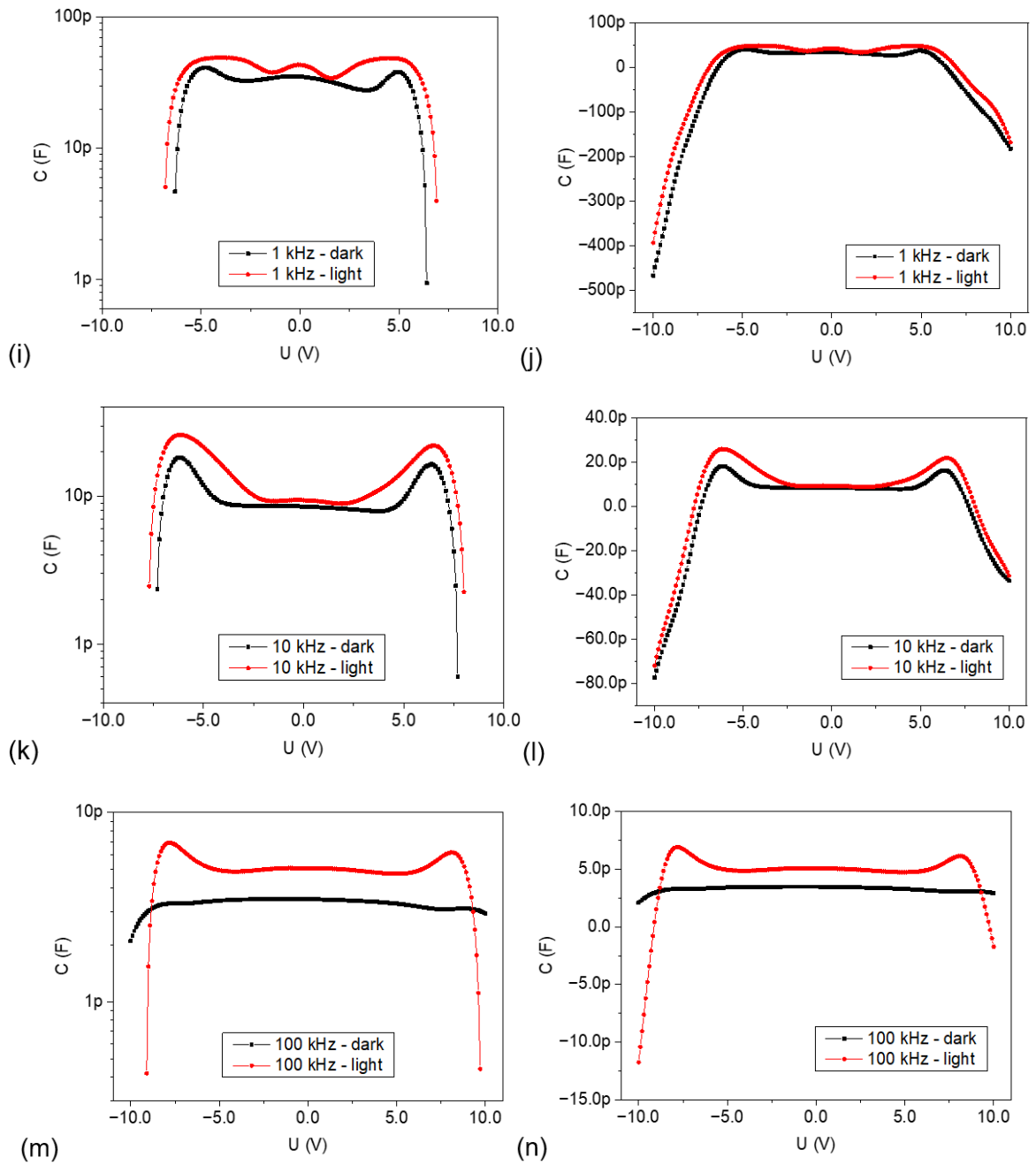
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Supplementary Materials

Evidence of Negative Capacitance and Capacitance Modulation by Light and Mechanical Stimuli in Pt/ZnO/Pt Schottky Junctions







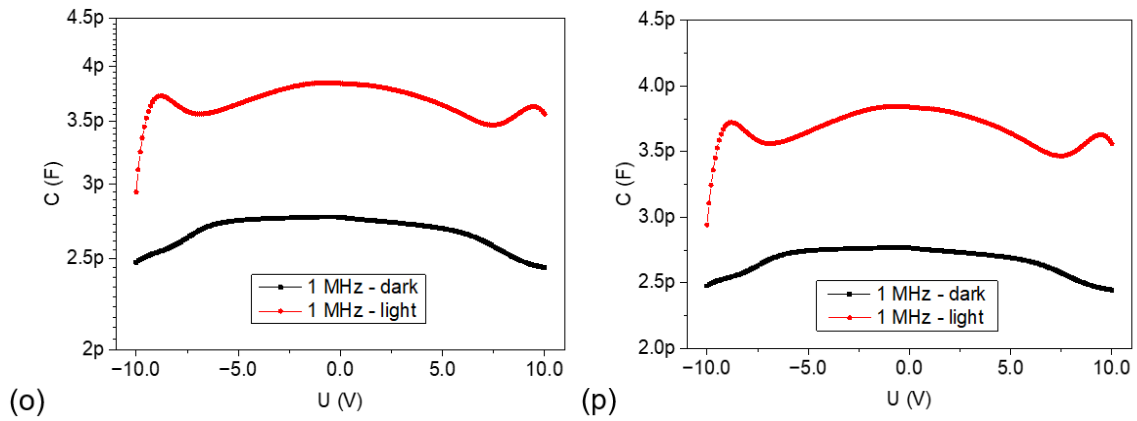
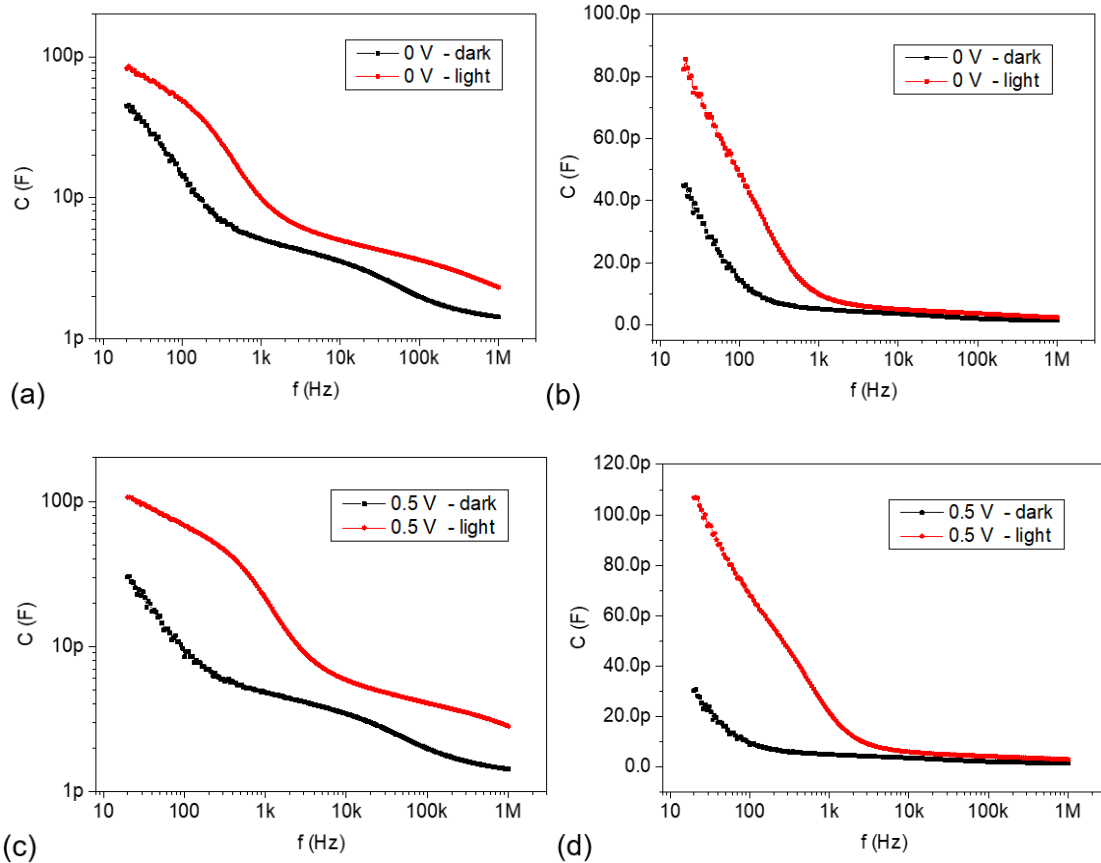
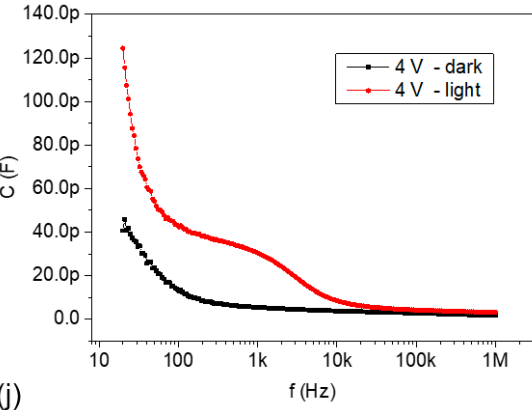
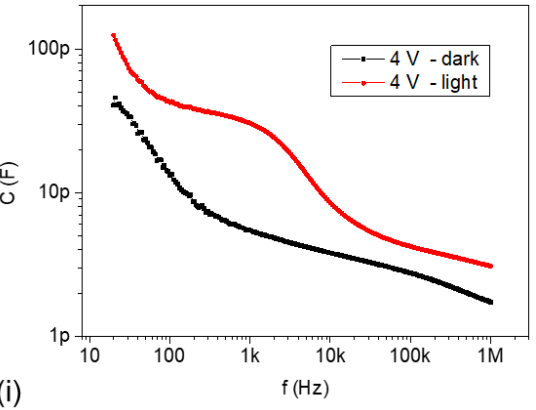
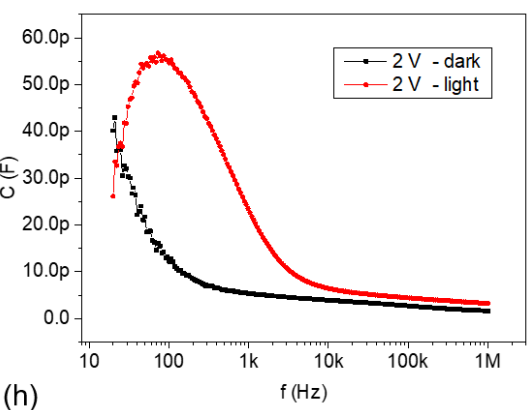
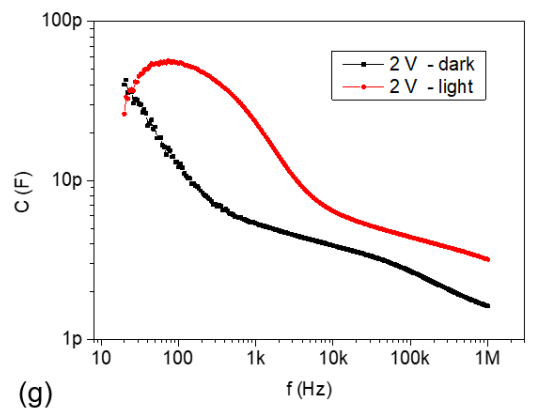
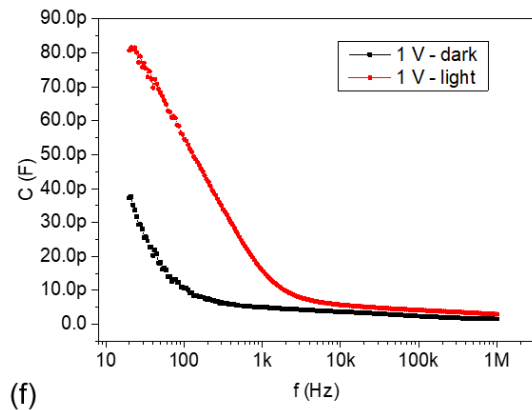
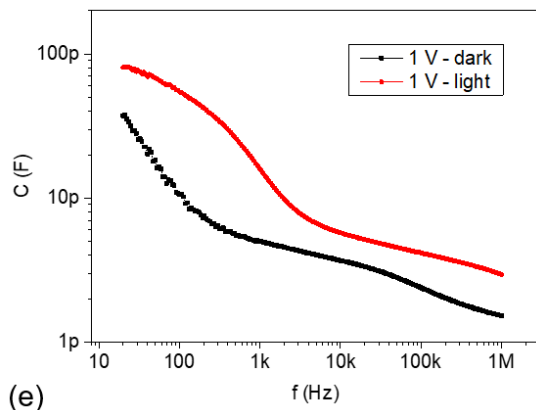


Figure S1. (C-V) characteristics under both dark and light conditions, for different fixed frequencies of the AC modulation superimposed to the DC bias and ranging between 20 Hz and 1 MHz. The voltage was swept between -10 V and 10 V, with a step voltage of 100 mV; (a) 20 Hz, log scale; (b) 20 Hz, linear scale; (c) 60 Hz, log scale; (d) 60 Hz, linear scale; (e) 100 Hz, log scale; (f) 100 Hz, linear scale; (g) 500 Hz, log scale; (h) 500 Hz, linear scale; (i) 1 kHz, log scale; (j) 1 kHz, linear scale; (k) 10 kHz, log scale; (l) 10 kHz, linear scale; (m) 100 kHz, log scale; (n) 100 kHz, linear scale; (o) 1 MHz, log scale; (p) 1 MHz, linear scale.





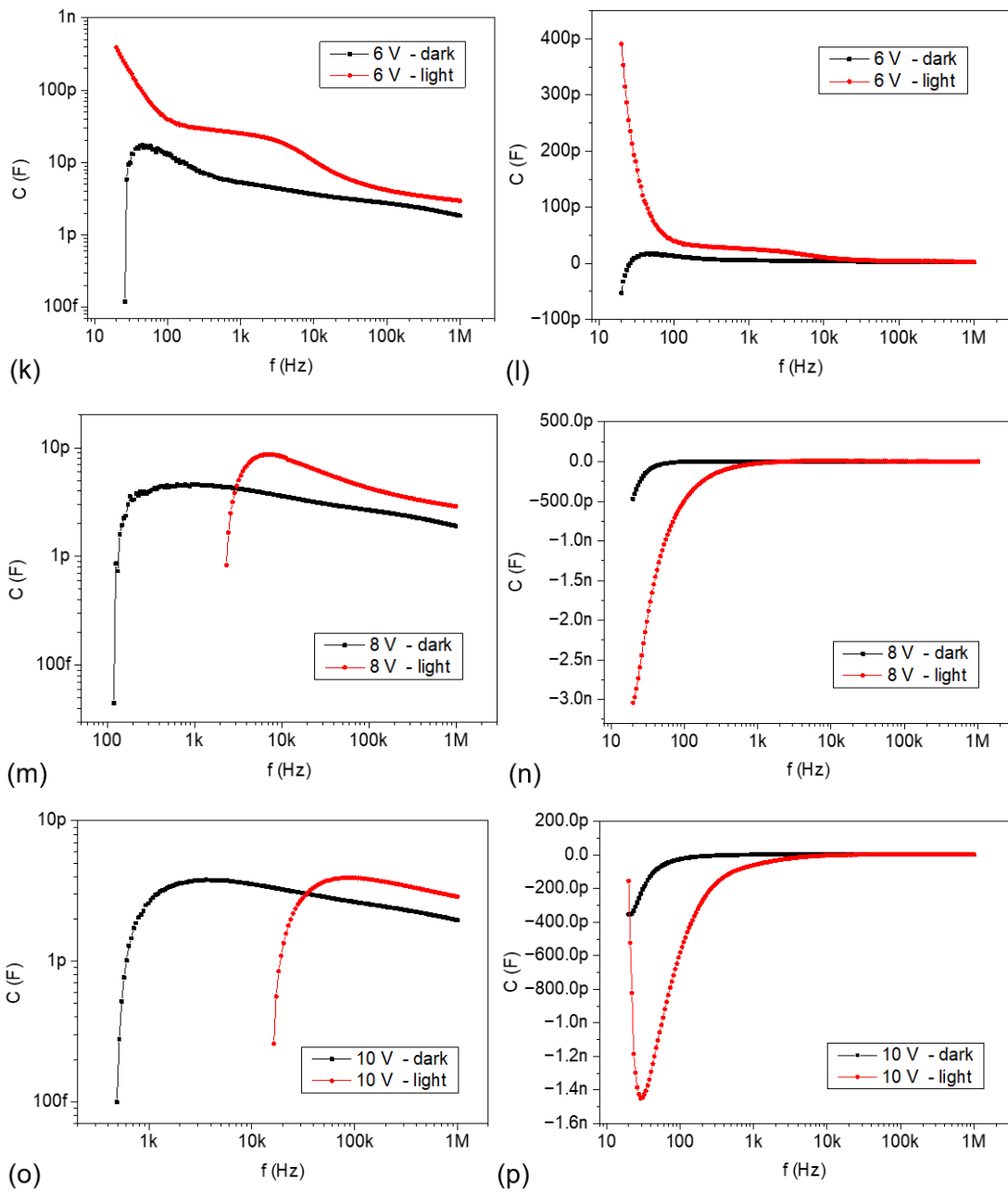
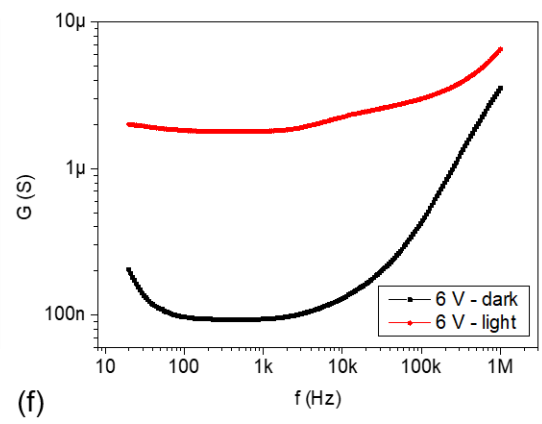
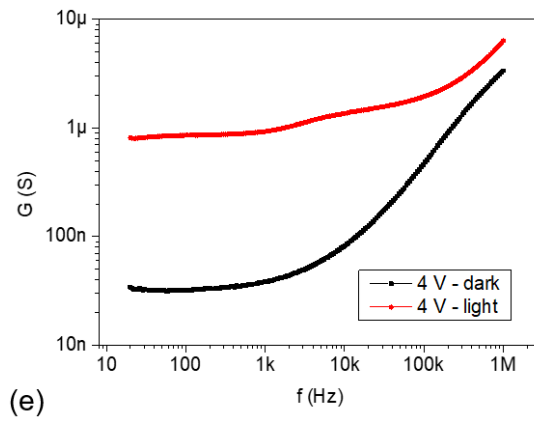
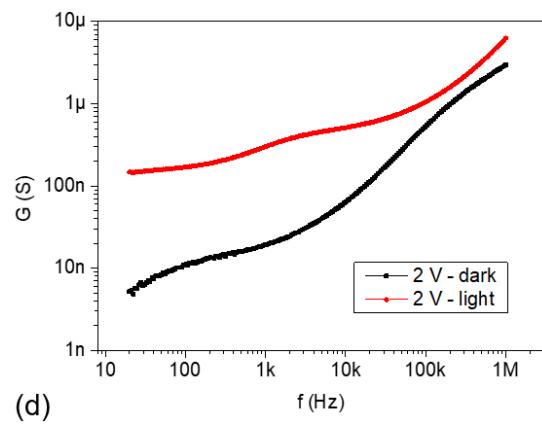
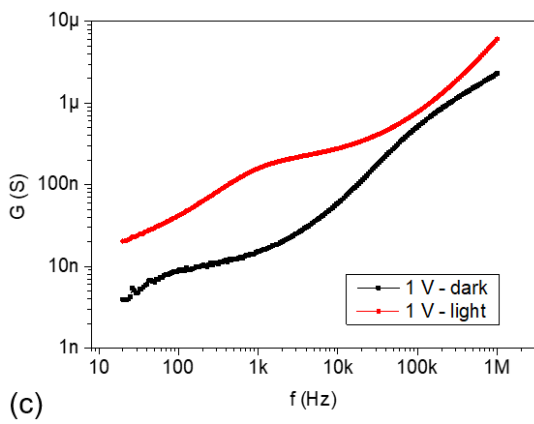
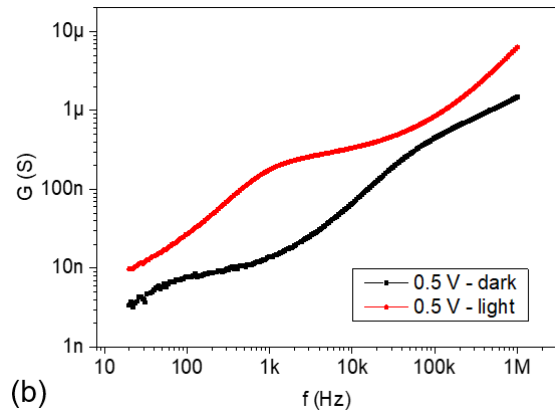
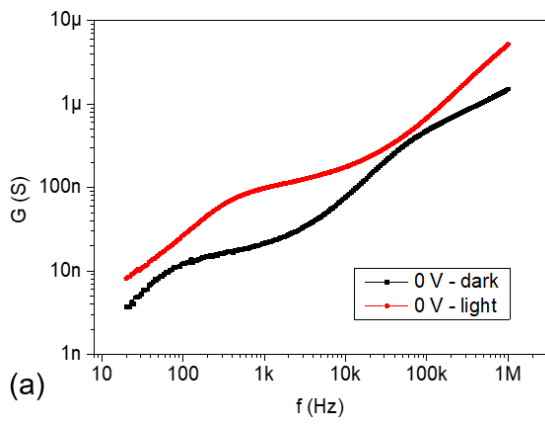


Figure S2. (C-f) characteristics under both dark and light conditions for different fixed bias voltages ranging between 0 V and 10 V. The frequency was varied with a logarithmic sweep between 20 Hz and 1 MHz; (a) 0 V, log scale; (b) 0 V, linear scale; (c) 500 mV, log scale; (d) 500 mV, linear scale; (e) 1 V, log scale; (f) 1 V, linear scale; (g) 2 V, log scale; (h) 2 V, linear scale; (i) 4 V, log scale; (j) 4 V, linear scale; (k) 6 V, log scale; (l) 6 V, linear scale; (m) 8 V, log scale; (n) 8 V, linear scale; (o) 10 V, log scale; (p) 10 V, linear scale.



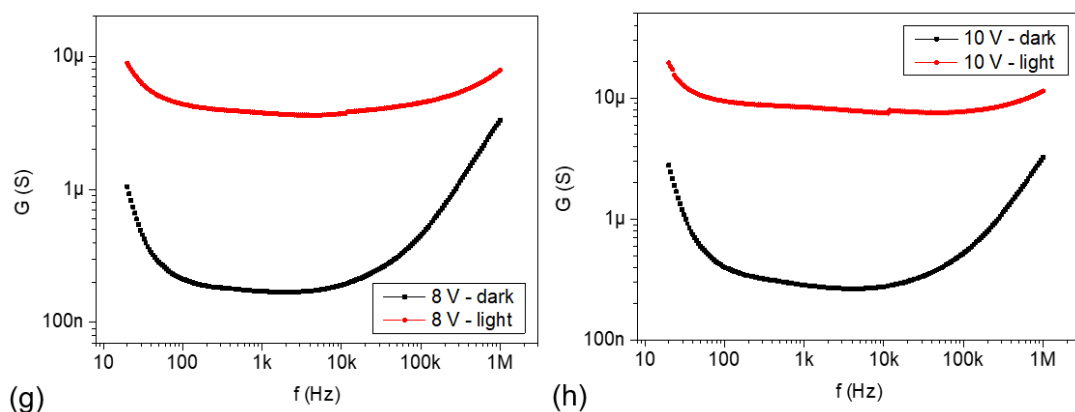
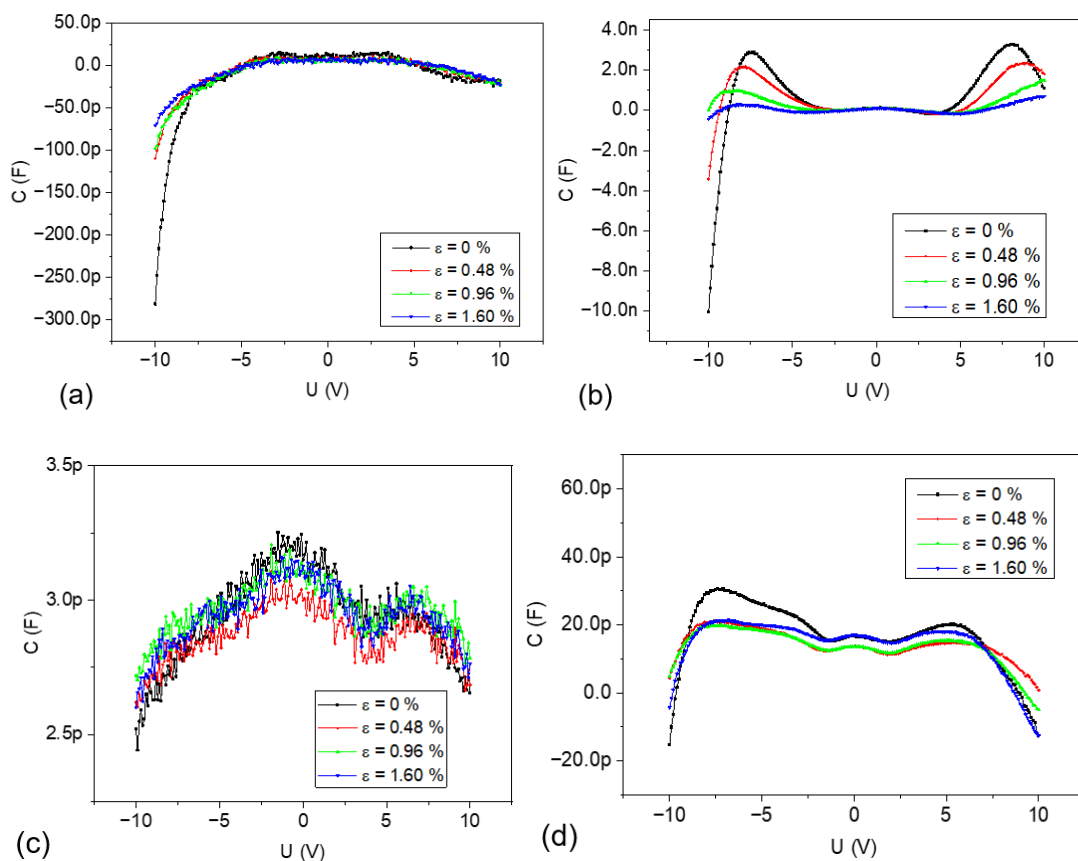


Figure S3. (G-f) characteristics under both dark and light conditions for different fixed bias voltages ranging from 0 V and 10 V. The frequency was varied with a logarithmic sweep between 20 Hz and 1 MHz; (a) 0 V, log scale; (b) 500 mV, log scale; (c) 1 V, log scale; (d) 2 V, log scale; (e) 4 V, log scale; (f) 6 V, log scale; (g) 8 V, log scale; (h) 10 V, log scale.



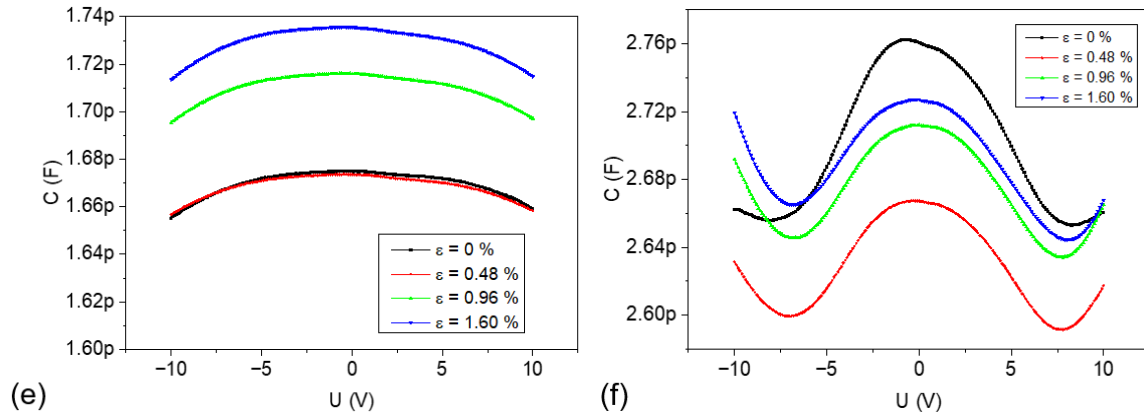


Figure S4. (C-V) characteristics under dark and light conditions for different fixed frequencies, with controlled compressive strain steps imposed on the junctions. The voltage was swept between -10 V and 10 V, with a step voltage of 100 mV; **(a)** dark conditions, 20 Hz; **(b)** light conditions, 20 Hz; **(c)** dark conditions, 1 kHz; **(d)** light conditions, 1 kHz; **(e)** dark conditions, 1 MHz; **(f)** light conditions, 1 MHz.

C. Experimental protocol for the determination of noise spectral density values

As detailed in the main body of the manuscript, noise measurements were performed using the Fast Fourier Transform (FFT) of the oscilloscope (WaveSurfer 3024, Teledyne LeCroy). A small Faraday cage was designed and mounted on the AFM nose to shield the sensors against the surrounding electromagnetic noises. This appendix thus aims at explaining the experimental protocol applied for the extraction of the noise spectral density values. The measurements performed with reference metal resistors will first be detailed, followed by the extraction of the noise spectral density values of the piezotronic sensors applied to specific experimental conditions.

Experimental protocol:

In order to assess and quantify the different types of noise, power spectrums curves were first acquired (in dBm, i.e. decibels relative to a milliWatt). The values from the power spectrum curves were then converted in units of Watt, using the equation:

$$P(W) = \frac{10^{\frac{P(\text{dBm})}{10}}}{1000} = 10^{\left(\frac{P(\text{dBm})-30}{10}\right)} \quad (\text{C.1})$$

The obtained power in Watts can be further expressed as a function of the squared tension V^2 and the resistance R_{line} (corresponding to the line impedance), as:

$$P(W) = \frac{V^2}{R_{\text{line}}} \quad (\text{C.2})$$

Which yields:

$$V^2 = P(W) \cdot R_{\text{line}} \quad (\text{C.3})$$

The squared value of the current I^2 can be subsequently obtained by dividing V^2 by the squared gain G^2 (i.e. the amplification) of the transimpedance preamplifier, as:

$$I^2 = \frac{V^2}{G^2} \quad (\text{C.4})$$

Finally, the noise spectral density S is obtained by dividing the squared value of the current I^2 by Δf , defined as the resolution bandwidth of the oscilloscope.

$$S = \frac{I^2}{\Delta f} \quad (\text{C.5})$$

Application with a 10 MΩ resistor:

Reference metal resistors of known values (100 kΩ, 1 MΩ and 10 MΩ) were used to ensure that the experimental values of the noise spectral density background measured without any bias voltage corresponded to the expected theoretical value of the Johnson-Nyquist white noise density. The methodology previously described is here applied to the 10 MΩ resistor, whose resistance is denoted as R_R and its noise spectral density values as S_R .

The theoretical value of the Johnson-Nyquist white noise density S_R^{th} is expressed and calculated as:

$$S_R^{\text{th}} = \frac{4 \cdot k_B \cdot T}{R_R} = \frac{4 \cdot 1.38064852 \times 10^{-23} \cdot 300}{10^7} = 1.66 \times 10^{-27} \text{ A}^2 \cdot \text{Hz}^{-1} \quad (\text{C.6})$$

This theoretical value is compared to the value S_R^{exp} calculated experimentally, following equations (C.1) to (C.5). Using the measured value of the power spectrum

curve $P(\text{dBm}) = -67 \text{ dBm}$, as well as $R_{\text{line}} = 50 \ \Omega$, $G = 10^9$ and $\Delta f = 6 \text{ Hz}$, the numerical applications yield:

$$P(W) = 10^{\left(\frac{P(\text{dBm})-30}{10}\right)} = 10^{\left(\frac{-67-30}{10}\right)} = 2 \times 10^{-10} \text{ W}$$

$$V^2 = P(W) \cdot R_{\text{line}} = 2 \cdot 10^{-10} \times 50 = 10^{-8} \text{ V}^2$$

$$I^2 = \frac{V^2}{G^2} = \frac{10^{-8}}{(10^9)^2} = 10^{-26} \text{ A}^2$$

$$S_R^{\text{exp}} = \frac{I^2}{\Delta f} = \frac{1 \cdot 10^{-26}}{6} = 1.66 \times 10^{-27} \text{ A}^2 \cdot \text{Hz}^{-1}$$

The correspondence between the theoretical and experimental values of the noise spectral density ($S_R^{\text{th}} = S_R^{\text{exp}}$) for the $10 \text{ M}\Omega$ resistor thus confirms the validity of the experimental protocol.

Application to the piezotronic sensors:

The experimental protocol described in this appendix was applied to the piezotronic strain sensors for the calculation of their noise spectral density values. As described in section 4.3.3, the noise analysis was performed on sensors with ALD-grown ZnO thin films deposited at temperatures of $80 \text{ }^\circ\text{C}$ and $60 \text{ }^\circ\text{C}$, while using different DC bias voltage values. This application will be limited to a defined set of experimental conditions, i.e. for ZnO thin films deposited at $80 \text{ }^\circ\text{C}$ with an applied DC bias voltage value of 6 V . The following parameters were used for the calculation: $R_{\text{line}} = 50 \ \Omega$, $G = 10^4$ and $\Delta f = 12 \text{ Hz}$. As the noise spectral density values of the piezotronic sensors depend on the applied frequency, numerical applications were carried out for every measurement point in the frequency domain. However, it is worth noting that the gain value of the preamplifier was adapted accordingly to the imposed DC bias voltage. The power spectrum curve obtained corresponding to the above-mentioned experimental conditions is displayed in Fig. C.1.

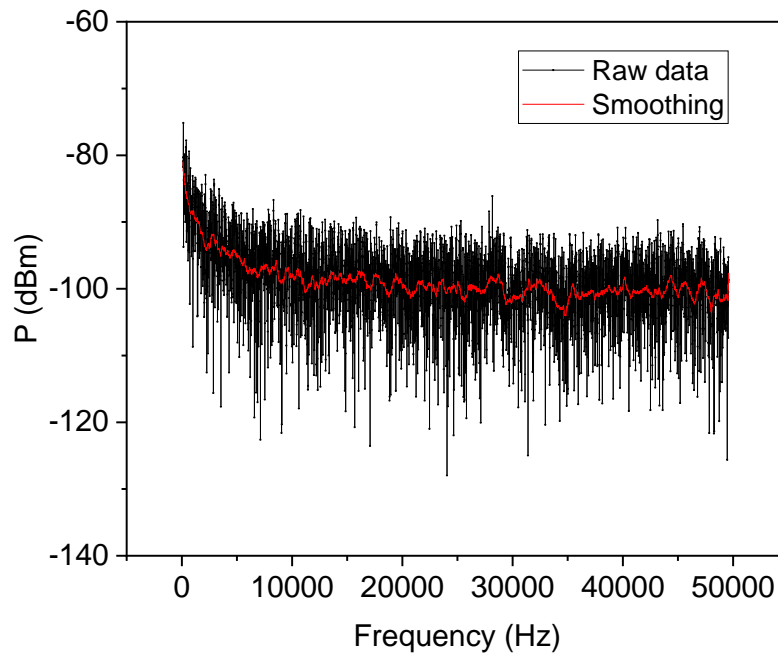


Figure C.1. Power spectrum curve corresponding to a piezotronic sensor with ALD-grown ZnO thin film deposited at 80 °C, with an applied DC bias voltage value of 6 V.

The black curve corresponds to the raw data while the red curve was obtained via a smoothing method on the software Origin to reduce noise from the obtained measurement. Subsequently, the numerical method described from equations (C.1) to (C.5) was applied on the smoothed data. The obtained noise spectral density values are represented in Fig. C.2.

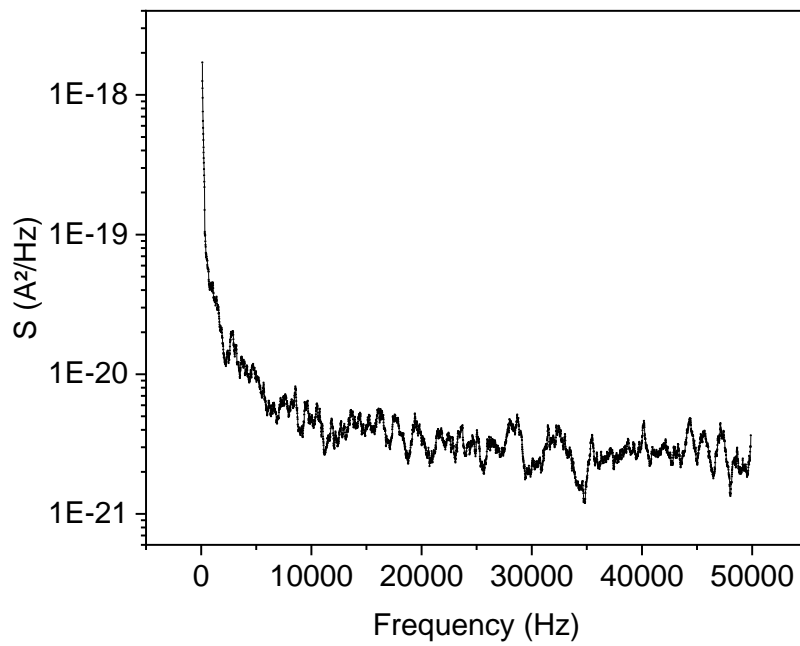


Figure C.2. Noise spectral density corresponding to a piezotronic sensor with ALD-grown ZnO thin film deposited at 80 °C, with an applied DC bias voltage value of 6 V.

This protocol was further applied for the different experimental conditions (i.e. ALD deposition temperature, DC bias voltage) presented in the section 4.3.3.

D. Measurement and imaging chain used for AFM imaging

This appendix details the instrumentation used within the measurement and imaging chain dedicated to AFM imaging.

A lock-in amplifier (LIA) (HF2LI, Zurich Instruments, Switzerland) was first used to generate a sinusoidal signal (with an amplitude of 200 mV and a frequency of 5 kHz) supplied to the piezotronic sensor. As the polyimide cantilever with the silica sphere were probing the sample's surface, the sensor's electrical signal was modulated by strain via the piezotronic effect. The sensor's signal response was connected to a variable gain current amplifier (DLPCA-200, FEMTO, Germany) converting the sensor's current into voltage (with an amplification of $10^7 \text{ V}\cdot\text{A}^{-1}$). The signal was thus returned to the LIA (using a bandwidth of 200 Hz), which compared the sinusoidal sensor's response to the excitation signal to measure its amplitude and its phase. The resulting signal amplitude was supplied to the LIA feedback loop, where it was locked to a set value (set-point) using a proportional-integral-derivative (PID) control algorithm. The sensor's amplitude response was decreasing during the sensor's scanning operation, indicating an increasing compressive strain state as the cantilever was further bent. More precisely, the set-point in deflection corresponding to an operating current of 13 nA was defined as a 4 % up to 8 % reduction compared to the steady-state sensor's amplitude corresponding to a steady-state current of 13.6 nA. This setpoint ensures a stabilized mechanical contact between the surface and the silica sphere of the cantilever. The feedback loop locked the amplitude to the set-point by retroacting on the Z-axis positioning of the probed surface via a piezo controller (PI controller). For this purpose, a Z-axis piezo positioner (P-622-ZCD, Physik Instrumente GmbH, Germany) was connected to a piezo controller (E-754_1CD, Physik

Instrumente GmbH, Germany), allowing a linear travel range of 250 μm by a closed loop configuration. The output signal from the feedback loop was thus sent to the PI controller, which further induced a proportional Z-axis movement so that the sensor's deflection amplitude remained equal to the set-point value.

Once the set-point defined, the cantilever's Z-axis approach on the surface was realized with the stepper motor from the Nanonics Multiview 4000. The approach was stopped manually once the set-point was reached at the half (i.e. 125 μm) of the Z-axis piezo positioner range. The resulting variations in the Z-axis position controlled by the feedback loop during the scanning operation were further sent to the Nanonics for subsequent imaging. Furthermore, the X and Y axis positions were controlled by the Nanonics via an integrated piezo controller (PI E-725.3CDA, Physik Instrumente GmbH, Germany), and its associated piezo positioner (P-517.3CD, Physik Instrumente GmbH, Germany). The generation of the image was then realized by the Nanonics Multiview 4000's software. The image's area consisted in a 100 x 100 μm^2 surface discretized in 128 x 128 pixels, with a corresponding scanning time of 20 ms.pixel⁻¹. The Z-axis position output value from the feedback loop corresponding to each pixel was thus used for imaging the surface over the defined scanned area. As the resulting raw image is in units of Volts for each pixel, a conversion formula was finally applied to convert the image in metric coordinates, corresponding to the digital conversion a \pm 10 V analog output into the 250 μm Z piezo range, as:

$$Z_m = Z_v \cdot 12.5 [\mu\text{m} \cdot \text{V}^{-1}] + 125 [\mu\text{m}]$$

Where Z_m corresponds to Z-axis position output value in metric coordinates and Z_v corresponds to Z-axis position output value in units of Volts.

Publications

R. Joly, S. Girod, N. Adjeroud, T. Nguyen, P. Grysan, S. Klein, K. Mengueli, C. Vergne, J. Polesel-Maris, *Polymeric cantilevered piezotronic strain microsensors processed by Atomic Layer Deposition*, *Sensors Actuators, A Phys.* (2020). doi:10.1016/j.sna.2020.112280.

R. Joly, S. Girod, N. Adjeroud, P. Grysan, J. Polesel-Maris, *Evidence of Negative Capacitance and Capacitance Modulation by Light and Mechanical Stimuli in Pt/ZnO/Pt Schottky Junctions*, *Sensors*. 21 (2021) 2253. doi:10.3390/s21062253.

T. Nguyen, N. Adjeroud, M. Guennou, J. Guillot, Y. Fleming, A.-M. Papon, D. Arl, K. Mengueli, **R. Joly**, N. Gambacorti, J. Polesel-Maris, *Controlling electrical and optical properties of zinc oxide thin films grown by thermal atomic layer deposition with oxygen gas*, *Results Mater.* (2020) 100088. doi:10.1016/j.rinma.2020.100088.

T. Nguyen, N. Valle, J. Guillot, J. Bour, N. Adjeroud, Y. Fleming, M. Guennou, J.-N. Audinot, B. El Adib, **R. Joly**, D. Arl, G. Frache, J. Polesel-Maris, *Elucidating the growth mechanism of ZnO films by atomic layer deposition with oxygen gas via isotopic tracking*, *J. Mater. Chem. C.* (2021). doi:10.1039/D0TC05439A.

R. Joly, S. Girod, P. Grysan, N. Adjeroud, C. Vergne, T. Nguyen, J. Polesel-Maris, *Investigation of back-to-back Pt/ZnO/Pt Schottky junctions to get highly sensitive strain sensors*, (2021), in preparation.

Patents

J. Polesel, S. Girod, **R. Joly**, P. Grysan, "Manufacturing method of a strain gauge sensor", filed Patent LU101963, 31/07/2020.

Oral presentations

Zinc oxide material elaboration by atomic layer deposition, role of molecular oxygen incorporation and Schottky consecutive behavior, **R. Joly**, N. Adjeroud, T. Nguyen, S. Girod, K. Menguelti, M. El Hachemi, J. Polesel-Maris, EuroCVD 22-Baltic ALD 16 Conference, June 2019, Luxembourg, Luxembourg.

Deposition and optimization of Schottky junctions by Atomic Layer Deposition for piezotronic strain sensors, **R. Joly**, S. Girod, N. Adjeroud, T. Nguyen, K. Menguelti, M. El Hachemi, P. Grysan, S. Klein, J. Polesel-Maris, 45th International Conference on Micro & Nano Engineering (MNE 2019), September 2019, Rhodes Island, Greece.

Optimized Schottky junctions by Atomic Layer Deposition for piezotronic MEMS strain microsensors, **R. Joly**, S. Girod, N. Adjeroud, M. El Hachemi, P. Grysan, T. Nguyen, K. Menguelti, S. Klein, J. Polesel-Maris, 20th International Conference on Atomic Layer Deposition (ALD 2020), June-July 2020, Ghent, Belgium, online conference.

Capacitance modulation by light and mechanical stimuli in ALD-deposited ZnO thin films integrated in piezotronic MEMS strain microsensors, **R. Joly**, S. Girod, N. Adjeroud, P. Grysan, J. Polesel-Maris, 21th International Conference on Atomic Layer Deposition (ALD 2021), June 2021, online conference.

Poster presentations

Structuration of piezotronic junctions for ultrasensitive strain sensors, **R. Joly**, S. Girod, N. Adjeroud, M. El Hachemi, J. Polesel-Maris, Kick-off meeting of the doctoral programme, February 2018, Belval, Luxembourg.

Structuration of ultrasensitive micro-strain gauges by Atomic Layer Deposition, **R. Joly**, S. Girod, N. Adjeroud, M. El Hachemi, K. Menguelti, P. Grysan, J. Polesel-Maris, Summer School: Micro and Nano sensors (DTU Nanotech), August 2018, Copenhagen, Denmark.

ECTS

Course title / Training	Place	Dates	ECTS
Poster presentation at the Kick-off meeting of the Doctoral Programme	University of Luxembourg	23.02.2018	0.5
Chemistry of Atomic Layer Deposition	University of Luxembourg	19.03 - 20.03.2018	0.5
Training Vacuum Physics and Technology	40-30 - Seyssinet	27.03 - 29.03.2018	1
Analyse des surfaces et des couches minces	Société Française du Vide - Paris, France	29.05 - 30.05.2018	0.5
Summer School: Micro and Nano sensors	Technical University of Denmark - Denmark	13.08 - 24.08.2018	2
Leadership Skills	University of Luxembourg	17.09 - 18.09.2018	1
Good Scientific Practice	University of Luxembourg	01.10 - 02.10.2018	1
Toolkit to get successfully manage your research outputs	University of Luxembourg	Winter Semester 2018 - 2019	1

Data visualization & statistical graphics with Stata	University of Luxembourg	26.03 - 02.04.2019	1
Oral presentation - International conference - EuroCVD 22-Baltic ALD 16 Conference	LUXEXPO - Exhibition & Congress Center, Luxembourg	24.06 - 28.06.2019	2
Summer School: Project Management: From Theory to Practice	European Summer School - Prague, Czech Republic	15.07 - 26.07.2019	2
Oral presentation - International conference - 45 th International Conference on Micro & Nano Engineering MNE2019	Rhodes Island, Rhodos Palace, Greece	23.09 - 26.09.2019	2
Oral presentation - 20 th International Conference on Atomic Layer Deposition	ALD 2020, Online conference	29.06 - 01.07.2020	2
Oral presentation - 21 st International Conference on Atomic Layer Deposition	ALD 2021, Online conference	27.06 – 30.06.2021	2

Total of: 18.5 ECTS

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LIST work contract: November 15th, 2017.

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