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A New Single-phase PLL based on the Input Voltage Magnitude Estimation

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Abstract

Many automatic control applications such as wide scale power grid management and local power conditioning rely on the fast and accurate detection of the voltage signal phase and amplitude. These information are almost all the time given by the Phase –locked Loop (PLL) systems and can be single-phase or three-phase and have many different structures. Many single-phase PLLs core structure are based on the regulation to zero of the voltage direct component in the rotating d-q frame obtained through the Park-transform. Their accuracy and dynamic rely on how quick and accurate the second voltage's component in the static α-β frame is estimated. This paper presents a new single-phase PLL structure, also based on the same core structure as described before, but implementing a novel voltage β-component generation. A brief review of some single-phase PLLs is made, then the proposed novel PLL structure is detailed and its performance is compared with that of the other PLL's taking into consideration the following signal disturbances: amplitude variations, phase step variation and frequency fluctuations as well as harmonic distortion.

Keywords: Single-phase PLL, Interconnected power systems, harmonic distortion, grid frequency variation.

1. Introduction

The accuracy and the dynamic of single-phase park-transform based PLLs rely on how quickly and fine the construction or estimation of the second voltage's component is in the

static α-β frame. Once this second component is created, the following calculations are exactly the same as that in the 3-phase synchronous reference frame PLL (dqPLL) depicted on Figure 1 (Rubens Marcos dos Santos Filho, Paulo F. Seixas, & Porfírio C. Cortizo): the α- and β-voltage components are transformed into the d-q rotating frame and the direct component is regulated through a PI controller to zero. Meanwhile, the quadrature component will converge to the signal amplitude and the controller output value will then correspond to the input signal angular velocity. Besides of being known to be the most robust and stable wave signal phase tracker, the dqPLL delivers not only the signal phase but also the signal amplitude. This last property can be quite interesting when comparing different PLL algorithms. Choosing one that has more deliveries than the phase of the signal is recommended if the monitoring or control requires other values such as the signal amplitude.

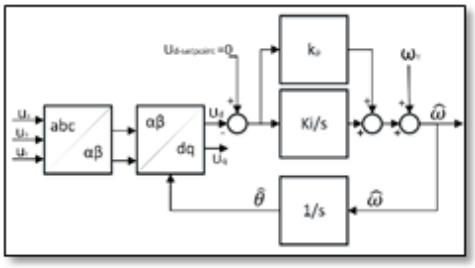

Figure 1: Block diagram of the 3-Phase synchronous Reference Frame PLL - dqPLL

2. Single-phase PLLs

2.1 Single-phase Delay PLL - dPLL

The Figure 2 shows the block diagram of the single phase dPLL. This one represents the least computational resources consuming PLL algorithm where a sample delay is used to build the Uβ component (Silva, S.M., Lopes, B.M., Filho, B.J.C., Campana, R.P., & Bosventura, W., 2004). The sample delay corresponds to one fourth of the input signal rated period.

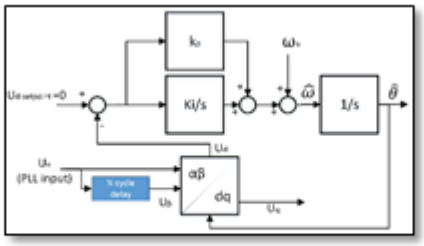

Figure 2: Block diagram of the single-phase delay PLL - dPLL

2.2 Single-phase Inverse Park PLL - ipPLL

In the case of the inverse Park PLL (ipPLL) shown on Figure 3 (Silva, S.M., Lopes, B.M., Filho, B.J.C., Campana, R.P., & Bosventura, W., 2004) (Atul Gupta, Anurag Porippireddi, Venu Uppuluri Srinivasa, Akash Sharma, & Mangesh Kadam, 2012), the voltage quadrature α-component is built as the feedback from the inverse Park transformation whose inputs are the synchronous voltages Ud and Uq that are filtered through first order filters (Rubens

Marcos dos Santos Filho, Paulo F. Seixas, & Porfírio C. Cortizo) (Sidelmo Magalhães Silva, Lícia Neto Arruda, & Braz J. Cardoso Filho, 2001).

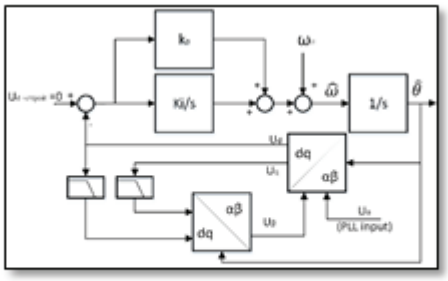

Figure 3: Block diagram of the Inverse Park PLL – ipPLL

2.3 Single-phase PLL Based on Generalized Integrator - giPLL

The Figure 4 depicts the voltage beta component generation using the second order generalized Integrator (Atul Gupta, Anurag Porippireddi, Venu Uppuluri Srinivasa, Akash Sharma, & Mangesh Kadam, 2012) (Mihai Ciobotaru, Remus Teodorescu, & Frede Blaabjerg, 2006) (Dr.-Ing. B. Burger & Dipl.-Ing. A. Engler, 2001) (Alfred Engler, 2001). Two signals are generated where the first might have the same amplitude and phase as the input signal and the second signal is equal to the first but with a phase shift of 90°. These are then used as input signals for the Park-transformation and the angular velocity controller block.

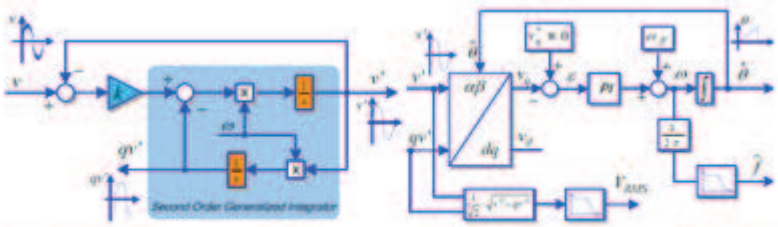

Figure 4: Block diagram of the generalized integrator based PLL giPLL

3. Single-phase PLL Based on the Estimated Signal Magnitude - mePLL

This proposed PLL, like the previously described ones, tries to quickly estimate the second voltage component in the static α-β frame. On the depicted diagram in Figure 5 , the β-component is calculated by determining the input signal magnitude U that is then multiply by the sinus of the estimated phase.

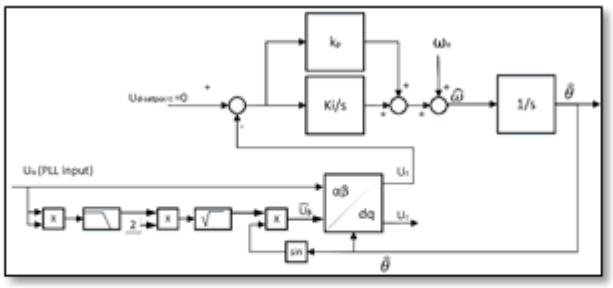

Figure 5: Block diagram of the magnitude estimated based PLL – mePLL

In a balanced and harmonic free state, the input signal magnitude is determined by squaring the input signal U_α

$$\begin{cases} U_\alpha = U \cdot cos(\omega t + \varphi) = U \cdot \cos\theta \\ U_\alpha^2 = \frac{1}{2}U^2 \cos(2\omega t + 2\varphi) + \frac{1}{2}U^2 \end{cases} \quad (1)$$

U as the voltage magnitude, ω the angular velocity, φ the phase angle offset and θ the final phase angle. A low pass filter LPF extracts the offset value $\frac{1}{2}U^2$ and the signal magnitude is deduced by computing the square root of the double of the LPF output value. The speed and the accuracy of the magnitude calculation depends only on the LPF's cut-off frequency and order.

Following the calculation of the voltage direct component U_d in the rotating frame through the Park transform (Rubens Marcos dos Santos Filho, Paulo F. Seixas, & Porfírio C. Cortizo),

$$\begin{cases} U_d = U_\alpha \sin\hat{\theta} - U_\beta \cos\hat{\theta} \\ with\ U_\beta = U \sin\theta \end{cases} \quad (2)$$

Where U_α and U_β components are calculated using the Clark transform. For this proposed PLL, U_β is replaced by the calculated amplitude times the sinus of the estimated signal phase.

$$U_d = U[\cos\theta \sin\hat{\theta} - \sin\hat{\theta}\cos\hat{\theta}] \quad (3)$$

$With\ \Delta\theta = \theta - \hat{\theta}$,

$$U_d = U\left[-\frac{1}{2}\sin(\Delta\theta) + \cos\left(2\theta - \frac{3}{2}\Delta\theta\right) \cdot \sin\left(\frac{\Delta\theta}{2}\right)\right] \quad (4)$$

For small phase difference $\Delta\theta$, U_d can be written as

$$U_d = U\left[-\frac{1}{2}\Delta\theta + \cos(2\theta) \cdot \frac{\Delta\theta}{2}\right] = -\frac{1}{2}U\Delta\theta + \frac{1}{2}U\Delta\theta\cos(2\theta) \quad (5)$$

The voltage direct component U_d is an offset oscillatory value whose frequency is very

close to the double of the input frequency and whose amplitude is proportional to the half of the input signal amplitude time the difference between the real and estimated phases. This remains quite small especially since the difference between the real and the estimated phases is small. Regulating this direct component to zero is totally possible since the amplitude of the oscillation will simultaneously decrease with the convergence of the regulated offset value ($\frac{1}{2}U\Delta\theta$) to zero.

4. Simulation Results and Performance Comparison

4.1 PLLs Configuration

A 3-phase signal is generated with a frequency of 50Hz, an amplitude of 100 and no phase shift. 0.3 second later, a magnitude step variation of +20% occurs, followed by a phase step variation of +15° at the time 0.4 second. At last comes a relative frequency deviation of +2% at the time 0.7 second. All the above described PLLs have been implemented at a sampling rate of 20 kHz and the delivered values are compared. As reference value for the angular velocity and signal phase will be taken the signal generator frequency times 2π and its integrated value respectively. The dqPLL is simplified for balanced system and is calculating based on 2 voltage signals, while the others need only one input signal. They are all set for a 50Hz signal (feedforward frequency) and all the controllers have the same gains $\mathrm{k_p} = 1\,\mathrm{rad}V^{-1}\mathrm{s}^{-1}$ and $\mathrm{k_i} = 25\,\mathrm{rad}V^{-1}\mathrm{s}^{-2}$; except the mePLL, where they are doubled: $\mathrm{k_p} = 2\,\mathrm{rad}V^{-1}\mathrm{s}^{-1}$ and $\mathrm{k_i} = 50\,\mathrm{rad}V^{-1}\mathrm{s}^{-2}$. The sample delay by the dPLL is 100 (1/4*20kHz/50Hz). The LPFs of the ipPPL have cut-off frequencies set at 50Hz. The second order generalized integrator of the giPLL have $\mathrm{k_p} = 4$ and $\mathrm{k_i} = 2 * \mathrm{pi} * 50\mathrm{s}^{-2}$. And finally the proposed mePLL has its 6th-order IIR LPF with a cut-off frequency set at 30Hz.

4.2 Amplitude and Phase Step Variation

The Figure 6 and Figure 7 show, to the exception of the giPLL, good responses to the input signal variations. The giPLL already has a static error even at the nominal frequency. The mePLL presents a transient oscillatory period when the signal amplitude changes but quickly decays to zero. This is due to the response time of the filter used to determine the signal magnitude. The most robust PLL (but not single-phase), the dqPLL, don't show any disturbance caused by the amplitude variation. After a phase step variation, they all have the same response time, very close to that of the dqPLL, to correct the error excluding the giPLL that will keep its steady state error.

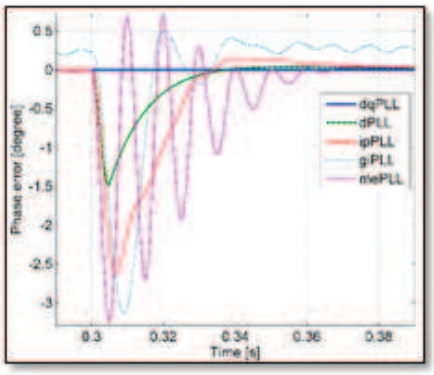

Figure 6: Phase error after a magnitude step variation of +20%

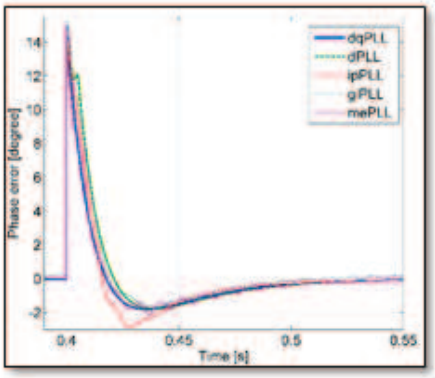

Figure 7: phase error after a signal phase step variation of +15°

4.3 Frequency Variation

In the case of a frequency variation (Figure 8), not only the giPLL but also the dPLL shows some weakness. Both have a steady phase error and that of the giPLL is still greater than its steady error before the frequency change. The proposed mePLL has a very good behavior toward this variation despite de transitory oscillations. The oscillations are very low in amplitude and, as in the case of amplitude and phase variation, decay quickly as the error decreases.

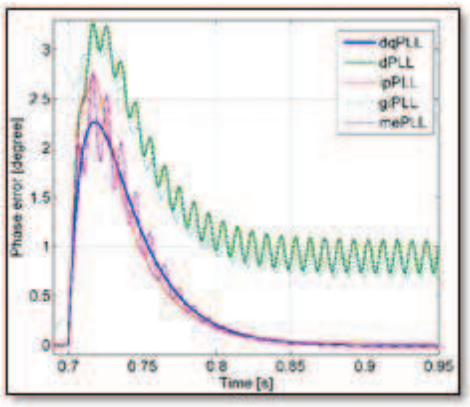

Figure 8: Comparison of phase error after a relative frequency deviation of +2%

5. Improved mePLL

The equation (5) shows that the oscillatory part in the calculated U_d value has a frequency close to the double of the signal input frequency. A band-stop filter is then used to eliminate the oscillations without hindering the system dynamic Figure 9).The Figure 10, Figure 11 and Figure 12 show the expected improvement brought by the band-stop filters. The transitory oscillations have been eliminated and the overall calculation system remained almost unchanged in dynamic and robustness.

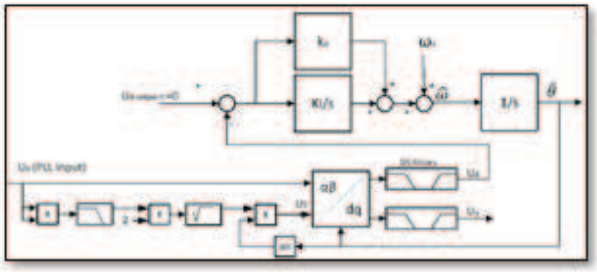

Figure 9: Block diagram of the filtered mePLL – mePLLc

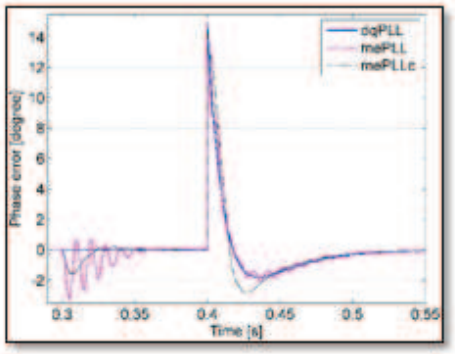

Figure 10: Improved phase error after a magnitude step variation of +20%

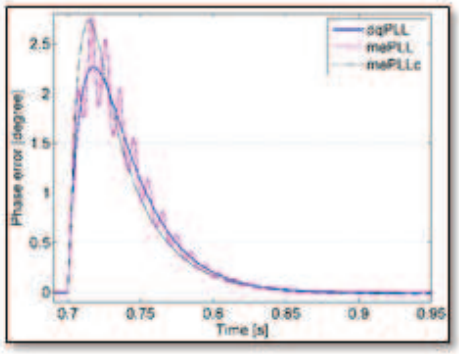

Figure 11: Improved phase error after a signal phase jump of +15°

Figure 13 shows the impact of harmonics on the phase detection accuracy. In presence of the 5th harmonic (250Hz) with a relative amplitude of 40% to the fundamental, the PLL remains stable with the same dynamic but the calculated output phase position oscillates around the set point with a maximum deviation of about 2.5° and 1.5° for the mePLL and dqPLL respectively.

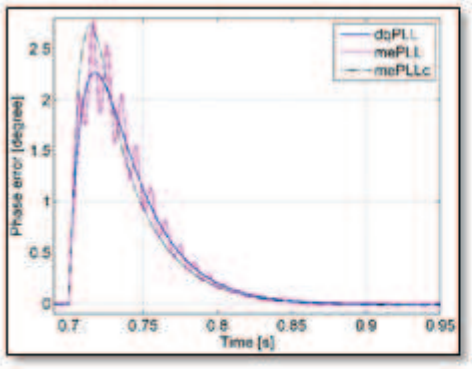

Figure 12: Improved phase error after a relative frequency change of +2%

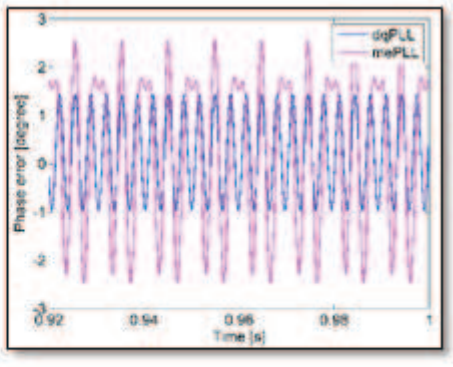

Figure 13: phase error by 40% 5th harmonic injection

6. Conclusion

This work presents a new single-phase PLL structure based on the estimation of the input signal amplitude through filtering the squared of the input signal value. Comparisons made with other single-phase PLLs show its stability and reliability.