Phase-error correction by single-phase Phase-Locked Loops based on transfer delay

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Abstract

Comparative studies of different single-phase phase-locked loops (PLL) algorithms have been made. They show that the PLL based on sample delay (dPLL), presents the lowest computational load and is as robust as the three-phase synchronous reference frame PLL dqPLL by input signal amplitude and phase variations. Its weakness appears when the input signal frequency differs from its rated frequency: it depicts a steady error on the calculated signal phase-angle. After a brief review of the dqPLL which constitutes de base structure of the dPLL, the following work will present three methods that improves the phase detection accuracy of dPLL. It is shown that the modifications brought in the original structure do not influence the robustness and stability of the algorithm but reduce the phase angle offset error by input signal frequency variation. This is corroborated by tests including not only the fundamental input voltage disturbance like amplitude, phase and frequency variation but also harmonic voltage distortion.

Key words: single-phase PLL, transfer delay PLL, phase-angle correction, frequency variation, harmonic distortion.

1 Introduction

Over the last decades the electricity market trade has led to more and more interconnected power grid. In addition to that, the worldwide exploding concern toward the environment's health by adopting many laws to reduce the pollution related to electricity generation and usage boosted the small scale decentralized power generation that is in most case connected to the main grid. The synchronisation that makes all these power interconnections possible relies on a critical component: the phase-locked-loop (PLL) [1] [2]. The PLL computes the grid voltage frequency, phase angle and most of the time also the amplitude. These information represent the basic data for many operations such as power grid conditioning, reactive and active power control [3] [4], security and protection processes [5] [6].

There are two main groups of PLL's implementations algorithms: the single-phase PLL and three-phase PLLs for single-phase and three-phase voltage system respectively. Comparative studies of different single-phase PLL algorithms have been presented in [7] [8] [9] and it shows that PLL based on sample delay, the delay PLL dPLL, presents the lowest computational load and is as robust as the three-phase synchronous reference frame PLL dqPLL by input signal amplitude and phase variations. Its weakness

appears when the input signal frequency differs from its rated frequency: it depicts a steady error on the calculated signal phase position. After a brief overview of the dqPLL of which a big part of the algorithm is also used for the dPLL, this document will presents three methods to cancel the dPLL steady phase-error by input signal frequency change.

2 Synchronous Reference Frame PLL – dqPLL

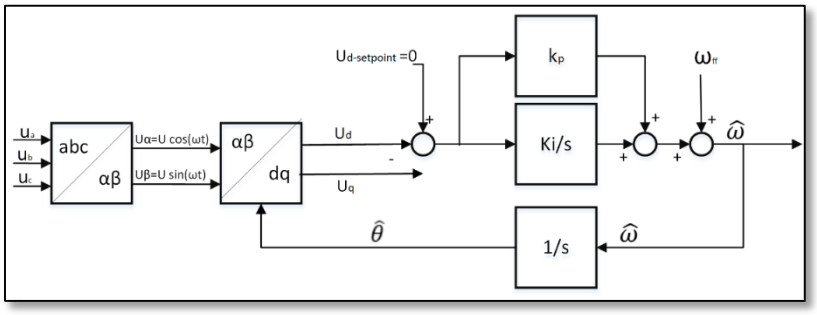

Figure 1: Block diagram of the synchronous Reference Frame PLL – dqPLL

The working principle of the dqPLL, depicted on Figure 1 [7] is based on regulating the voltage direct component U_d in the rotating dq-frame to zero. The α- and β-voltage components obtained from the Clark Transform, are transformed into the d-q rotating frame and the direct component is regulated through a PI controller to zero while the quadrature component will converge to the signal amplitude and the controller output value will then correspond to the input signal angular velocity. U_d is calculated using the estimated phase angle that is the integrated value of the estimated angular velocity. In a balanced and harmonic free system, U_d and U_q are expressed as:

$$\begin{bmatrix} U_d \\ U_q \end{bmatrix} = \begin{bmatrix} \sin\hat{\theta} & -\cos\hat{\theta} \\ \cos\hat{\theta} & \sin\hat{\theta} \end{bmatrix} \cdot \begin{bmatrix} U_\alpha \\ U_\beta \end{bmatrix}$$
$$Where \begin{cases} U_\alpha = U\cos\theta \\ U_\beta = U\sin\theta \end{cases} with\ U\ equals\ the\ input\ signal\ amplitude \quad (1)$$

Then

$$\begin{cases} U_d = U\cos\theta\sin\hat{\theta} - U\sin\theta\cos\hat{\theta} \\ U_q = U\cos\theta\cos\hat{\theta} + U\sin\theta\sin\hat{\theta} \end{cases} \rightarrow \begin{cases} U_d = -U\,sin(\theta - \hat{\theta}) \\ U_q = U\cos(\theta - \hat{\theta}) \end{cases} \quad (2)$$

These equations show that when the estimated phase angle $\hat{\theta}$ is nearing the real phase angle θ, U_d will approximate zero while U_q will tend to the input voltage amplitude. For small value of $\Delta\theta = \theta - \hat{\theta}$, when the estimated phase angle is close to the real one, the direct component can be simplified to:

$$U_d = -U \cdot \Delta\theta \quad (3)$$

From the block diagram, we can write:

$$-U_d = U(\omega t - \hat{\omega} t)$$
$$-U_d = U\left(\frac{\omega}{s} - \frac{\hat{\omega}}{s}\right) = U\left(\frac{\omega}{s} - \frac{1}{s}\left(\omega_{ff} + \left(k_p + \frac{k_i}{s}\right)\cdot -U_d\right)\right) \quad (4)$$

$$With\ \Delta\omega = (\omega_{ff} - \omega) \rightarrow U_d = \frac{\Delta\omega \cdot s}{\frac{1}{U}s^2 + sk_p + k_i} \quad (5)$$

The transfer function describing the evolution of U_d in function of the frequency/angular velocity variation of the input signal is:

$$TF_{U_d \Delta\omega} = \frac{U_d}{\Delta\omega} = \frac{s}{\frac{1}{U}s^2 + sk_p + k_i} \tag{6}$$

Therefore, the transfer function linking the estimated angular velocity and a frequency deviation from the feed-forward frequency is:

$$TF_{\hat{\omega}\Delta\omega} = \frac{-sk_p - k_i}{\frac{1}{U}s^2 + sk_p + k_i} \tag{7}$$

Since U is absolutely positive, the system will be stable if the regulator coefficients k_p and k_i are also positive. The dynamic and robustness are determined by the value of these coefficients. The boundary condition to no overshoot of the calculated direct component is given by

$$k_p^2 - \frac{4k_i}{U} \geq 0 \rightarrow \frac{k_p^2}{k_i} \geq \frac{4}{U} \tag{8}$$

The ratio ${k_p}^2/k_i$ is then inversely proportional to the signal amplitude. This means, to maintain de same robustness of the system, the controller coefficients ratio k_p to k_i has to increase by decreasing amplitude and inversely. This gives the idea of implementing an adaptive controller especially in the case of a harmonic compensation system where the harmonic's amplitude is decreasing to zero.

3 Single-phase delay PLL – dPLL

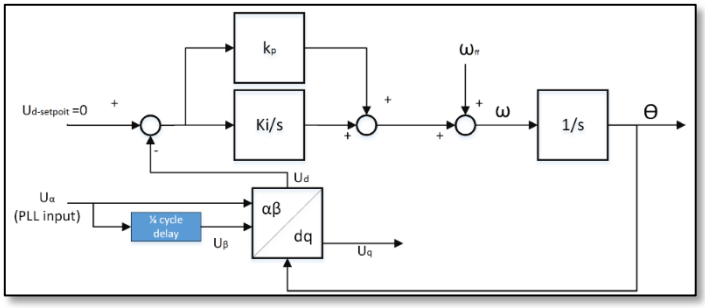

Figure 2: Block diagram of the single-phase delay PLL - dPLL

Figure 2 [7] shows the block diagram of the single phase dPLL. This one represents the least computational resources consuming PLL algorithm where a sample delay is used to build the U_β component [7]. The sample delay corresponds to one fourth of the input signal rated period. Despite its good detection precision behaviour toward a signal phase angle and amplitude step variation, it has a constant oscillating error range when it comes to a signal frequency change [7]. This is caused by the fixed length delay used to build the rotating quadrature component used by the dq-transformation. Using the ¼ cycle delay time on $U_\alpha = U\cos\omega t$ to build the U_β component,

$$U_\beta = U_\alpha\left(t - {}^1\!/_4\, T_0\right) = U\cos\left(\omega\left(t - {}^1\!/_4\; T_0\right)\right) \tag{9}$$

Where: ω is the actual angular velocity and T_0 the rated time period

U_β can also be written using the rated angular velocity ω_0 as

$$U_\beta = U\cos\left(\omega t - \frac{\pi}{2}\frac{\omega}{\omega_0}\right) \tag{10}$$

With $\omega = \omega_0(1 + \varepsilon_\omega)$ where ε_ω represents the relative angular velocity variation.

$$\varepsilon_\omega = \frac{\omega - \omega_0}{\omega_0} \tag{11}$$

$$U_\beta = U\cos\left(\omega t - \frac{\pi}{2}(1+\varepsilon_\omega)\right) = U\sin(\omega t - \frac{\pi}{2}\,\varepsilon_\omega) \tag{12}$$

Using the dq-transformation matrix (equation (1)), the direct voltage component in the dq-frame can be written as follow

$$U_d = U\left[\cos(\theta)\sin(\hat{\theta}) - \cos(\hat{\theta})\,\sin(\theta - \frac{\pi}{2}\,\varepsilon_\omega)\right] \tag{13}$$

$$With\ \Delta\theta = \theta - \hat{\theta}\ and\ \alpha = \frac{\pi}{4}\varepsilon_\omega$$
$$U_d = U\left[\frac{1}{2}\sin(-\Delta\theta) - \frac{1}{2}\sin(-2\alpha + \Delta\theta) + \frac{1}{2}(2\cos(2\theta - \Delta\theta - \alpha)\sin(\alpha))\right] \tag{14}$$

Since $\Delta\theta$ and α are very small values,

$$U_d = U(-\Delta\theta + \alpha) + U\alpha\cos(2\theta - \Delta\theta - \alpha) \tag{15}$$

This means, U_d has an oscillatory part U_{dd} equals to $U\alpha\cos(2\theta - \Delta\theta - \alpha)$ whose frequency is very close to the double of the input signal frequency and its amplitude $U\cdot\alpha$ is proportional to the input signal amplitude U and the relative input signal frequency variation to the rated frequency. This oscillatory part is considered as measurement disturbance to the stationary part U_{d0}.

$$\begin{cases} U_{dd} = U\cdot\alpha\cos(2\theta - \Delta\theta - \alpha) \\ U_{d0} = -U\cdot\Delta\theta + U\cdot\alpha \end{cases} \tag{16}$$

$$U_{d0} = -U\left(\frac{\omega}{s} - \frac{1}{s}\left(\omega_{ff} + \left(k_p + \frac{k_i}{s}\right)\cdot -U_d\right)\right) + U\cdot\alpha$$

$$U_{d0} = \frac{(\omega_{ff} - \omega)s + \alpha s^2}{\frac{1}{U}s^2 + (sk_p + k_i)}$$

$$with\ \Delta\omega = \omega_{ff} - \omega\ and\ \alpha = \frac{\pi}{4}\frac{\omega - \omega_{ff}}{\omega_{ff}} = -\frac{\pi}{4}\frac{\Delta\omega}{\omega_{ff}} = A\cdot\Delta\omega$$

$$\frac{U_{d0}}{\Delta\omega} = \frac{As^2 + s}{\frac{1}{U}s^2 + k_p s + k_i} \tag{17}$$

This characteristic equation of the transfer function is the same as the one for the dq-PLL, this means the dPLL has exactly the same dynamic and robustness as the dqPLL: the U_β calculation using the samples delay cannot lead to the PLL system instability but to inaccuracy. When the input signal frequency is equal to the nominal frequency of the PLL, $\alpha = 0$ this induces $U_{dd} = 0$ and $U_{d0} = -U\Delta\theta$. The dPLL by no frequency deviation has exactly the same results as the dqPLL.

4 Phase error cancellation methods

The non-oscillatory expression of the voltage direct component U_{d0} given in equation (16) shows that applying the standard $U_d$regulation to zero will automatically lead to a steady phase-shift that equals to α.

$$-U\Delta\theta + U\alpha = 0 \rightarrow\ \Delta\theta = \alpha \tag{18}$$

To avoid this permanent error on the signal phase position, one can choose to

- Change the PI controller set-point to $U\alpha$
- Correct the final output phase position by α
- Prevent the appearance of the phase-shift

4.1 Delay PLL with PI modified regulator's set-point– dPLL-Csp

The block diagram depicted on Figure 3 shows the structure of a delay PLL where the regulator set-point is not zero. The main idea of this method is to regulate the U_d value to another set-point U_{d-sp}

inducing a zero-error estimated angle. Based on equation (18), we can observe that changing the set-point from 0 to $U\alpha$ automatically leads to regulating the phase error to zero. Normally, the input signal amplitude U and the relative frequency deviation from the rated frequency are unknown (used to calculate α). However, the PLL itself, despite the oscillatory output values, gives good indicators of these unknown values: the quadrature component U_q is very close to the signal amplitude so is the estimated angular velocity to the real one therefore the estimated relative angular velocity change. So the regulator set-point is given by

$$U_{d-sp} = U_q \cdot \hat{\alpha} \; where \; \hat{\alpha} = \frac{\pi}{4}\widehat{\varepsilon_\omega} = \frac{\pi}{4}\left(\frac{\hat{\omega} - \omega_{ff}}{\omega_{ff}}\right) \tag{19}$$

This methods concentrates only on the offset value α, this means there will be a remaining oscillatory part appearing in the final output angle position since there is no correction for it.

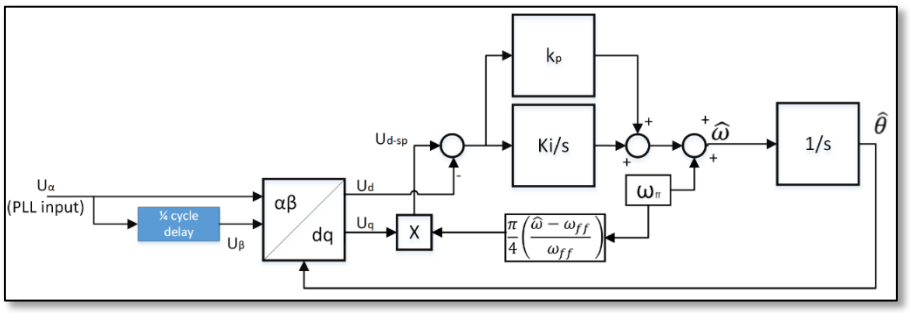

Figure 3: Block diagram of the delay PLL with modified controller set-point

4.2 Delay PLL with corrected output angle – dPLL-Ca

Very similar to the dPLL-Csp, this structure (Figure 4) focuses on correcting the final output angle without changing the Ud regulator set-point. In this case the correction has absolutely no influence on the system computations since the correction is only for the final output value with no feedback loop. Our goal being to make sure the PLL is in phase with the input signal, this means no difference between the actual phase and the adjusted estimated phase $\hat{\theta}_c$ by the PLL, this means $\theta = \hat{\theta}_c$.

We know from equation (18) $\theta - \hat{\theta} = \hat{\alpha}$

$$\rightarrow \hat{\theta}_c = \hat{\theta} + \hat{\alpha} \; with \; \hat{\alpha} = \frac{\pi}{4}\frac{\left(\hat{\omega} - \omega_{ff}\right)}{\omega_{ff}} \tag{20}$$

Just like the previous method, this will correct only the offset value α ignoring the oscillations.

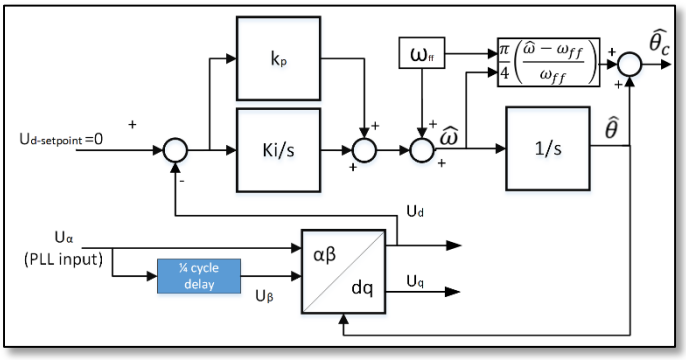

Figure 4: Block diagram of the delay PLL with the correction made on the output phase-angle value

4.3 Delay PLL with corrected voltage β-component – dPLL-CUb

Any input signal frequency variation from the rated PLL frequency causes oscillating errors on the delivered values. This is due to the fixed length delay set for the rated frequency which causes a bad estimation of the voltage U_β component. The two previous methods focus on correcting the

consequences of the U_β bad estimation on the contrary of the following (Figure 5) method that concentrates on avoiding the error in the estimation U_β.

Equation (12)**Error! Reference source not found.** gives the expression of U_β determined directly hrough the transfer delay $U_{\beta 0}$

$$\begin{aligned} U_{\beta 0} &= U\sin(\omega t - \frac{\pi}{2}\,\varepsilon_\omega) \\ &= U\sin(\omega t)\cos\left(\frac{\pi}{2}\,\varepsilon_\omega\right) - U\cos(\omega t)\sin\left(\frac{\pi}{2}\,\varepsilon_\omega\right) \\ U_{\beta 0} &= U\sin(\omega t)\cos\left(\frac{\pi}{2}\,\varepsilon_\omega\right) - U_\alpha\sin\left(\frac{\pi}{2}\,\varepsilon_\omega\right) \end{aligned} \tag{21}$$

In order to have the corrected error-free value $U_{\beta c}$ of U_β which should be $U\sin(\omega t)$, $U_{\beta 0}$should be corrected.

$$U_{\beta c} = \frac{U_{\beta 0} + U_\alpha \sin\left(\frac{\pi}{2}\,\varepsilon_\omega\right)}{\cos\left(\frac{\pi}{2}\,\varepsilon_\omega\right)} \tag{22}$$

Exactly as in the two previous cases, the estimated relative frequency variation will be used since the exact value is unknown.

$$U_{\beta c} = \frac{U_{\beta 0} + U_\alpha \sin\left(\frac{\pi}{2}\,\widehat{\varepsilon_\omega}\right)}{\cos\left(\frac{\pi}{2}\,\widehat{\varepsilon_\omega}\right)} \tag{23}$$

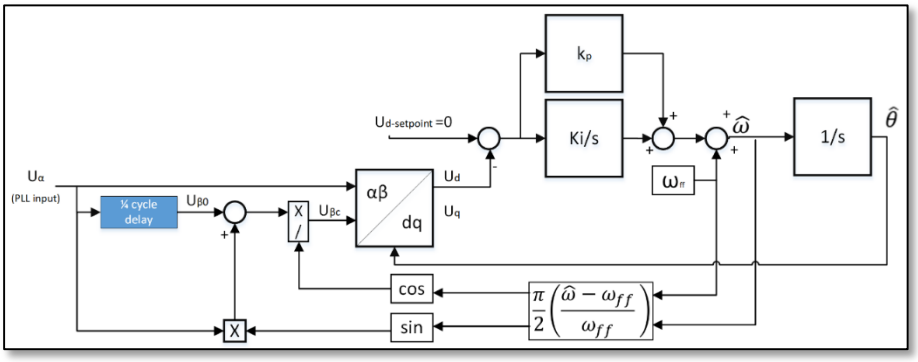

Figure 5: Block diagram of the delay PLL with the corrected β-component

5 Performance evaluation

A 3-phase signal is generated with a frequency of 50Hz, an amplitude of 100 and no phase shift. 0.3 second later, a magnitude step variation of +20% occurs, followed by a phase step variation of +15° at the time 0.4 second. At last comes a relative frequency deviation of +2% at the time 0.7 second. As reference value for the angular velocity and signal phase will be taken the signal generator frequency times 2π and its integrated value respectively. They are all set for a 50Hz signal (feedforward frequency), all the controllers have the same gains $\mathrm{k_p} = 1\ \mathrm{rad}V^{-1}\mathrm{s}^{-1}$ and $\mathrm{k_i} = 25\ \mathrm{rad}V^{-1}\mathrm{s}^{-2}$ and the sample delay length is $100\left(\frac{1}{4}\cdot\left(\frac{20\ kHz}{50\ Hz}\right)\right)$.

5.1 Amplitude and phase step variation

Figure 6 shows the evolution of the phase-error caused by a swell of 20%. All the PLLs (single-phase) except the dqPLL (3-phases) exhibits phase error between 1.5 and 2.5 degrees. This error will rapidly be reduced under 20ms to less than 0.2 degree. On the other hand, a 15° phase-shift of the input signal has nearly the same impact on all the PLLs that need about 100ms to get the phase-error under 0.5 degree (Figure 7). These observations show that the different changes made in the dPLL structures do not affect the dynamic response to the input signal amplitude and phase variation.

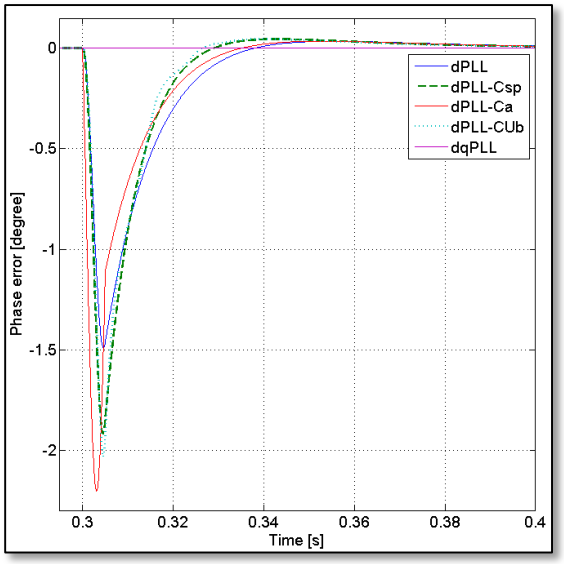

Figure 6: PLLs phase-angle response to a voltage swell of +20%

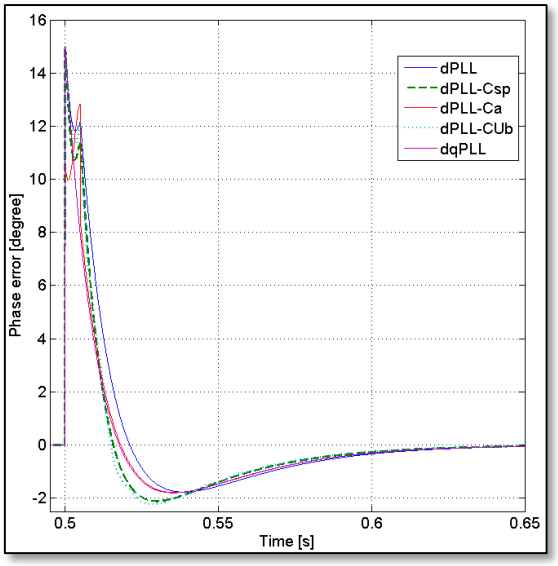

Figure 7: PLLs phase-angle response to a phase-jump of +15°

5.2 Frequency variation

The main focused weakness of the standard dPLL is depicted on Figure 8: any frequency deviation from its rated frequency leads to a steady oscillating phase-error. The realised modifications worked as expected. The improvement brought by the dPLL-Csp as well as the dPLL-Ca is the cancellation of the steady error despite the increase of the oscillations amplitude. However the oscillations amplitude remain very small (about 0.25 and 0.35 degree for dPLL-Csp and dPLL-Ca respectively). The best correction is performed by the dPLL-Cub where not only the steady offset error but also the oscillations disappear. It can also be observed that all the PLLs including the reference dqPLL have the same response time to reach their final value.

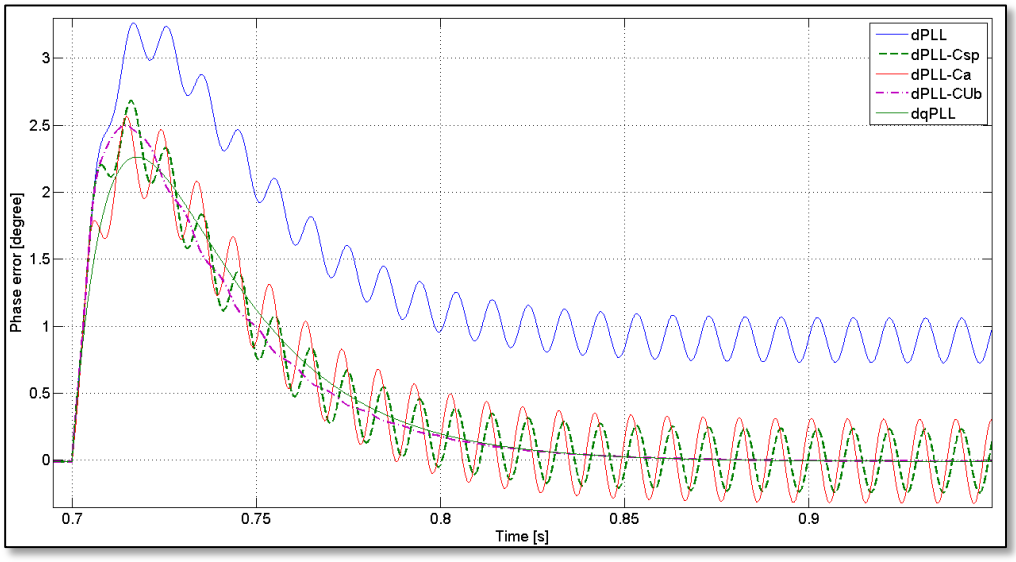

Figure 8: Phase-angle response to a frequency increase of 2%

The following figure Figure 9 shows the evolution of the maximum amplitude the oscillating phase errors after the 5th harmonic is injected, with different amplitude, into the input signal. First this reveals that no PLL is not influenced by harmonics with the dPLL-Ca having the highest sensitivity. The dPLL-CUb is more accurate than the others single-phase PLLs by no harmonics but becomes very fast less accurate than the dPLL-Csp (at about 2.5 % of the 5th harmonic injection). Filtering the control value U_d for dPLL-Csp and dPLL-Ca with band-stop filters (since the oscillations frequency range is known) brings

a considerable improvement. As shown on Figure 10, the phase-error is no longer oscillating and is zero for a harmonic-free signal. This makes them perfect structures for pre-treated (filtered) input signals. One can also observe that their sensitivity is reduced by around 34% and 54% respectively and most remarkably the fact that the filtered dPLL-Csp depicts a better accuracy than the dqPLL when dealing with distorted input signals. This is caused, in this case, by the large bandwidth of the band-stop stop filter which reduces also the oscillations in the direct voltage calculation caused by the 5th harmonic.

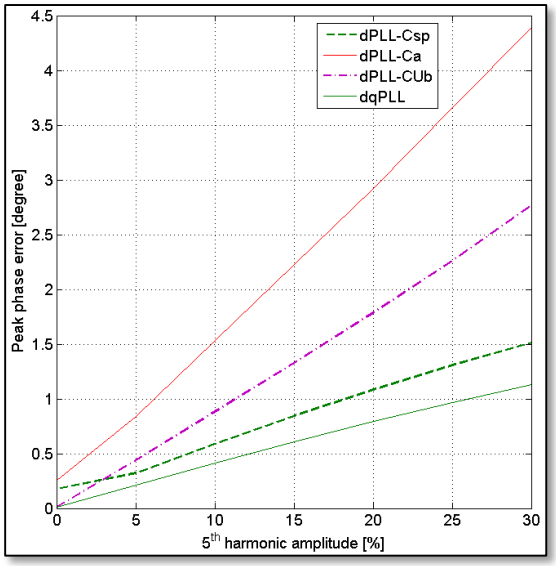

Figure 9: PLLs Peak phase error in function of 5th harmonic amplitude

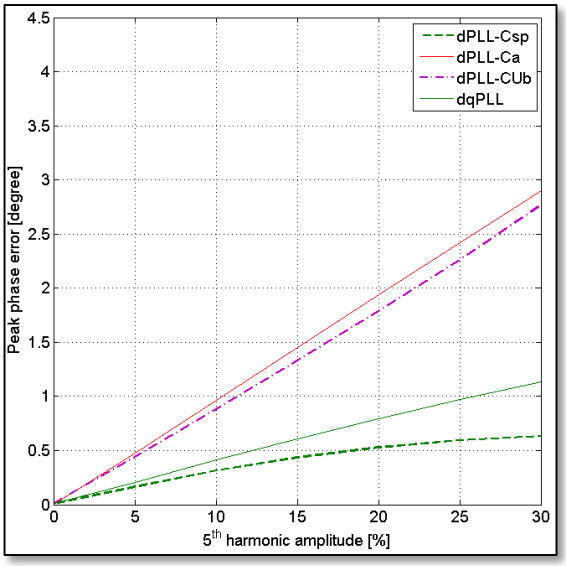

Figure 10: filtered PLLs Peak phase error in function of 5th harmonic amplitude

6 Conclusion

The identification of the amplitude, frequency and offset value of the steady oscillating error that appears by the dPLL when the input signal frequency deviates from its rated frequency, has been detailed. The error amplitude is proportional to the input signal amplitude and the relative frequency deviation from the rated frequency. Its frequency is very close to the double of the input signal frequency and the final phase steady offset value is proportional to the relative frequency variation to the rated one.

Three improvement approaches to correct that steady error have also been proposed and evaluated based on their true phase angle error. The error-mitigation structures dPLL-Ca and the dPLL-Csp succeed in cancelling the offset error but not the oscillations while the error-preventing structure dPLL-CUb eliminates also the oscillations. The proposed structures also proved their good performances in presence of harmonic disturbances in the input signal. Even though the magnitude of oscillations grows proportionally with the level of harmonics content, the PLLs remain stable. For dPLL-Ca and dPLL-Csp, filtering the output voltage direct component with band-stop filters considerably improves their detection efficiency by cancelling the inherent phase-error oscillations.

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