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ELECTRICAL CHARACTERIZATION OF KESTERITE THIN FILM ABSORBERS AND SOLAR CELLS

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CHAPTER

ONE

INTRODUCTION

Thin film solar cells have great perspective in terms of a competitive sustainable energy source [1]. In the lab CdTe and $Cu(In,Ga)Se_2$ (CIGSe) have already achieved record device efficiencies of 21.5 % [2] and 21.7 % [3], respectively. However, for installations in the TW scale a concern of these technologies is the scarcity of In and Te [1], which requires looking for new materials.

One promising candidate is the material system Cu, Zn, Sn, S(e). It crystallizes in the kesterite structure [4], which can be derived from the chalcopyrite structure as shown in Fig. (1.1) [5]. Starting from $Cu(In,Ga)Se_2$, the group three element In/Ga is replaced by the group two and group four element Zn and Sn, respectively such that it forms $Cu_2ZnSnSe_4$ (CZTSe). Alloying with S results in $Cu_2ZnSn(S,Se)_4$ (CZTSSe) and allows for engineering the bandgap between 1.0 eV and 1.5 eV for $Cu_2ZnSnSe_4$ and Cu_2ZnSnS_4, respectively [6]. Experimentally and theoretically, a direct bandgap was found for these semiconductors [7] and therefore the interesting range of bandgaps for solar cell applications [8] can be covered.

Due to the similarity with CIGSe, the same solar cell structure can be used, which is a soda lime glass (SLG)/Mo substrate and a CdS/i:ZnO/Al:ZnO window layer [9]. The highest efficiency so far was demonstrated for a mixed S and Se device, i.e. $Cu_2ZnSn(S,Se)_4$ (CZTSSe), with a power conversion efficiency of 12.6 % [10]. The highest efficiency for the pure Se and S devices reached values of 11.6 % [11] and 9.2 % [12], respectively. Note that the 9.2 CZTS device was fabricated with an CdS/In_2S_3 buffer layer. A recent review paper by Fella *et al.* [13] summarizes the different growth techniques employed for reaching high efficient kesterite devices. In contrast to CIGSe, the highest efficiencies for CZTSSe are reached by non-vacuum deposition techniques with a sequential process [10]. The best high temperature co-evaporated device is made by NREL with 9.4 % [14].

The major problem in achieving higher efficiencies is a high open circuit voltage deficit for all kesterite based devices [15]. Repins *et al.* [14] observed for high efficient (9.4 %) co-evaporated CZTSe devices lifetimes around 2 - 3 ns, which is small compared to lifetimes above 100 ns observed for high efficient CIGSe devices [16]. However, the authors also pointed out that these small lifetimes responsible for the low observed open circuit voltages cannot alone be due to deep Shockley-Read-Hall (SRH) recombination centres. Gokmen *et al.* [17] pointed out that also strong tailing occurs in CZTSe devices, which could explain the low V_{oc} values for the low bandgap CZTSSe (high [Se]/([Se] + [S]) ratio) devices. However, for higher S contents the tailing alone is not sufficient to describe the V_{oc} deficit and therefore also other effects need to be taken into account. In Ref. [17] it was also proposed that the tailing could be due to

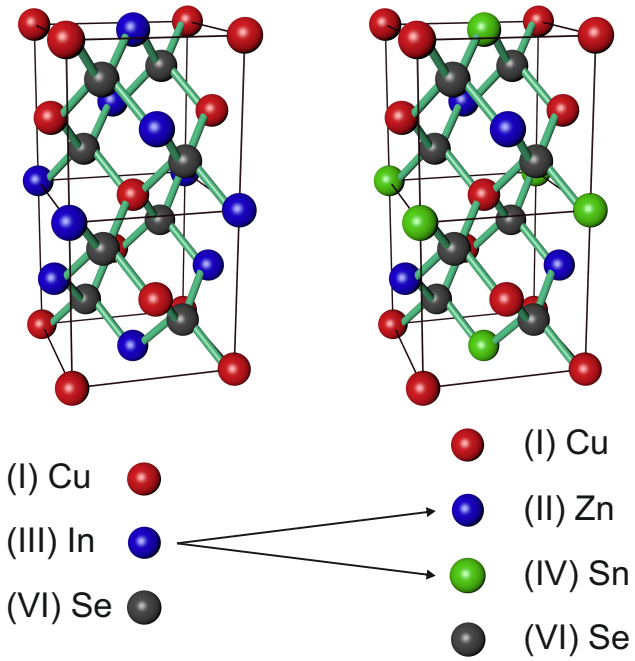


Figure 1.1.: ***Comparison of chalcopyrite and kesterite crystal structure*** *- Crystal structure of kesterite is obtained if In with 3 outer electrons is replaced by Zn and Sn with 2 and 4 outer electrons, respectively. Image adapted from Ref. [5].*

electrostatic potential fluctuations due to the [Cu_{Zn} + Zn_{Cu}] antisite defect complex. Indeed, due to the low formation energy of 0.21 eV for this defect [18] a large number of these defects is expected at room temperature [17]. A high Urbach energy was also observed by Redinger *et al.* [19]. Experimentally, a phase transition between the ordered and disordered kesterite was observed [4, 20–22], where the disordered kesterite is characterized by a random site occupation by Cu and Zn atoms in the Cu-Zn planes (see Fig. (1.1)). The critical temperatures are found to be 260 °C and 200 °C for the pure S [20] and pure Se [22] kesterite. Below these temperatures, the degree of ordering increases with lowering temperatures, but will reach the perfectly ordered state only at 0 K, i.e. there will be always [Cu_{Zn} + Zn_{Cu}] antisite defect states present at operating temperatures [22].

1.1. Defect characterization

All these points discussed above (small minority carrier life times, tailing) lead to the desire of a better understanding of the defects present in the kesterite samples to gather a better understanding of the low V_{oc}. One commonly applied technique for defect characterization is thermal admittance spectroscopy developed by Losee [23]. Measuring the capacitance (and conductance) with respect to frequency and/or temperature enables the detection of possible defect states in the sense that a drop in capacitance is observed from low to high frequencies and high to low temperatures. Walter *et al.* [24] refined this theory such that it is possible to extract defect distributions from an admittance spectrum. For the compound CIGSe for instance Hanna *et al.* [25] could show with the help of admittance spectroscopy that the concentration

of a specified defect correlates with the open circuit voltage deficit and that the lowest defect concentration is obtained for a [Ga]/([Ga] + [In]) of 0.3, which is the value where the best CIGSe devices are prepared (without potassium treatment) [26]. For CZTSe I could show that a deep defect distribution is introduced after annealing appearing as a broad high temperature capacitance transition with a detrimental effect on the V_{oc} [27].

In literature only a few papers are published dealing with admittance spectroscopy on kesterite based solar cells. Additionally, these papers discuss solely the commonly observed low temperature capacitance transition. A summary of these papers is given in Tab. 1.1. The first row indicates the material of the absorber, i.e. whether the measurements were done on pure S, pure Se or SSe devices.

The second row reports the appearance of the major capacitance transition. The major capacitance transition is characterized by exhibiting clearly identifiable inflection frequencies in the observed temperature range. Some groups find that this capacitance transition results from a single step, while others find this transition to be composed of two (generally overlapping) capacitance steps. Evidently, the appearance of this transition is not linked to the [Se]/([Se] + [S]) ratio. However, in almost all publications the high frequency and low temperature capacitance seems to be the geometrical capacitance. Despite that fact the observed capacitance step(s) are nevertheless often attributed (and also evaluated) as deep defects. Clearly, a better picture of the low temperature behaviour in admittance spectroscopy needs to be settled.

The third row indicates whether the above mentioned high temperature capacitance transition is observed. Interestingly, many groups also observe such a transition but no further investigations were carried out. Even the 10.1 % efficient CZTSSe device reported in Ref. [28] shows a strong rise of capacitance with lowered frequencies and increased temperatures pointing to the fact that also in these high efficient hydrazine processed absorbers the detrimental deep defect distribution is present.

Some groups also investigate the doping density either by capacitance-voltage (CV) profiling [29] or by drive-level capacitance profiling (DLCP) [30]. The deduced values are given in rows 4 and 5 in Tab. 1.1. The list for the reported values of doping densities is not complete. Many other groups also measured the doping density (by CV or DLCP) but not an admittance spectrum. These papers are therefore omitted in Tab. 1.1. However, while theoretically the Zn_{Cu} antisite defect is predicted to be the dominant doping acceptor [18], experimentally no conclusive picture can be drawn.

Within the scope of this thesis I have characterized CZTSe based solar cells with the help of admittance spectroscopy and CV measurements. Based on these measurements I will show that the high temperature capacitance transition is due to a broad deep defect distribution which has a detrimental effect on the V_{oc}. This finding is presented in section 5.5.2.2 and was also published in Ref. [27]. Thus, if this deep defect can be prevented by finding suitable annealing conditions, it would help to lower the above mentioned high V_{oc} deficit in kesterite based solar cells.

Concerning the major capacitance transition, I generally observed an overlapping double capacitance step for CZTSe devices as I have demonstrated in Ref. [27, 41, 43]. I will show that these steps occur below the space charge region (SCR) capacitance and therefore cannot be attributed to deep defect levels. In literature, the final capacitance step was interpreted as a carrier freeze-out [31]. However, in section 5.7 I will show that a mobility freeze-out is also a reasonable explanation. For the origin of the second capacitance step I suggest a barrier due to the buffer layer. This assumption is backed up by temperature dependent IV measurements.

Table 1.1.: *List of publications dealing with admittance spectroscopy on kesterite based solar cells.*

absorber	low temp. transition	high temp. transition	doping density	method	Ref.
CZTSSe	single step	yes	$8 \cdot 10^{15}$	DLCP	[28]
CZTSSe - CZTS	single step	no	$1 \cdot 10^{15}$ - $1 \cdot 10^{16}$	DLCP	[31]
CZTSSe	single step	yes	N/A	-	[32]
CZTSSe - CZTS	single step	yes, small	$1 \cdot 10^{15}$ - $1 \cdot 10^{16}$	DLCP	[33]
CZTSe	single step	no	$1 \cdot 10^{15}$	CV	[34]
CZTS	single step	no	N/A	-	[35]
CZTS	double step	N/A	N/A	-	[36]
CZTSSe	double step	yes, small	$1 \cdot 10^{16}$ - $1 \cdot 10^{17}$	CV	[37]
CZTSSe - CZTS	double step[a]	no	N/A	-	[38]
CZTS	double step	yes	N/A	-	[39]
CZTSe - CZTSSe	double step	yes	N/A	-	[40]
CZTSe	double step	yes	$1 \cdot 10^{15}$ - $1 \cdot 10^{17}$	CV	[41]
CZTSe	double step	(yes)[b]	$2 \cdot 10^{16}$	CV	[42]

[a] only one step (the higher energetic one) is discussed.
[b] capacitance spectra are not shown. But a deep defect around midgap was found by DLTS.

To be able to quantify the overlapping double capacitance step I will present a new evaluation method capable of fitting the complete temperature dependent capacitance spectrum (section 5.3.2). With that approach the double capacitance step is deconvoluted, which is not possible with the Walter method [24]. Additionally, this method allows the characterization of the afore mentioned high temperature capacitance transition which lead to the assignment to a detrimental deep defect distribution.

1.2. Overview of this thesis

I will start the thesis with a discussion of solar cell devices in chapter 2. It includes the theoretical description of a n^+p junction (section 2.1) followed by the actual solar cell structure used for CZTSe absorber layers (section 2.2). The last section 2.3 deals with the description and analysis of current-voltage (IV) curves. It discusses different recombination processes and how the parameters describing the IV curve can be extracted from experiment.

Chapter 3 describes the growth of CZTSe absorber layers. It first explains the PVD growth chamber (section 3.1), in which the precursor and absorber layers are grown. I have applied two different approaches for the growth of absorber layers: a sequential (section 3.2) and a high temperature co-evaporation process (section 3.3). The difference in the microstructure resulting from these growth processes was investigated by scanning electron microscopy (SEM) and is presented in section 3.5.

The experimental setup for IV, IVT and admittance measurements is presented in chapter 4.

Chapter 5 is dedicated to the characterization by capacitance measurements. If covers the theoretical background of CV and admittance measurements in sections 5.1 to 5.4. Sections 5.5 and 5.6 will then cover the experimental results for the sequentially processed and co-evaporated samples, respectively. A discussion on the interpretation of the major capacitance step seen by

admittance spectroscopy will be given in section 5.7. Section 5.8 summarizes the findings and information obtained from the capacitance measurements.

Chapter 6 deals with the characterization by temperature dependent IV measurements. The chapter introduces first the theoretical background in section 6.1. It covers the evaluation of the dominant recombination pathway and discusses possible mechanisms which lead to a thermally activated series resistance as it is observed experimentally. Section 6.2 and section 6.3 then discuss the results for the sequentially processed and co-evaporated samples, respectively. The interpretation of these results is then discussed and summarized in section 6.4.

In chapter 7 a common model is put up which describes the experimentally features from IVT and capacitance measurements.

CHAPTER

TWO

FUNDAMENTALS OF SOLAR CELL DEVICES

A solar cell is a semiconductor device and based on a pn junction. Is the n-type semiconductor much higher doped than the p-type semiconductor such a junction is called a n^+p junction. Such an asymmetric junction is the basis of thin film solar cells and will be discussed in section (2.1). For the thin film solar cells discussed in this work, the p-type semiconductor is the p-type CZTSe absorber layer and the Al:ZnO window layer is the n^+ side. However, the exact structure of a whole solar cell device includes more layers and it will be discussed together with its band alignment in section (2.2).

Finally, the current-voltage characteristics of a solar cell will be discussed in section (2.3). It includes the discussion of different recombination pathways and their impact on an IV curve.

2.1. n+p heterojunction

A np junction is the connection of a n-type and a p-type semiconductor. If the same material is used for the n-type and p-type semiconductor, the junction is said to be a homojunction, while the connection of two semiconductors of different materials is called a heterojunction.

In the following I will quickly sketch the derivation of the space charge distribution, which in turn will result in formulas for the SCR width and the built-in voltage. These quantities will later be needed to discuss capacitance-voltage measurements (see section 5.1). Detailed derivations can be found in more detail in common textbooks for example in Ref. [44].

Bringing the p- and n-type semiconductor in contact, electrons from the n-side flow into the p-side and holes from the p- to the n-side. As a consequence, positive and negative charged ions form on the n-side and the p-side, respectively and therefore an electrostatic field is built up. In thermal equilibrium the forces due to a gradient of the cnhemical potential and a gradient of the electric potential cancel out such that the gradient of the electrostatic potential E_F equals zero and no electron (or hole) current flows, that is:

$$J_i = \mu_i i \frac{dE_F}{dx} = 0, \tag{2.1}$$

where i is either n or p for electrons or holes, respectively. It needs to be pointed out that the total current J_i equals zero because the forces cancel out and not due to two currents, the diffusion and the drift current, with equal magnitude but different signs. [45].

Thus, with the condition of a flat Fermi level across the pn-junction in thermal equilibrium, the built-in voltage V_{bi} is given by

$$qV_{bi} = E_g - (qE_{fn\infty} + qE_{fp\infty}) = q\Psi_n + q\Psi_p, \tag{2.2}$$

where $E_{fn\infty}$ ($E_{fp\infty}$) denote the distance of the Fermi level from the conduction (valence) band of the n-type (p-type) semiconductor away from the junction and Ψ_n and Ψ_p the potential drop on the n- and p-side, respectively. A schematic of the notations of these values is shown in Fig. (2.1) for a pn homo junction . Therefore, with a higher doping density and thus a lower value of $E_{fn\infty/fp\infty}$, a higher V_{bi} is achieved.

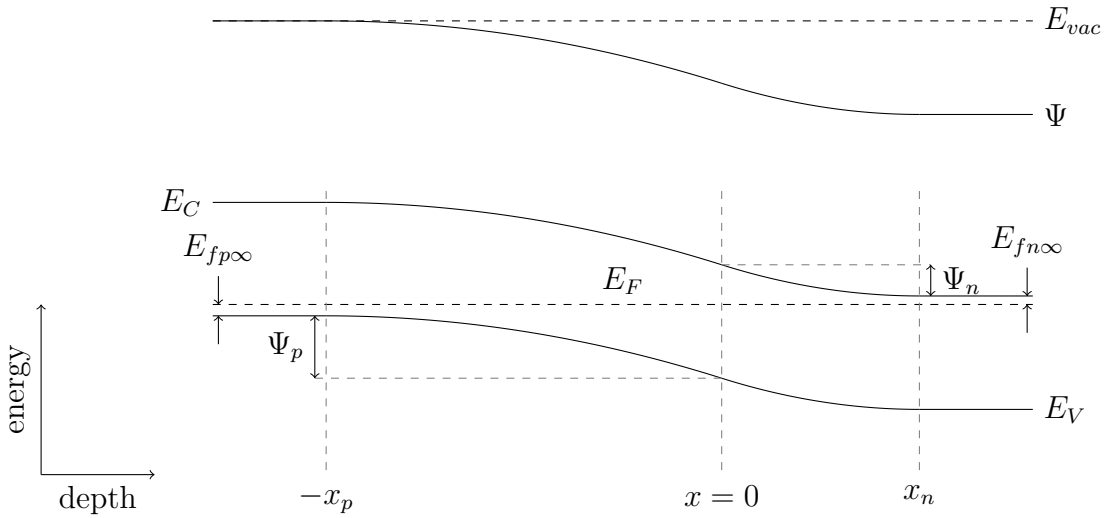


Figure 2.1.: ***Banddiagram of a pn homojunction*** *- Banddiagram is depicted in correct scale for a doping density of* $N_A = 5 \cdot 10^{15}\, cm^{-3}$ *and* $N_D = 1 \cdot 10^{16}\, cm^{-3}$*. Since* $N_A < N_D$*, the SCR extends further into the bulk of the p-type semiconductor compared to the n-type semiconductor.*

In order to calculate the SCR width we assume complete ionization of the dopants on each side, charge neutrality over the whole junction and an abrupt junction at $x = 0$. Additionally, we assume a box like charge distribution namely the depletion approximation. It assumes a space charge (per unit volume) of $-N_A$ extending until x_p on the p-side and a space charge of N_D until $-x_n$ on the n-side. Consequently, the charge neutrality reads:

$$N_A x_p = N_D x_n. \tag{2.3}$$

The SCR width is then obtained with the help of the Poisson equation, which links the electrostatic potential Ψ with the charge density ρ and reads

$$-\frac{\mathrm{d}^2\Psi}{\mathrm{d}x^2} = \frac{\mathrm{d}\mathcal{E}}{\mathrm{d}x} = \frac{q}{\epsilon_R \epsilon_0}\rho(x) \tag{2.4}$$

with

$$\rho(x) = \begin{cases} -N_D & : \; -x_n \leq x \leq 0 \\ N_A & : \; 0 < x \leq x_p. \end{cases} \tag{2.5}$$

$\mathcal{E}$ denotes the electric field, ϵ_R the dielectric constant of the material and ϵ_0 the vacuum permit-

tivity. By integrating Eqn. (2.4) the electric field across the SCR is obtained. At the transition from the p- to n-type semiconductor the electric field reaches its maximum $\mathcal{E}_m$ and reads

$$\mathcal{E}_m = \frac{qN_D x_n}{\epsilon_R \epsilon_0} = \frac{qN_A x_p}{\epsilon_R \epsilon_0}, \tag{2.6}$$

assuming the same ϵ_R for the p- and n-type semiconductor. Integrating Eqn. (2.4) a second time, the potential drops Ψ_p and Ψ_n on the p- and n-side respectively are obtained as

$$\Psi_p = \frac{qN_A x_p^2}{2\epsilon_R \epsilon_0} \qquad \text{and} \qquad \Psi_n = \frac{qN_D x_d^2}{2\epsilon_R \epsilon_0}. \tag{2.7}$$

Now, using Eqn. (2.2), (2.3), (2.6) and (2.7) the widths of the space charge regions are obtained with respect to the built-in voltage and the doping densities. For the p-side this is:

$$x_p = \sqrt{\frac{2\epsilon_R \epsilon_0 \Psi_{bi}}{q} \frac{N_D}{N_A(N_A + N_D)}} \tag{2.8}$$

and for the n-side:

$$x_n = \sqrt{\frac{2\epsilon_R \epsilon_0 \Psi_{bi}}{q} \frac{N_A}{N_D(N_A + N_D)}}. \tag{2.9}$$

Now, we assume $N_D \gg N_A$ as in a n^+p junction and Eqn. (2.8) and (2.9) simplify to

$$x_p \approx \sqrt{\frac{2\epsilon_R \epsilon_0 \Psi_{bi}}{qN_A}} \qquad \text{and} \qquad x_n \approx 0. \tag{2.10}$$

Thus, the SCR width only extends into the p-side and also the potential drops only on the p-side. For our structure the n^+-layer will be the highly doped window layer in general Al:ZnO and the p-layer the CZTSe absorber layer. Therefore, for many considerations the n^+p junction will be approximated as a Schottky contact as for example for admittance spectroscopy (see section 5.2. However, the structure of a whole solar cell device does not only consist of these two layers and will be discussed in section 2.2.

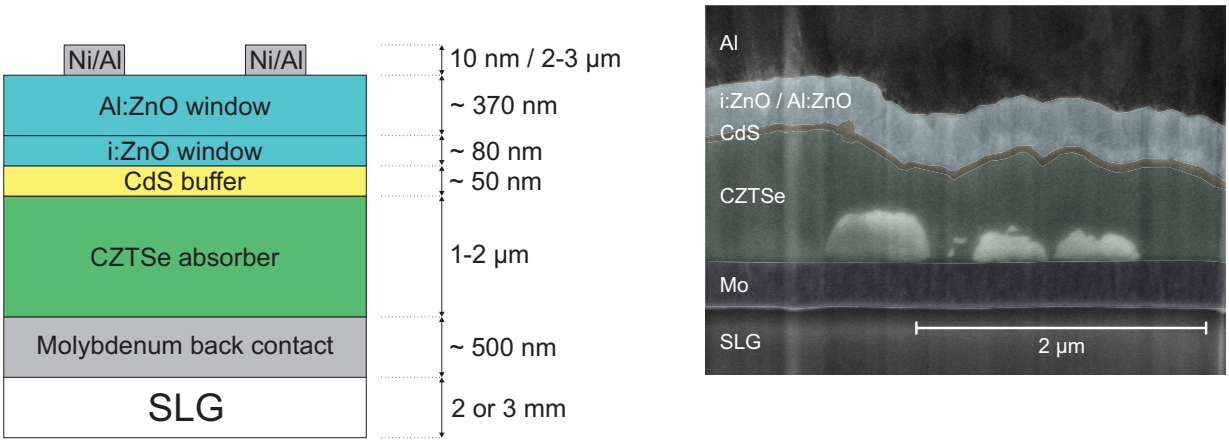
2.2. CZTSe solar cells

In the preceding section we discussed the simple case of a n^+p junction. However, in reality the structure of a solar cell is more complex and with it its bandalignment. These two topics will be discussed in the following two sections.

2.2.1. Solar cell structure

The schematic cross section of a CZTSe based solar cell is show in Fig. (2.2a).
The solar cell is in substrate configuration meaning that the absorber is grown on a metallic back contact and the light enters through a transparent conducting oxide (TCO), which represents the front contact.

The back contact consists of a roughly 400 nm sputtered Mo layer. On top of the Mo back contact the absorber or precursor layer is grown by co-evaporation, see sections (3.3) and



(a) Schematic of solar cell structure *(b) Cross section of a working solar cell device*

Figure 2.2.: ***A thin film solar cell device*** *- CZTSe based solar cell device in substrate configuration shown as a schematic (a) and of a real device (b). The Ni layer of the grid is to thin to be resolved and the difference between Al:ZnO and i:ZnO is only hardly visible. The cross section in (b) was prepared by a focused ion beam (FIB) from the device with a double CdS buffer layer (c.f. section 3.4).*

(3.2) for details on the absorber growth processes. The absorber layer represents the p-type semiconductor as discussed in section 2.1.

Between the n^+ window layer and the p-type absorber layer two additional layers are added. First comes the chemical bath deposited CdS buffer layer, which forms the crucial interface to the absorber layer. It only has a thickness of 50 nm, is n-type and has a doping density of nominally 1e16 cm^{-3}. Thus, when the pn-junction forms the buffer layer will be completely depleted of carriers.

On top of the buffer layer comes the TCO, which is the window layer. It is conductive enabling it to collect the carriers laterally while at the same time it is transparent such that photons can penetrate the window layer in order to get absorbed in the absorber layer. If not stated otherwise the TCO in general is a double layer of intrinsic ZnO (i:ZnO) and Al doped ZnO (Al:ZnO or AZO). The i:ZnO layer is deposited to add an artificial series resistance in order to reduce V_{oc} losses due to lateral inhomogeneities of the saturation current density J_0 [46, 47]. The AZO layer acts as the n^+ layer and as the front contact of the solar cell.

A grid is e-beam evaporated on top of the AZO layer for better current collection. It consists of a roughly 10 nm thick Ni layer and a 2-3 μm thick Al layer. In general a 2 μm thick Al layer is enough to yield a sufficient small resistance for good carrier collection. However, for some devices the thickness was increased to obtain a stronger grid which helps to contact the solar via bonding.

For our champion devices the AZO layer is replaced by a biased ZnO layer. The biased ZnO layer is characterized by a lower doping but higher electron mobility. It therefore has less absorption in the near infrared region while conserving the same sheet resistance compared to the AZO layer [48].

2.2.2. Bandalignment

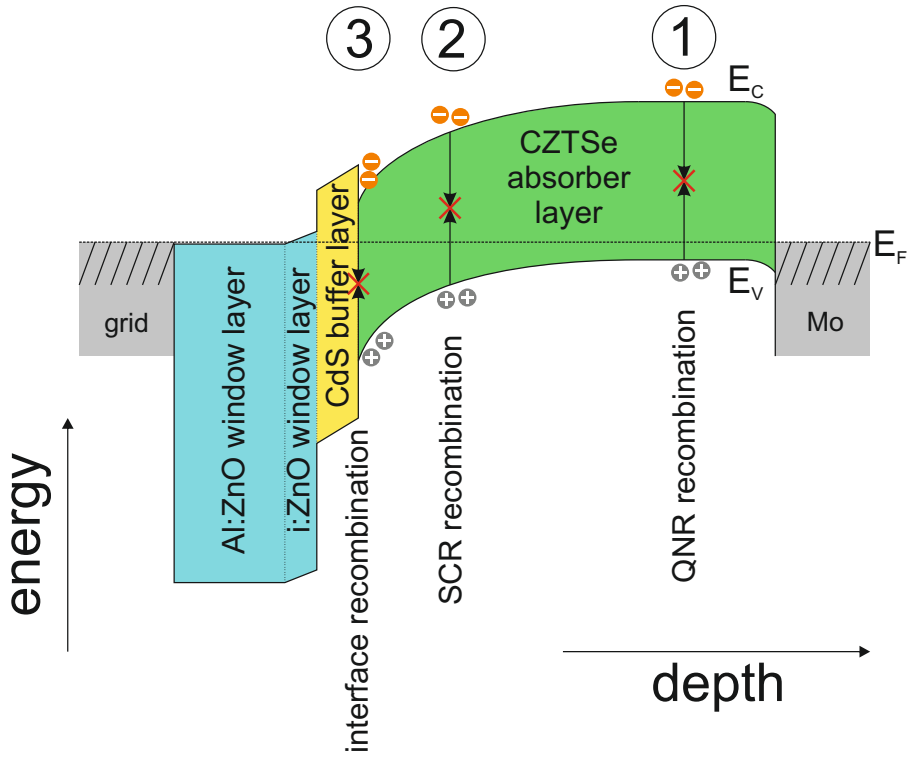


Figure 2.3.: ***Band diagram of a CZTSe solar cell*** *- Possible band diagram for the structure of a solar cell device. Assumed is a conduction band spike at the absorber-buffer interface as well as a small back barrier.*

The more complex solar cell structure compared to a n^+p junction goes along with a more complex band diagram compared to a Schottky contact. A possible band diagram is show in Fig. (2.3). Except the SLG substrate it contains all the layers as shown in Fig. (2.2a). It needs to be pointed out that this alignment only represents one possibility. It is depicted with a positive conduction band offset $\Delta E_C > 0$ and a back barrier, which might exist at the CZTSe/Mo interface [49].

According to Ref. [50], the conduction band offset is defined as $\Delta E_C = E_C^l - E_C^s$, where E_C^l and E_C^s stand for the energy of the conduction band minimum of the semiconductor with the large and the small bandgap, respectively. The values of E_C itself is given by the electron affinity χ of the semiconductor. In the same way as the conduction band offset, the valence band offset is defined: $\Delta E_V = E_V^s - E_V^l$. The band alignment featuring $\Delta E_C > 0$ is said to have a conduction band spike, while a negative band offset $\Delta E_C < 0$ is said to have a conduction band cliff. For this structure in this work the large and small bandgap semiconductor is CdS with $E_g = 2.4\,\text{eV}$ [50] and CZTSe with a bandgap of roughly $1\,\text{eV}$ [51].

Experimentally there are no direct or indirect measurements for the band offset between CZTSe and CdS. Only for the sulphur containing compound CZTS there are measurements showing a cliff-like alignment [52–54]. However, for CZTSe there are indications of a conduction band spike as deduced from electrical measurements [55], from UPS measurements [56] and from theoretical calculations [57]. In general, for thin film solar cell devices a conduction band spike is favourable only if ΔE_C is not exceeding $0.3\,\text{eV}$ [58]. For higher conduction band offsets

the spike acts as a barrier for photo generated electrons from the absorber layer. In fact, the limiting current density over a conduction band spike assuming thermionic emission is given by [50, 58]:

$$J_{0,TE} = \frac{1}{4q\nu_n} n_{a,z=0} \exp\left(-\frac{\Delta E_C}{kT}\right). \tag{2.11}$$

$n_{a,z=0}$ gives the density of free electrons at the interface. Thus, to pass a certain current density over a given conduction band spike ΔE_C requires a sufficient high density of free electrons at the interface, which is accomplished by a good inversion layer. An inversion layer (in the absorber) at the CdS/CZTSe interface means that minority carriers in the bulk of the absorber become majority carriers at the interface [59]. This property is given for a Fermi level which is closer to the conduction band than to the valence band (see Fig. 2.3). For a good inversion layer it is required that the doping level of the absorber layer is not too high. If the doping density is low enough, the built in potential drops mainly in the absorber layer (see section 2.1) and thus inverts the surface. The beneficial effect of an inversion layer also affects the recombination at the interface and will be discussed in section 2.3.1.

The band offset between the buffer and the window layer is also not allowed to be too large as it can act as a barrier for the diode current [50]. However, the window/buffer band offset will not be discussed here, as it is not object of the experimental section.

2.3. IV analysis

An IV curve in general is described by the 1-diode model, where the current density $J(V)$ expresses as:

$$J(V) = J_0 \left[\exp\left(\frac{q\,(V - r_s J)}{AkT}\right) - 1\right] + \frac{V - r_s J}{R_{sh}} - J_{ph}. \tag{2.12}$$

J_0 is the saturation current density, r_S the series resistance, R_{sh} the shunt resistance, A the diode quality factor, k the Boltzmann constant and T the temperature. The saturation current density is thermally activated with an activation energy E_A and can be written in the form

$$J_0 = J_{00} \exp\left(-\frac{E_A}{AkT}\right) \tag{2.13}$$

where J_{00} is the reference current density. Depending on the recombination pathway different values for J_{00}, E_A and A are obtained. A complete overview is given in [50]. At open circuit conditions and assuming $V_{oc}/R_{sh} \ll J_{ph}$, Eqn. (2.16) can be resolved with respect to V_{oc} and reads

$$V_{oc} = \frac{E_A}{q} - \frac{AkT}{q} \ln\left(\frac{J_{00}}{J_{ph}}\right). \tag{2.14}$$

From this equation it is evident that the three parameters E_A , A and J_{00} are important parameters responsible for the V_{oc} of the solar cell. E_A directly affects the V_{oc}, while A and J_{00} are multiplicative factors additionally reducing the V_{oc}. Note that J_{00} is generally much larger than J_{sc} [60, 61] and thus $\ln(J_{00}/J_{ph}) > 0$. An effect of the diode quality factor on V_{oc} is simulated and shown in Fig. 2.4a for three different values of A while keeping the rest of the

parameters constant.

2.3.1. Recombination processes

Three different recombination processes are shown in Fig. (2.3), which can occur in our solar cell devices and can be described by [50]:

$$J_{\text{diode}} = qD_n \left.\frac{\mathrm{d}n(x)}{\mathrm{d}x}\right|_{x=x_p} + q\int_{x_p}^{0} (U_n(x) - G_0(x))\,\mathrm{d}z + J_{\text{diode, IF}}. \tag{2.15}$$

D_n is the electron diffusion coefficient, $G_0(x)$ the thermal generation rate and $U_n(x)$ the recombination rate. The right hand side of Eqn. (2.15) describes the three contributions to the diode current J_{diode} from the quasi neutral region (QNR) $J_{\text{diode,QNR}}$, from the SCR $J_{\text{diode,SCR}}$ and from the absorber/buffer interface $J_{\text{diode,IF}}$. The contribution due to back surface recombination is neglected due to low minority carrier diffusion lengths in CZTSe absorber layers [14]. The voltage and temperature dependence of each of these contributions can be described by an exponential form like

$$J = J_0\left[\exp\left(\frac{qV}{AkT}\right) - 1\right] \qquad \text{with} \qquad J_0 = J_{00}\exp\left(\frac{-E_A}{AkT}\right). \tag{2.16}$$

The exponential voltage dependence of the diode current results from the exponential voltage dependence of the carrier densities, which governs the recombination rates.

Eqn. (2.16) contains three parameters, which are specific for different recombination mechanisms.

- diode quality factor A: The diode quality factor A describes the voltage dependence of the diode current. It depends on the type of recombination and where the carriers recombine (i.e. interface, SCR or QNR). An overview about the diode quality factors and their temperature dependencies is given in Ref. [50].

- activation energy E_A: The activation energy E_A represents the activation of the saturation current density J_0 and therefore the temperature dependence of the diode current. For a good heterojunction the activation energy is given by the absorbers bandgap. However, due to a conduction band miss alignment or Fermi level pinning also lower activation energies are possible for recombination at the interface [62].

- reference current density J_{00}: The prefactor of the saturation current density is specific for different recombination processes. Especially for tunnelling enhanced recombination the value of J_{00} can be strongly increased, and therefore significantly increases also J_0. An overview about values of J_{00} dependent on the different recombination processes is given in Ref. [50] Tab. 2.2.

All three recombination processes shown in Fig. (2.3) happen in parallel. However, dependent on the value of J_0 (due to the parameters J_{00} , E_A and A) one recombination process can dominate over the others and thus gives the diode current J_{diode}. Still, due to different voltage dependencies it is still possible that a process with a high diode quality factor dominates at low voltages, while another process with a small diode quality factor dominates at higher voltages.

Radiative recombination in the QNR is the recombination which ultimately limits the solar cell performance via the Shockley-Queisser limit [8]. However, this recombination process is not the limiting process for thin film solar cells. For instance for CIGSe based solar cells the radiative lifetime was found to be $\tau_{rad} \approx 1\mu s$, while measured lifetimes are of the order of ns [63]. Thus, for the compound CIGSe the radiative recombination is not limiting the solar cell performance. Also for the compound CZTSSe measured lifetimes are below 10 ns [14, 17, 64] and thus excludes radiative recombination to be responsible for limiting the performance of these devices.

We therefore focus on non-radiative recombination via deep defect states - the Schockley-Read-Hall recombination [65, 66].

2.3.2. Schockley-Read-Hall recombination

Schockley-Read-Hall (SRH) recombination is the recombination of carriers via localized states within the bandgap. In that case the recombination rate can be written as [50]

$$R_{\mathrm{SRH}} = \frac{np - n_i^2}{\gamma_p(n + n^*) + \gamma_n(p + p^*)}, \tag{2.17}$$

where n^* and p^* are auxiliary carrier densities which would be realized if the Fermi level were at the defect level. In the absence of tunneling enhanced recombination γ_p and γ_n are the minimum carrier lifetimes $\tau_{p,0}$ and $\tau_{n,0}$ for holes and electrons respectively and defined as

$$\tau_{p,0} = (\sigma_{p,0} v_{p,0} N_t)^{-1} \qquad \text{and} \qquad \tau_{n,0} = (\sigma_{n,0} v_{n,0} N_t)^{-1} \tag{2.18}$$

$\sigma_{p/n}$ and $v_{p/n,0}$ is the capture cross section and the thermal velocity for holes/electrons and N_t is the number of trap sites per unit volume. Taking also tunnelling enhanced recombination into account, the quantities γ_p and γ_n contain an additional factor, accounting for an increased carrier density at the trap site. These quantities can be expressed as [67]:

$$\gamma_p = \tau_{p,0}\,(1 + \Gamma_p)^{-1} \qquad \text{and} \qquad \gamma_n = \tau_{n,0}\,(1 + \Gamma_n)^{-1} \tag{2.19}$$

From Eqn. (2.19) it becomes evident that the locally increased carrier density due to tunneling results in lowered lifetimes for the free carriers.

As mentioned above, recombination can occur in the SCR, in the QNR and at the heterointerface. Now I will discuss briefly the impact of the region of recombination on the diode parameters, in the case of SRH recombination.

2.3.2.1. SCR recombination

Based on Eqn. (2.17) the SRH recombination rate takes its maximum at the position where $\tau_{p,0}^{-1} p = \tau_{n,0}^{-1} n$ and therefore is located in the SCR. For SRH recombination in the SCR the diode quality factor equals 2. The picture behind a diode quality factor of 2 is that at the point of maximum recombination, where $\tau_{p,0}^{-1} p = \tau_{n,0}^{-1} n$, the quasi Fermi levels move symmetrically with respect to the defect level. Therefore, each Fermi level moves $qV/2$ and thus $A = 2$.

However, assuming an exponential defect distribution [68], also voltage independent diode quality factors between 1 and 2 are possible.

Considering additionally tunnelling enhanced recombination, diode quality factors above 2 are possible [69]. Tunnelling enhanced recombination not only alters the diode quality factor

but also deteriorates J_0via J_{00}. The contribution due to tunnelling on J_0 gets severe at room temperature for doping densities $N_A > 2e16\,cm^{-3}$ [50].

For all recombination processes in the SCR the activation energy of J_0 is always equals the absorber bandgap E_g. Even in the case of tunnelling enhanced recombination an activation energy of E_g is obtained as it only increases the number of free carriers at the site of recombination. Thus, as already mentioned, increases the saturation current density.

2.3.2.2. QNR recombination

However, even though the maximum of recombination happens in the SCR, the diode current can still be dominated by recombination in the QNR. Dominated QNR recombination occurs for sufficient high carrier lifetimes so that the carriers first drift out of the SCR before they recombine [50]. For recombination in the QNR the diode factor equals 1 as long as the bias voltage is not too large, such that the condition of low injection is still fulfilled. Under low injection conditions the majority quasi Fermi level stays roughly constant and only the minority quasi Fermi level moves with respect to the voltage, which is qV; thus, $A = 1$. Evidently, as for SCR recombination the activation energy is given by the absorbers bandgap.

2.3.2.3. Interface recombination

The recombination processes discussed above all yield an activation energy of J_0 equal to the bandgap. However, due to recombination via deep defect states at the interface also activation energies below E_g can occur for certain scenarios.

For the following considerations we only take an asymmetric n^+p junction into account and recombination via deep defect sates. For the n^+p junction the electrons are majority carriers at the interface and thus we write $n_{\mathrm{IF}} \gg p_{\mathrm{IF}}$. Eqn. (2.17) can then simplified to

$$R_{SRH} = p_{\mathrm{IF}}\gamma_p^{-1} = p_{\mathrm{IF}}S_p, \tag{2.20}$$

where S_p denotes the surface recombination velocity. For this case there are then two reasons for a lowered activation energy than the absorber band gap:

One reason is a conduction band cliff, i.e. $\Delta E_C < 0$. For this scenario we assume that cross recombination is possible, i.e. electrons of the buffer layer can recombine with holes of the absorber layer. This results in a reduced interface bandgap $E_{g,IF} = E_g + \Delta E_C$, with $\Delta E_C \leq 0$ [62] and therefore the activation energy is lowered compared to the absorbers bandgap.

The second reason for a reduced activation energy is a pinned quasi Fermi level of the majority carriers at the interface. For a n^+p junction this is the electron quasi Fermi level. Then the electron concentration at the interface is constant and does not change with bias voltage. The activation energy is given by temperature independent quantity Φ_b^p, which is the energetic distance of the absorber valence band to the hole quasi Fermi level at the interface. Experimentally, this activation energy can be deduced by temperature dependent IV (IVT) measurements and Eqn. (2.14). IVT measurements will be discussed in section 6.1.

2.3.3. Solar cell parameters

In section 2.3 I have discussed the three parameters E_A, A and J_{00} describing the diode current. However, in order to characterize the efficiency of the solar cell, there is a set of parameters directly available from the measurement, namely the open circuit voltage V_{oc}, the short circuit

current density J_{sc}, the fill factor FF and the power conversion efficiency η . J_{sc} gives the photo current at zero applied bias voltage and V_{oc} is the voltage in open circuit conditions, when no current flows. With the current density J_m and the voltage V_m at the maximum power point, the FF is defined as

$$FF = \frac{V_m J_m}{V_{oc} J_{sc}}. \tag{2.21}$$

The (power conversion) efficiency is defined as the ratio of the generated electrical power and the incoming power as

$$\eta = \frac{P_{out}}{P_{in}} = \frac{V_m J_m}{P_{in}} = \frac{FF V_{oc} J_{sc}}{P_{in}}. \tag{2.22}$$

A simulated IV curve according to Eqn. (2.12) is shown in Fig. (2.4a). Annotated are the points at V_{oc} and at J_{sc}. From this image the FF is defined as the ratio of the area of the light grey rectangle and the dark grey rectangle and therefore can be pictured as the squareness of the IV curve. Also shown as dashed lines are IV curves with diode quality factors of 1 and 2. The effect on the IV curve is a lowered V_{oc} according to Eqn. (2.14) as well as the voltage dependence of the exponential function. This can be seen by the current onset of the exponential function, which is more abrupt for $A = 1$ compared to $A = 2$. In Fig. (2.4b) the same IV curve is shown on a logarithmic ordinate with the same set of parameters (solid red line). From this graph three regions can me made out. The first region 1) is dominated by the shunt resistance and therefore is present as a logarithmic function on the logarithmic scale. The second region 2) represents the diode as a straight line with a slope of $1/AkT$. This region is only apparent if the series resistance is not too high. The third region 3) in far forward bias is dominated by the series resistance. With a logarithmic scale the presence of a series resistance is seen by the bending of the IV curve from the straight line of region 2).

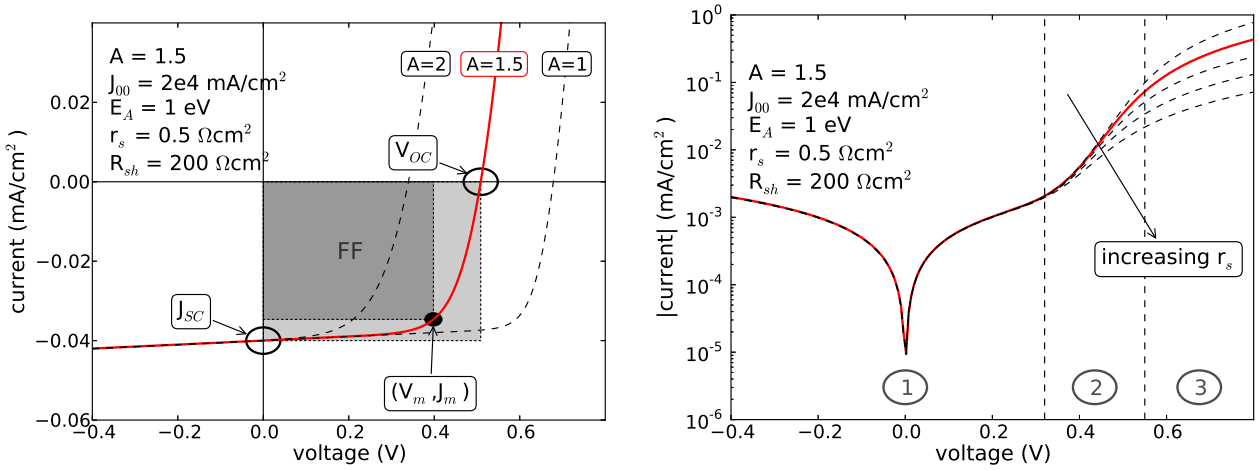
2.3.3.1. Determination of solar cell parameters

There exist several methods on how to extract the solar cell parameters from a measured IV curve. In this section I will focus on two methods, to which I will refer later on for the determination of the IV parameters.

iv-fit This methods fits the measured IV curve to Eqn. (2.12) [70]. It needs to be pointed out that a orthogonal-distance regression is used in order to account for the strongly varying slope of the IV curve.

Sites-method This method was first introduced by Sites and Mauk [71] and later extended by Hegedus and Shafarman [72]. It relies on the certain approximations and manipulations of Eqn. (2.12) such that in consecutive plots the IV parameters are obtained. However, in order to correctly account for the shunt resistance for the determination of r_S and A, the formula used in [71] needs to be used and not the one given in Ref. [72]. The derivation is given in appendix (A). The actual determination of the IV parameters was done by a Python script and is discussed in detail in section A.2.

For both methods only the saturation current density J_0 is obtained. In order to also get the values for J_{00} and E_A, temperature dependent measurements are necessary, as discussed in section 6.1.



(a) Solid red line according to parameters given in the figure. Dashed black lines are IV curves with diode quality factors of 1 and 2.

(b) Variation of the series resistance r_S. Solid red line is simulated with the same parameters as in Fig. (2.4a) but without a photo current.

Figure 2.4.: *Simulation of IV curves* *- Simulation according to Eqn. (2.12). Annotated are the quantities V_{oc}, J_{sc} and FF. The dashed lines show IV curves with the same set of parameters but with a diode quality factor of 1 and of 2. The maximum power point is denoted as (V_m, J_m), Fig. (2.4a). Fig. (2.4b) shows the IV curve on a logarithmic scale with a variation of the series resistance.*

CHAPTER

THREE

GROWTH OF THE CZTSE ABSORBER LAYER

The growth of the CZTSe absorber layer is described in this chapter. It is divided in two sections: section 3.2 is dedicated to the sequential process and section 3.3 to the high temperature co-evaporation process. Both techniques have in common that the materials (Cu, Zn, Sn, Se) are deposited by co-evaporation in an molecular beam epitaxy (MBE) chamber. This system is described in section 3.1. Section 3.5 compares the differences in microstructure arising from the different growth techniques by polished SEM and TEM images.

3.1. PVD system

Precursor (section 3.2) and absorber (section 3.3) layers are grown in an MBE chamber, which is sketched in Fig. (3.1). SnSe, Cu, Zn and Sn are evaporated from effusion cells and Se is supplied by a valved cracker source. Elemental fluxes were controlled by changing the bulk temperature of the sources and measured by a quartz crystal monitor and a Bayard Alpert pressure gauge.

The sample chamber is pumped by a turbo molecular pump and additionally cooled with liquid nitrogen to achieve a pressure (during growth) of $\sim 10^{-8}$ torr. The sample holder is rotated during growth to improve homogeneity and can be heated as indicated in Fig. (3.1). Four inch $\times$ inch substrates can be mounted into the sample holder. Thus four identical absorber/precursor samples are obtained from each process run. A pyrometer with a detection range from 2 μm to 2.6 μm measures the temperature of the substrate and allows *in-situ* process control. Also diffuse laser light scattering (LLS) is measured during the growth processes, but will not discussed in this thesis. Details about growth monitoring by LLS can be found for example in Refs. [19, 73].

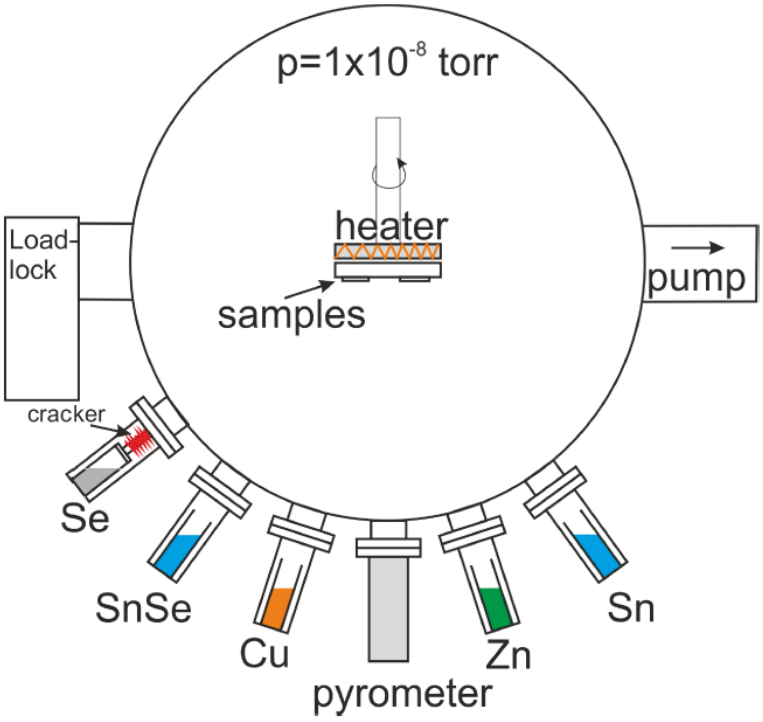


Figure 3.1.: ***MBE chamber*** *- For deposition of CZTSe precursor and absorber layers. Included are SnSe, Cu, Zn and Sn effusion cells. Se is supplied by a valved cracker source. Image take with permission from Alex Redinger (unpublished).*

3.2. Sequential process

The solar cells fabricated from absorbers processed with a sequential process are described in this section. Section 3.2.1 explains the difficulties in growing high quality kesterite layers and gives a motivation for the sequential process. The growth of two different kinds of precursors is presented in section 3.2.2 and section 3.2.3. The high temperature annealing procedure needed for a good crystal structure is described in section 3.2.4.

3.2.1. Decomposition reaction

One problem which occurs at high temperatures is the decomposition reaction of the kesterite phase given in Eqn. (3.1) [74, 75]:

$$Cu_2ZnSnS(e)_4 \leftrightarrow Cu_2S(e) + ZnS(e) + SnS(e) + \frac{1}{2}S(e)_2(g). \tag{3.1}$$

This equation also holds if the chalcogen species S is replaced with Se (thus the notation of $S(e)$) in order to obtain CZTSe [76]. As I am dealing in this thesis with pure Se based absorbers, the discussion in the following is based on CZTSe. From Eqn. (3.1) if follows that Se is lost from the film. Due to the high vapour pressure of SnSe at these temperatures [77], also Sn losses are expected [78]. In order to prevent the decomposition reaction, a SnSe and Se vapour pressure needs to be supplied to keep the reaction in equilibrium, i.e. shift the reaction to the left hand side.

Thus, based on these considerations of the decomposition reaction which can occur at high

temperatures motivates the approach of a sequentially processed absorber layer: First, a precursor is grown at low temperatures, where no elemental losses from the film are observed [79]. In a second step this precursor is annealed at high temperatures - with the addition of Se and SnSe into the annealing chamber a Se and SnSe partial pressure is created to prevent the decomposition reaction (3.1). These high vapour pressures of SnSe and Se cannot easily be supplied in a PVD chamber.

Another decomposition reaction of the kesterite phase which was proposed in literature is the back contact reaction with Mo [80, 81]. It suggests that the CZTS/Mo interface is thermodynamically not stable at the commonly applied annealing temperatures (> 500 °C) and thus decomposes. The result is that a MoS_2 layer and secondary phases form at the back contact. However, a study by Shin *et al.* [82] on pure Se based absorbers shows that the formation of an intermediate $MoSe_2$ layer between CZTSe and Mo is due to the diffusion of Se through the absorber layer and not due to a decomposition reaction. Note that the experiments by Scragg *et al.* [80, 81] were carried out with pure S containing precursors, while Shin *et al.* [82] used pure Se precursors.

The samples which are produced by the sequential process presented here also exhibit a $MoSe_2$ layer at the back contact. The thicknesses were determined by polished TEM images and are around 100 nm. However, detrimental effects of the $MoSe_2$ layer were observed for thicknesses above 600 nm [83]. Besides, the state-of-the-art CZTSe devices with a 11.6 % efficiency exhibits a $MoSe_2$ layer of roughly 200 nm as well [11]. Thus, the formation of the $MoSe_2$ layer is not further investigated in the framework of this thesis as it seems not to be detrimental.

3.2.2. Precursor growth at 320 °C

The following discussion is based on the growth process by Mousel *et al.* [84]. Besides, the precursors and the resulting absorbers were grown by Marina Mousel as well. However, the sequentially processed solar cells discussed in section 5.5 and 6.2 arise from this growth process, which is therefore described in this section.

The precursor is grown at 320 °C in the PVD chamber at constant fluxes of Cu, Zn, Sn and Se. The precursor growth temperature was kept below 350 °C to prevent expected Sn and Se losses [79]. The precursor was grown under Cu-rich conditions. It is known from CIGSe that a Cu-rich phase in the growth process improves the grain growth, which was also found for the CZTSe compound [9, 84]. A consequence of a Cu-rich precursor growth is that a $Cu_{2-\delta}Se$ phase forms on the surface [84]. This $Cu_{2-\delta}Se$ phase needs be etched by KCN [85] prior to annealing to obtain working solar cell devices. Otherwise a detrimental Cu-Sn-Se phase forms on the surface during annealing [86]. After the KCN etch, the precursors shift to a Cu-poor composition due to the removal of the copper selenide layer [84]. These resulting Cu-poor precursors are subsequently annealed following the high temperature annealing process as described in section 3.2.4.

3.2.3. Precursor growth at low temperatures

Similar to the deposition of the precursor described in the previous section, the growth temperature can even be lowered. The heater of the sample holder was switched off during the growth process of these precursors. Nevertheless, heating still occurs from the sources itself. The tip temperature of the Cu and Sn evaporation sources is around 1300 °C. This means that

the samples are radiatively heated from the sources. The exact sample temperature cannot be estimated and is assumed to be around 100 °C.

A motivation of this process is to grow a precursor layer which is as homogeneous as possible and to reduce the segregation of secondary phases. Besides, the highest efficiency for pure Se based absorber layers are currently obtained from a sequential process with a growth temperature of the precursor of 150 °C [11].

Fig. (3.2) shows the compositional depth profile of a precursor measured by an EDX cross sectional linescan (Fig. (3.2a)) and by secondary ion mass spectroscopy (SIMS) (Fig. (3.2b)).

Full symbols/dashed lines in Fig. (3.2a) show the compositional depth profile when the Mo peak is taken into account for the evaluation of the EDX data. The Mo peak is seen throughout the sample thickness due to the interaction volume of the electron beam. Thus, the same data was evaluated without taking the Mo peak into account (open symbols, solid lines). From this data a homogeneous in-depth composition can be deduced. The SIMS profile in Fig. (3.2b) shows a rather homogeneous Zn, Sn and Se concentration, while a strong gradient is observed for the Cu concentration. However, the exact same Cu gradient was obtained when the sample was ripped off from the substrate and measured from the back to the front surface. Therefore, it is concluded that the strong Cu gradient in the SIMS profile is an artefact of the measurement. A possible explanation could be that the sputtering process promotes the diffusion of Cu atoms deeper into the film resulting in such a Cu profile. Such a phenomenon is not observed for the samples grown at 320 °C [84] and could be due to the amorphous structure of the precursor film (due to the low growth temperature). In conclusion:

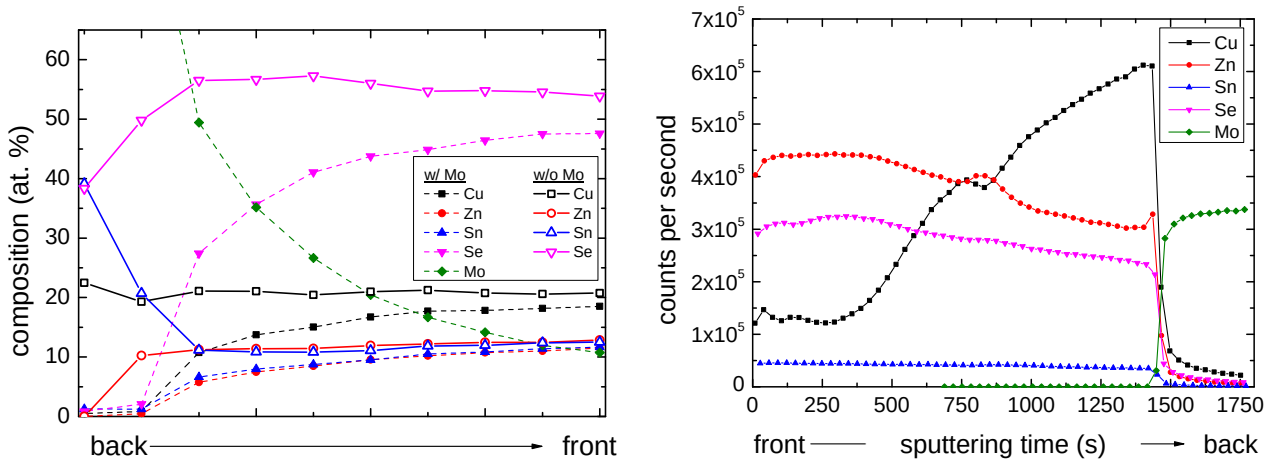
1. The SIMS profiles are not reliable for these kind of precursors due to artefacts of the measurements.

2. EDX linescanes indicate a homogeneous compositional depth profile.

3.2.4. High temperature annealing

In order to form the kesterite crystal structure, the precursors need to be heated to high temperatures [78, 87]. This annealing procedure is done in a tube furnace as it is depicted in Fig. (3.3). The sample is placed inside a graphite box, which itself is put into a quartz tube. The quartz tube is heated from the outside as indicated by the heaters (red bars). A thermocouple is pressed with a screw against an inside wall of the graphite box to measure its temperature. Additional Se and SnSe can be placed into the cavities inside the graphite box in order to create a SnSe and Se atmosphere at high temperatures and consequently to prevent the decomposition reaction of CZTSe (see section 3.2.1). The removable lid has a small hole in the middle in order to allow for pumping and flushing of the inside of the graphite box. The sample is not placed directly under the hole as the SnSe and Se atmosphere is expected to be less homogeneous in this area. Indeed, annealed samples show less homogeneity if the sample is placed under the hole, which is visible by eye.

The temperature profile of an annealing process is depicted in Fig. (3.4). The green curves represents the setpoint of the temperature and the blue curve the measured temperature of the thermocouple shown in Fig. (3.3). The annealing process can be described by the following steps:



(a) EDX linescan (b) SIMS profile

Figure 3.2.: ***Compositional depth profile of low temperature precursor*** *- (a) shows an EDX linescane across a cross section of a precursor deposited at 100 °C with an acceleration voltage of 7 keV. Analysis was made w/ (solid symbols) and w/o (open symbols) taking the Mo peaks into account. A flat compositional profile is observed when not taking into account the Mo peaks. (b) shows a SIMS profile of the same precursor. A strong Cu gradient is observed from the front to back contact, which is an artefact of the measurement.*

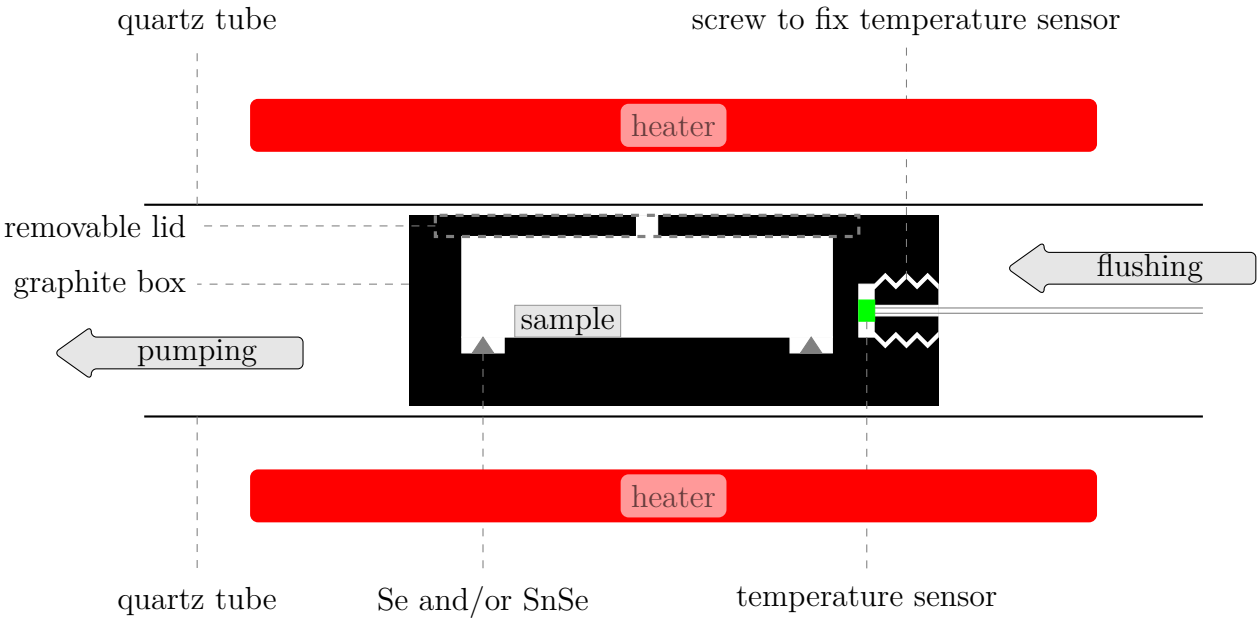


Figure 3.3.: ***Tube furnace for high temperature annealing process*** *- Sample is placed inside a quartz tube. Additional Se and/or SnSe can be placed into the cavities of the inside of the graphite box to prevent the decomposition reaction of CZTSe at high temperatures (see section 3.2.1). A temperature sensor is pressed at the wall inside the graphite box in order to determine the temperature of the graphite box.*

1. Mounting of the sample and additional Sn and SnSe inside the graphite box and evacuating the quartz tube.
2. 4 x flushing with N_2 at room temperature.
3. Heating to 100 °C.
4. 4 x flushing with H_2/N_2, when the graphite's temperature is above 100 °C.
5. Setting a background pressure of 1 mbar H_2/N_2.
6. Heating to 520 °C.
7. Annealing at 520 °C for about 30 minutes, i.e. timespan the measured temperature of the graphite box is at 520 °C.
8. Natural cool down to room temperature

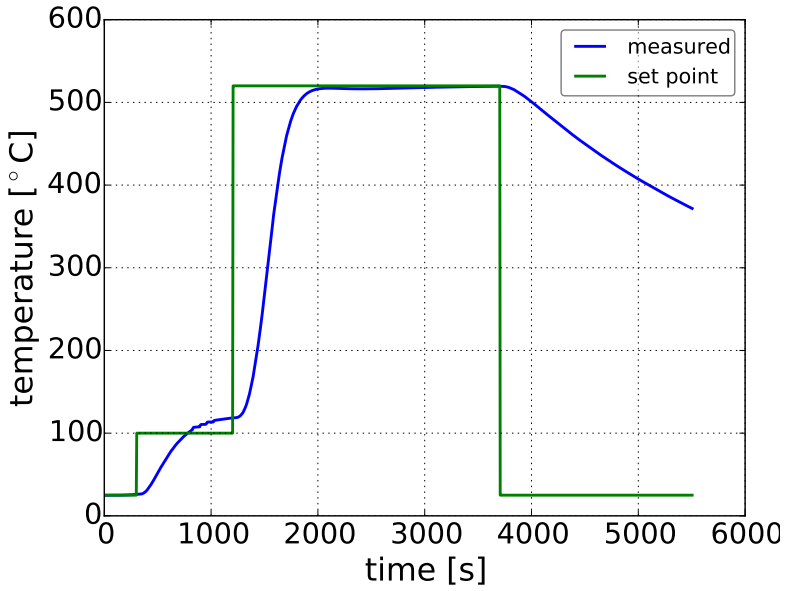


Figure 3.4.: ***Temperature profile from the high temperature annealing process*** *- The annealing time at 520 °C is roughly 30 minutes. The measured temperature corresponds to the reading of the thermocouple pressed against the graphite box (see Fig. (3.3)).*

Generally, 20 mg of Se powder and 15 mg of SnSe chunks were used to supply the Se and SnSe atmosphere. The powder and chunks were split roughly in half and put into the two cavities of the graphite box.

3.3. High temperature co-evaporation

For the growth of the absorber layers described in this section, the substrate temperature is set to high temperatures and thus no additional annealing process is required. In order to prevent the decomposition reaction as described in section 3.2.1, the substrate temperature is set only to 470 °C such that the required Se overpressure does not need to be as high as for the

sequential process [1]. Besides, a SnSe evaporation source is used to stabilize the decomposition 3.1 mentioned in section 3.2.1.

3.3.1. Overview of literature processes

In the initial co-evaporation deposition stage only ZnSe and Cu_xSe_y forms at the back contact while Sn is not incorporated into the film [73, 79, 88–90]. This penomenon was also observed for CZTS [91]. Kaune *et al.* [73] suggest that this is related to the detrimental decomposition reaction with Mo. However, the expected thickness of the $MoSe_2$ layer from this reaction is too large for the decomposition reaction to be the sole reason that Sn is not incorporated in the early stage of the deposition. According to my best knowledge, there is no published study explaining the delayed formation of the kesterite phase. However, as Cu_xSe_y exists independent on whether Cu-rich (Cu/Zn flux > 1) or Zn-rich (Cu/Zn flux < 1) growth conditions are applied, a possible (liquid-phase assisted [92, 93]) grain growth due to Cu_xSe_y is possible in both cases [94].

Continuing the deposition process, the Cu_xSe_y is consumed to form CZTSe [89]. The ZnSe in contrast is only consumed if the ongoing deposition is Cu-rich enough [94]. Another factor determining the consumption of ZnSe might be the substrate temperature [89], i.e. at lowered substrate temperatures the diffusivity of atoms reduces such that the buried ZnSe at the back side cannot react to form CZTSe.

Another approach to reduce the growth of ZnSe at the back side of the film is a lowered substrate temperature at the beginning of the process [19, 95, 96]. In that case the ZnSe growth is reduced and the growth of CZTSe is not delayed [95].

It has been shown by Hsu *et al.* that ZnSe grains at the back contact are not harmful to device performance [94, 97]. Nevertheless, large amounts of ZnSe, i.e. almost complete layers, diminish the solar cell performance [95, 98].

At the end of the process, the Cu flux is shut down prior to the Zn flux if Cu-rich growth conditions are applied in order to end up with a Cu-poor absorber layer [99]. Additionally, a Zn-rich surface layer is induced which was shown to increase the efficiency of the solar cell [100].

3.3.2. Our process

The standard process of the co-evaporated absorber layers used in this thesis is shown in Fig. (3.5). The upper and the lower graph show the temperature profile and the shutter status during the growth process, respectively. The temperature of the evaporation sources were kept constant throughout the deposition process, which results in constant elemental fluxes. In that case the growth conditions are Zn-rich. To increase the reactivity of Se, the cracker is heated to 1000 °C. The substrate is preheated to 500 °C. The processes then starts with decreasing the substrate temperature in order to reduce the amount of ZnSe grains at the back contact, as discussed above. The depostion at low temperatures is carried out for 5 minutes before the heater temperature is increased to 500 °C. The substrate temperature measured by the pyrometer is not constant during the deposition and may vary for example due to changes in secondary phases [99]. The measured temperature by the pyrometer levels off at around 470 °C, which is the referred value of the growth process.

After a deposition time of 45 minutes at a heater temperature of 500 °C, the Cu and the Zn shutter are closed and the sample is annealed in a Sn, SnSe and Se flux/atmosphere for

[1] Remember that the high temperature annealing is carried out at 520 °C.

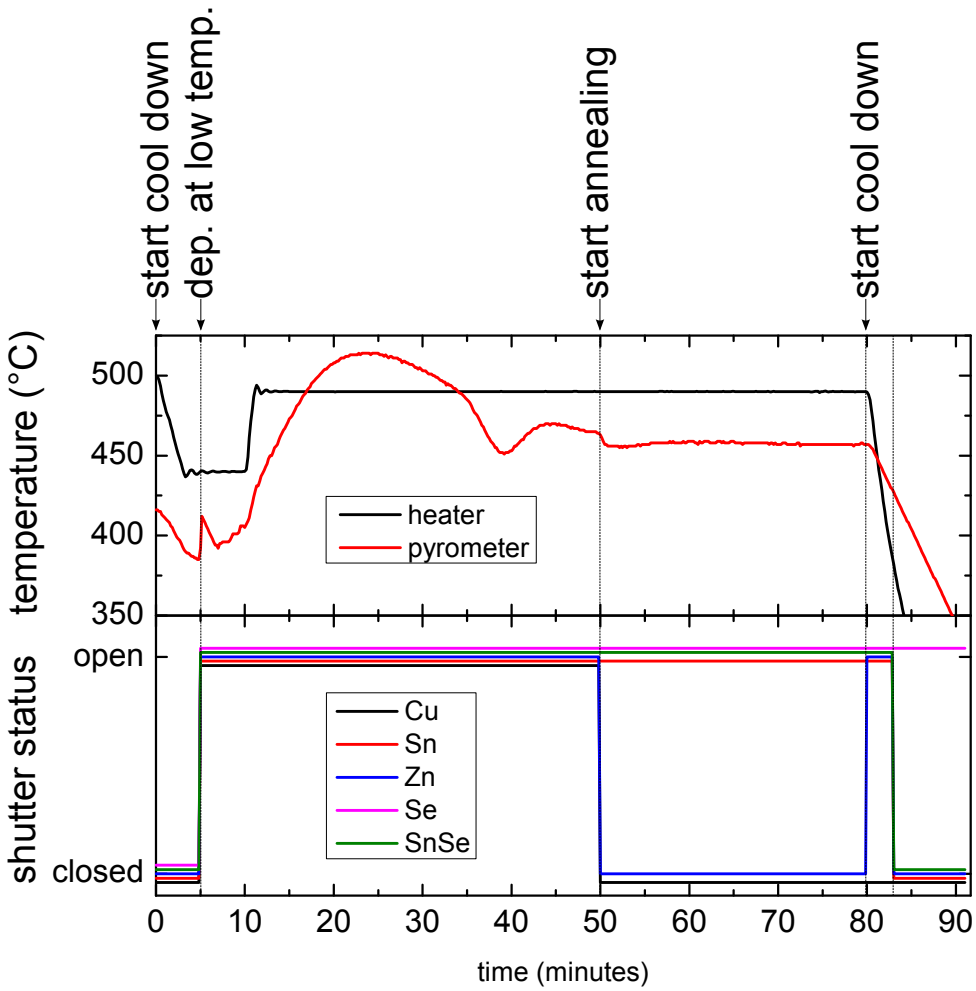


Figure 3.5.: ***Growth process by co-evaporation at high temperatures*** *- The process can be devided into a growth section (5 minutes - 50 minutes) and an annealing section (50 minutes - 80 minutes). At the beginning of the process, the substrate temperatures is lowered to reduce the formation of ZnSe at the back contact [89]. During the first 3 minutes of the cooldown, the Zn shutter is opend in order to induce a Zn-rich surface [100].*

30 minutes. The sample is cooled to 200 °C after the annealing step. In the first 3 minutes of the cooldown, Zn, Sn, SnSe and Se is supplied. Zn is needed to induce a Zn-rich cap. Repins *et al.* reported that a Zn-rich cap in combination with an air annealing increases the device efficiency [99]. However, the solar cells ended up dead if the absorber layer grown according to the process shown in Fig. (3.5) was air annealed. Still, a Zn-rich cap can favour the formation of ZnSe over SnSe or Cu_xSe_y, which are much more detrimental to solar cell performance [98]. The further cool down in Sn, SnSe and Se atmosphere prevents the decomposition reaction at high temperatures (see section 3.2.1). It was shown by Bishop *et al.* that if the surface is not stabilized during cool, the solar cell efficiency decreases significantly.

The behaviour of the pyrometer was not discussed in literature extensively. Redinger *et al.* interpreted the broad oscillations in terms of interference fringes [19] based on the examination of the *in-situ* laser light scattering signal in Ref. [73]. Mise *et al.* interpreted the first strong rise of the pyrometer signal by an increased emissivity at 2000 nm in the early stage of the deposition. The transition from the minimum around 40 minutes to the subsequent plateau between 45 minutes to 50 minutes was interpreted as the transition from a Cu-rich to a Cu-poor film. As the fluxes in the process shown in Fig. (3.5) were set constant during growth and no intentional Cu-rich step was included, the Cu-rich to Cu-poor transition in the pyrometer could be the point were all the initial formed Cu_xSe_y is consumed. The drop of the pyrometer signal at 50 minutes is linked to the closing of the Cu shutter. The Cu-tip is operated around 1300 °C such that a substantial heating occurs from that source alone leading to an apparent temperature drop after closing the Cu-shutter. An additional loss of reflected infra-red light from the source could also lead to a drop in the pyrometer signal.

3.3.2.1. Mutli-stage process

A variation of the process described above (section 3.3.2) is the so-called *multi-stage process* [19]. The rather long deposition (45 mins) and annealing (30 mins) period shown in Fig. (3.5) is chucked into several shorter periods of deposition and annealing. A motivation of this process variation is that a higher quality material is formed right away.

However, solar cell devices generally did not show an improved efficiency. Also the capacitance spectra were similar as mentioned in section 5.6.1. Thus, for most of the devices presented here, the more simple process depicted in Fig. (3.5) was applied for the growth of the absorber layer.

3.3.3. Additional heat treatment

Additional to the high temperature co-evaporation process a heat treatment can be applied to the absorber layers. Two different heat treatments were carried out from which finished solar cell devices were characterized by IVT (section 6.3.2) and admittance (section 5.6.2) measurements.

low temperature heat treament This treatment includes an annealing at 180 °C in the PVD chamber, i.e. in vacuum with a base pressure of approximately $1 \cdot 10^{-8}$ torr. The temperature is slightly below the critical temperature of the order-disorder transition of 200 °C and thus, a bit of ordering is expected after the heat treatment.

high temperature annealing The high temperature annealing process for the high temperature co-evaporated absorber layers is the same as for the sequential process described in

section 3.2.4. A motivation for an additional high temperature annealing in a Se and SnSe atmosphere is to provide a high Se and SnSe partial pressure at high temperatures, which is not possible in the PVD chamber. Shin *et al.* [83] showed that if the Se partial pressure during annealing is not high enough, PL peaks below the bandgap arise, which might be defect related.

3.4. CdS thickness variation

As described in section 2.2.1, the solar cell structure includes a CdS buffer layer with a nominal thickness of 50 nm. As will be shown in section 6.3.1.1 and section 5.7.2, insights about recombination processes and barriers within the heterojunction can be obtained by investigating samples with different CdS buffer layer thicknesses. Different CdS buffer layer thicknesses were deposited on absorbers from one co-evaporation process. It needs to be emphasized that all absorbers came from the same deposition run and are therefore identical except the CdS buffer layer. Also the window layer (i:ZnO/Al:ZnO bilayer) and the Ni/Al grid was processed for all these samples in the same run.

3.4.1. Absorber growth

The samples were grown by the standard co-evaporation process described in section 3.3.2. An additional low temperature heat treatment was applied inside the MBE chamber directly after the growth process, i.e. without any air exposure in between. As I will show in section 6.3.2 and have published in Ref. [41] such a heat treatment reduces the doping density significantly and a double capacitance step gets more pronounced[2]. A clear double capacitance step facilitates the evaluation of the admittance data and therefore allows for interpretation of the admittance data based on different CdS buffer layer thicknesses (see section 5.7.2). Additionally, the liquid N_2 cooling of the chamber was maintained throughout the low temperature heat treatment in order to prevent any desorption of elements from the chamber walls onto the absorbers.

3.4.2. CdS growth

The CdS buffer layer is grown by a chemical bath deposition process following Contreras *et al.* [101]. The deposition of CdS onto the absorber starts as soon as the Thiourea ($(NH_2)_2CS$) is added into the solution of cadmium sulfate ($CdSO_4$) and ammonia (NH_3). From this point on the deposition of CdS takes around 4:40 minutes to obtain a roughly 50 nm thick CdS buffer layer. This procedure with a deposition time of 4:40 (280 s) minutes is in the following referred to "1.0 CdS runs".

The growth of CdS is generally not constant with respect to time. In order to check the deposition rate, CdS was grown on CZTSe absorbers for different time periods between 70 and 280 s. The amount of CdS was then evaluated by EDX measurements. The result is shown in Fig. (3.6) from which it is concluded that the growth rate within this time interval is approximately constant.

[2]However, the reduction of the effective doping density was not observed to be as strong as for the samples with air exposure between growth and additional heat treatment

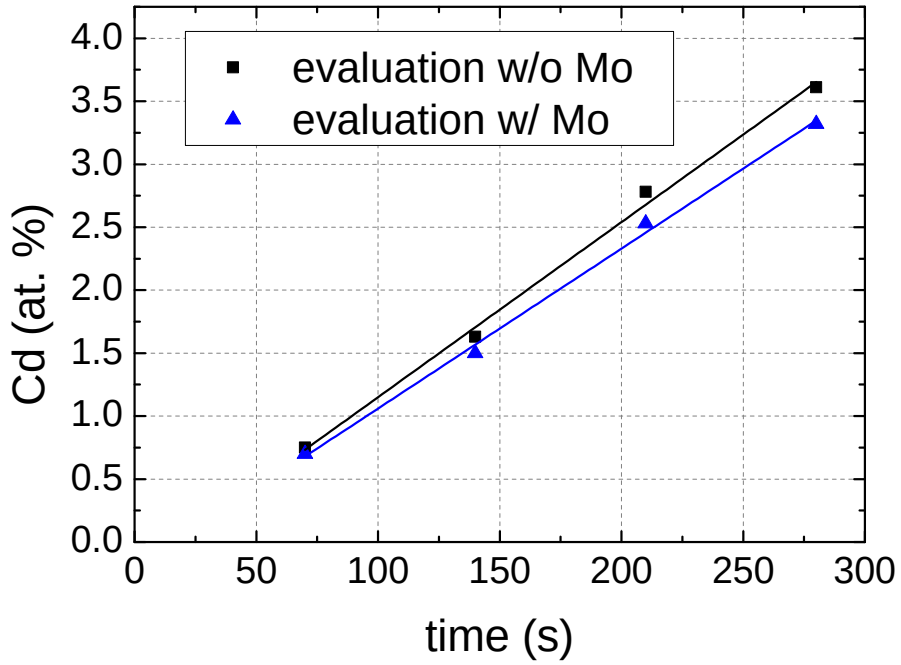


Figure 3.6.: ***Evaluation of the CdS thickness by EDX*** *- Amount of at. % of Cd in the film is evaluated with EDX measurements. As the CdS layer is grown onto CZTSe, the evaluated elements are Cu, Zn, Sn, Se, Cd and Mo (blue triangles). Black circles show the result when the Mo peak is not taken into account for the EDX evaluation. An approximately linear deposition rate with respect to time can be inferred.*

Four solar cells were then prepared with CdS buffer layer thicknesses grown by 0.5, 1.0, 1.5 and 2.0 CdS runs spanning a nominally buffer layer thickness between 25 nm and 100 nm. An overview of these devices can be found in section E.1.

3.5. Differences in microstructure

In this section I want to point out the micro structural differences from the different growth techniques, which are seen by electron microscopy. Fig. (3.7) shows four polished SEM cross section: an annealed low temperature precursor (a), an annealed 320 °C grown precursor (b), an high temperature co-evaporated absorber (c) and an annealed high temperature co-evaporated absorber (d). The white patches were identified by EDX mappings to be ZnSe. Sample (c) shows these ZnSe grains at the back contact in agreement with the discussion in section 3.3.1. Sample (d) shows that an annealing of a high temperature co-evaporated absorber does not lead to additional formation of ZnSe in the bulk of the absorber as it is seen in samples (a) and (b). Bishop *et al.* [96] grew absorber layers by co-evaporation as well, but with a different process: the first stage was set to 300 °C for 120 minutes. The second stage was at 500 °C for 15 minutes. This process resembles basically a sequential process. Polished cross sectional SEM images show similar ZnSe inclusions as shown in Fig. (3.7b).

A detailed study on the precursors grown at low temperatures can be found in the Masterthesis of M. Spies [102].

Hence, based on the images of the samples (a), (b) and (d) (and Ref. [96]) it can be concluded that the formation of ZnSe is due to the different growth processes of the precursor. For the co-evaporated absorbers discussed here, Redinger *et al.* [19] showed that the CZTSe grains are stoichiometric in the [Zn]/[Sn] ratio. Also Brammertz *et al.* [64] and Todorov *et al.* [103] found an average composition of [Zn]/[Sn] = 1 for a 9.7 % and a 11.1 % efficient device, respectively. This leads to the assumption that the excess Zn in the precursors segregates in the form of ZnSe during the annealing process. As ZnSe is the least detrimental secondary phase for kesterite based solar cells [51, 98], many groups grow Zn-rich absorber layers, i.e. [Zn]/[Sn] > 1.

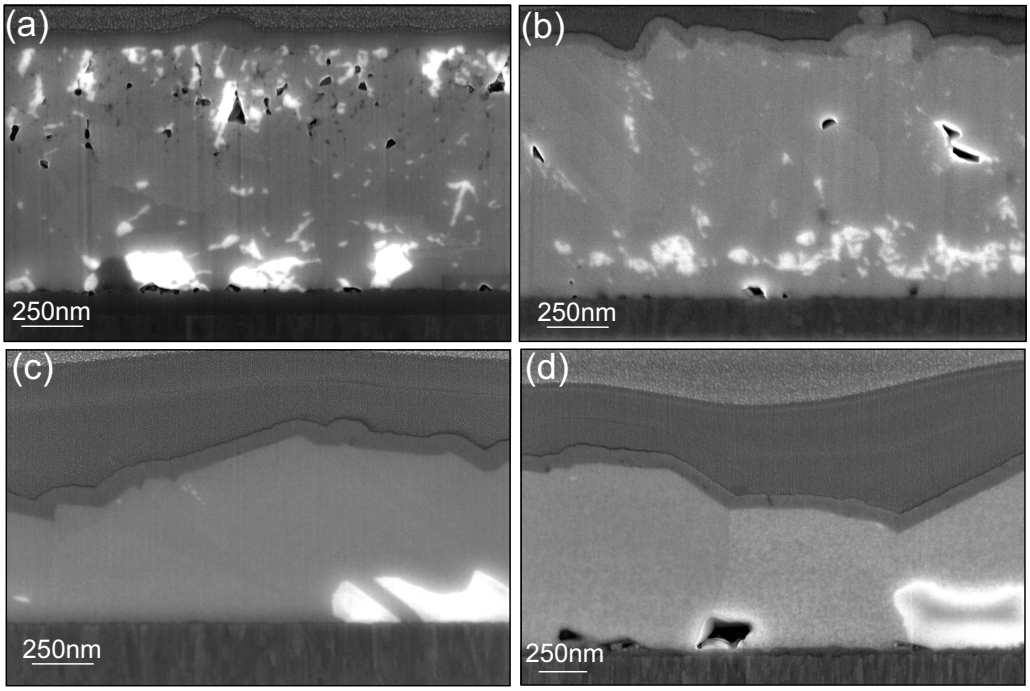


Figure 3.7.: ***Micro structural differences due to different absorber growth processes*** *- SEM cross sections of an annealed low temperature precursor (a), an annealed* $320\,^{\circ}\mathrm{C}$ *grown precursor (b), an high temperature co-evaporated absorber (c) and an annealed high temperature co-evaporated absorber (d).*

CHAPTER

FOUR

EXPERIMENTAL SETUP

Fig. (4.1) shows the experimental setup, which is used for capacitance and IVT measurements. To switch between these two types of measurements, only the cables at the contacts need to be changed to connect either to a LCR meter (capacitance measurements) or to a Keithley (IVT measurements).

The coldfinger of the cryostat is located inside the *sample chamber*, which allows for temperature variations. The *cryo generator* is located at the bottom of Fig. (4.1). The compressor for the *cryo generator* is situated below the table and is not shown in the picture. In order to prevent condensation of water/ice at low temperatures, the sample is kept in vacuum. For that purpose the *sample chamber* is connected to a turbo molecular pump via the flexible tube annotated with *pumping*.

For capacitance and IVT measurements without illumination the *sample chamber* is cloaked from the top as well as from the side windows. For illuminated IVT measurements only the side windows are cloaked in order to minimize unintentional background illumination. On top of the setup a *halogen lamp* is fixed as the illumination source. A fan is mounted on top of the halogen lamp for cooling purposes. The *shutter* is opened during the acquisition of the IV curve, while it is closed during the time of temperature equilibration in order to prevent heating effects due to the illumination. A *filter wheel* can be placed directly on top of the *sample chamber* to adjust for six different illumination intensities. The attenuation of the illumination is achieved with neutral density filters. The transmittance of these filters is 54 %, 66 %, 84 % and 93 %. A metal plate and no filter at all is used for 0 % and 100 % transmittance, respectively.

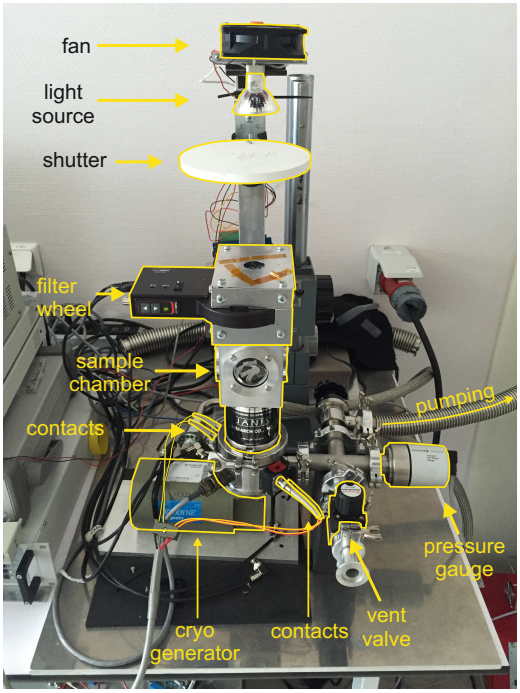


Figure 4.1.: ***Experimental setup*** *- All capacitance and IVT measurements are performed in this setup. At the contacts the cables can be changed to switch between a LCR meter (capacitance measurements) and a Keithley (IVT measurements) as the measuring unit.*

4.1. Temperature control

The temperature is controlled with a *JANIS closed cycle refrigerator*. For the measurement the temperature control was set to the cold finger of the cryostat on which the sample was mounted (sensor A). However, this temperature does not reflect the real temperature of the absorber as the sample is grown either on a 2 or 3 mm glass substrate. Additionally, the sample was glued onto a 3 mm thick aluminium plate, which serves as the sample holder. To get a better estimate of the temperature on top of the glass substrate, a *Lakeshore DT-670* temperature sensor was glued onto a glass substrate next to the sample under test (sensor B). A typical temperature curve measured on top of a 2 mm (red triangles) and a 3 mm (green circles) glass substrate is shown in Fig. (4.2). As the temperature controller regulates with respect to the sensor of the cold finger it is obvious that the temperatures of sensor A are the same as the setpoint. However, the temperature measured by sensor B, glued on top of the glass substrate, deviates from the straight line at low temperatures, which is more pronounced for the 3 mm glass substrate than for the 2 mm glass substrate.

In general, the temperature was varied between 320 K and 20 K in steps of 10 K (sensor A). However, not all the samples were measured on the complete temperature range, but in a reduced range, generally starting from 300 K down to 40 K, with the same step size. As soon as the temperature sensor A reached its setpoint within an accuracy of 1 K, an additional wait time of 300 s was introduced to equilibrate also the temperature of the absorber, i.e. the temperature of sensor B.

For some IVT and admittance measurements, the sensor B was not removed and re-glued prior to the measurements. As a consequence, the sensor B became a bit loose and the reading of the sensor was overestimated at low temperatures since the thermal contact was diminished.

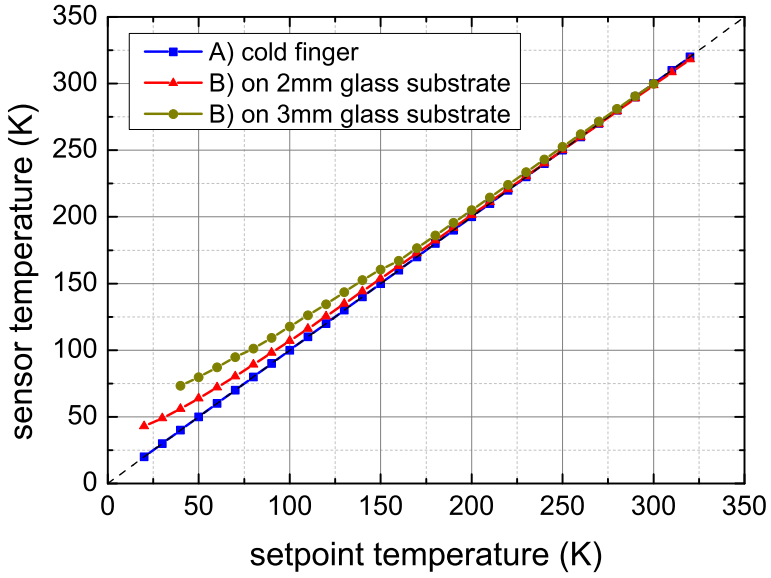


Figure 4.2.: ***Temperature curve of the cold finger sensor A) and on top of a glass substrate (sensor B)*** *- Temperatures were measured on top of a 2 mm (red triangles) and on a 3 mm (green circles) glass substrate. The glass substrate was glued on a 3 mm thick Al plate, representing the sample holder. The additional waittime for the equilibration of sensor B was set to 300 s.*

However, the sample itself was glued correctly prior to each measurement and thus it can be assumed that the temperature of the absorber yields a value for a good (not loose) thermal contact. In order to evaluate the measurements of these samples with the correct temperature, a temperature calibration curve was recorded and fitted with a quadratic polynomial. The temperature of the absorber was then estimated from the fitted calibration curve. This procedure was employed for the CAPRI samples. For the co-evaporated samples, which were measured in a later stage of my thesis, this problem was already known and the sensor B was always re-glued at the same time as the sample under test was glued to the sample holder. For these samples the temperature of the absorber was taken from the reading of sensor B.

4.2. Capacitance measurements

For the measurement of the capacitance with respect to voltage and frequency an *Agilent E4980A Percision LCR Meter* is used.

Admittance measurements were performed under zero bias voltage in a frequency range between 100 Hz and 1 MHz in equidistant steps on a logarithmic scale. A modulation voltage amplitued of 30 mV was used. It is know from CIGSe that light or voltage soaking can change the state of the sample due to metastabilities [104, 105]. The sample was therefore left in the dark at 300 K over night (at least 10 h) prior to an admittance measurement in order to put the sample into an equilibrium state. However, detailed experiments about metastabilities were not carried out and according to my knowledge were also not reported in literature.

For CV measurements, the voltage was initially swept from reversed to forward bias with a waittime after each voltage adjustment of 4 s. This procedure was applied for the CAPRI samples. The co-evaporated samples (later stage of my thesis) were measured from forward to reversed bias. The reason is that a reversed bias soaking can influence the state of the

sample and with that the capacitance measurement [106, 107]. For a few samples a difference between these two measurement directions was observed, while some other samples did not show a dependence on the sweeping direction. However, the determined carrier density was not influenced by this sweeping direction of the voltage.

The applied bias voltage in forward bias is limited by the maximal specified current of the LCR meter, which is 100 mA. Thus, the measurement is disturbed at a certain forward biased voltage, as the current increases exponentially with forward bias according to the diode equation (see Eqn. (2.12)). At lowered temperatures, the maximal value for the forward bias voltage can be increased due to the thermal activation of J_0. Therefore, the onset of the dominating exponential term in Eqn. (2.12) is shifted to higher forward voltages.

4.3. IVT measurements

Current voltage data is recorded with a *Keithley 2440 5A SourceMeter*. The voltage is swept from reversed bias to forward bias in steps of 10 mV. After the adjustment of the voltage a waitime of 25 ms was applied. The waittime is kept small in order to minimize heating effects due to the illumination during the acquisition of the IV curve. For illumination dependent IV measurements the filter wheel is used as described in section 4. The filter wheel is controlled to measure from low light intensities to full illumination. For full illumination intensity the distance of the halogen lamp to the sample was adjusted such that the same J_{sc} value is obtained as for a calibrated IV measurement (c.f. section 4.4). After each measurement at a certain illumination intensity, a waittime of 60 s was applied in order to equilibrate the temperature due to the heating of the light source. If this waittime is not added, the plot of V_{oc} versus J_{sc} is bent in a sense that the V_{oc} for high J_{sc} values (high intensity) is smaller than expected. A reason might be the increased temperature due to heating during the measurements.

4.4. IV measurements

IV measurements at room temperature were carried out in a separate setup than the one described in Fig. (4.1). A cold mirror halogen lamp is used as an illumination source. The light intensity is calibrated to 100 mW/cm^2 with a reference silicon solar cell. The reported efficiencies of solar cell devices in this thesis are measured in the IV setup (and not in the IVT setup).

CHAPTER

FIVE

CHARACTERIZATION BY CAPACITANCE MEASUREMENTS

The admittance is defined as the complex conductance of a circuit as in $UY = I$ and can be written as [29]

$$Y = G + iS = G + i\omega C. \tag{5.1}$$

I and U are the current and the voltage, respectively. The real part of the admittance in Eqn. (5.1) is the conductance G and the imaginary part the susceptance $S = \omega C$. ω is the angular frequency of an external ac voltage applied to the circuit.

The capacitance (per unit area) is defined as the change of charge (per unit area) by a change of applied voltage according to

$$C = \frac{\mathrm{d}Q}{\mathrm{d}V} \tag{5.2}$$

For a n^+p junction without deep defects the charge is modulated in the n^+ layer very close to the hetero interface and in the p layer at the SCR edge. These two modulations can be considered as two capacitors in series, as [108]

$$C^n_{SCR} = \frac{\Delta Q}{x_n} \tag{5.3}$$

$$C^p_{SCR} = \frac{\Delta Q}{x_p}. \tag{5.4}$$

As $N_D \gg N_A$ it holds that $x_n \ll x_p$ (see section 2.1) and therefore the resulting SCR capacitance of the series connection is dominated by the lower one, such that it holds: $C_{SCR} \cong C^p_{SCR}$. Thus, Eqn. (5.2) can be written as

$$C_{SCR} = \frac{qN_A\mathrm{d}x_p}{\mathrm{d}V} = \frac{\epsilon_R\epsilon_0}{x_p} = \sqrt{\frac{q\epsilon_R\epsilon_0 N_A}{2}}\left(V - \frac{2kT}{q}\right)^{-1/2}, \tag{5.5}$$

where Eqn. (2.10) is used for the width of the SCR on the p side and $\mathrm{d}Q = qN_A\mathrm{d}x_p$. ϵ_R denotes the dielectric constant of the absorber and V the total potential drop across the junction with $V = V_{bi} - V_b$, with V_b the applied bias voltage. Not that V_{bi} is positive in this notation and V_b is positive for forward bias voltages. The term $2kT/q$, which is not included in Eqn. (2.10),

describes the deviation from the depletion approximation, since in general the space charge distribution is not a step function but thermally smeared out at the edges.

5.1. Capacitance voltage measurements

As shown in Eqn. (5.5) the capacitance has a voltage dependence. We can rewrite this formula to obtain the so called Mott-Schottky representation as [44]

$$\frac{1}{C_{SCR}^2} = \frac{2}{q\epsilon_R N_A}\left(V - \frac{2kT}{q}\right) \approx \frac{2}{q\epsilon_R N_A}\left(V_{bi} - V_b\right). \tag{5.6}$$

The term of $2kT/q$ has been neglected as the built-in voltage and the bias voltage in general are much bigger than the thermal voltage. From Eqn. (5.6) it follows that the Mott-Schottky plot. intersects the abscissa at V_{bi} and has a slope $\propto N_A^{-1}$. However, it has to be noted that Eqn. (5.6) is only valid if no deep defects contribute to the capacitance. Deep defects can contribute to the measurement of the capacitance if the following two requirements are met:

1. The deep defect has to cross the Fermi level (within the SCR). If the deep defect does not cross the Fermi level, the occupation of that defect is either filled or empty of carriers and the charge state cannot be changed by applying a small external test voltage. Thus, the deep defect level does not contribute to the capacitance. On the other hand, at the position where the deep defect crosses the Fermi level the charge state can be changed with a small externally applied test voltage. Hence, at this position, the deep defect adds to the capacitance [109].

2. The time constant for trapping and detrapping of carriers needs to be smaller than the time constant of the ac voltage change. Only with that condition the charging and discharging of the trap state can follow the applied ac bias voltage and thus contributes to the capacitance [23,29]. The frequency dependence of the capacitance will be discussed in section 5.2. In the following it is assumed that for high (enough) frequencies the trap state do not contribute to the capacitance anymore.

The space charge distribution ρ with the corresponding band diagram for a Schottky contact including an acceptor like deep defect level with density N_t is shown in Fig. (5.1). The deep defect intersects the Fermi level at x_t and thus for $x < x_t$ the deep defect is occupied by electrons, i.e. empty of holes, and thus adds to the space charge distribution and $\rho = -(N_A + N_t)$. For $x > x_t$ the deep defect is neutral and only the doping acceptor contributes to the space charge; thus $\rho = -N_A$. In the QNR the space charge is neutral as the density of the free holes equals the density of the (negatively charged) doping acceptors.

Therefore, in the presence of deep defects, charge is not only modulated at x_p but also at x_t due to the deep defects. As a consequence Eqn. (5.6) cannot straight forwardly be applied. However, dependent on the applied voltage, it is still possible to make estimates of the doping density. For that we first define the distance $\lambda = x_p - x_t$ (see Fig. (5.1)), which is specific for the trap and independent of bias voltage. Assuming parabolic band bending λ is given by [29]:

$$\lambda = x_p - x_t = \left(\frac{2\epsilon_0\epsilon_R}{e^2 N_A}(E_F - E_t)\right)^{1/2}. \tag{5.7}$$

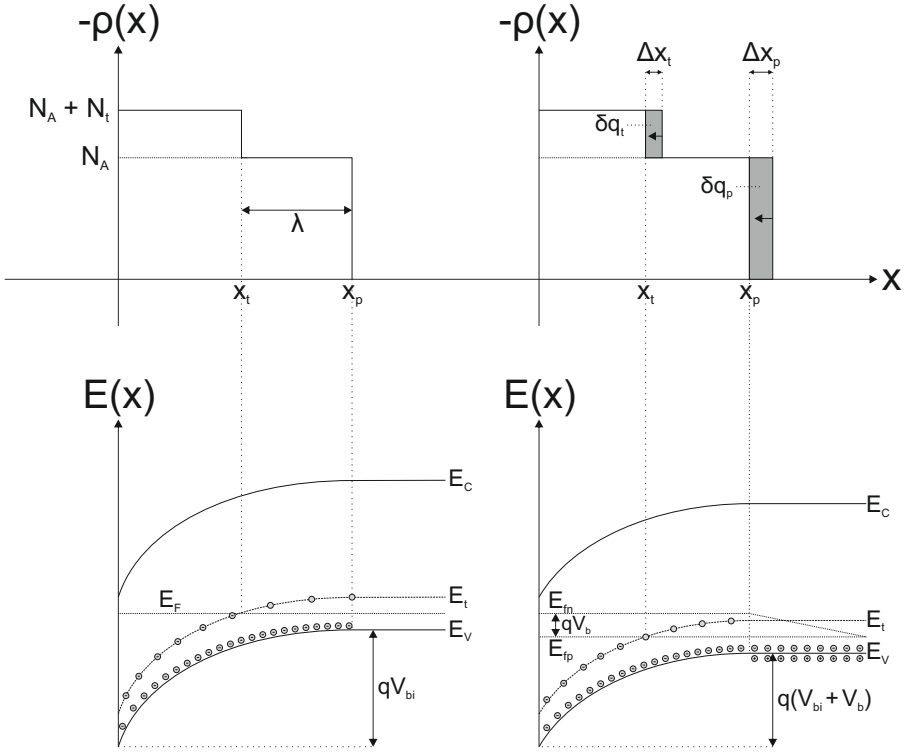


Figure 5.1.: ***Schematic of space charge distribution and trap occupancy*** *- Space charge distribution and band diagram with one acceptor like deep defect depicted without (left) and with (right) applied forward bias voltage. Image adapted from [29].*

As λ is independent of voltage it also holds that $\Delta x_t = \Delta x_p$ (c.f. Fig. (5.1)).

For far *reversed* bias it is $\lambda \ll x_p$ and hence $x_t \approx x_p$. Thus, the position of charge modulation can be approximated to be at x_p with a charge density of $\rho = N_A + N_t$. Therefore, the evaluated doping density according to Eqn. (5.6) gives $N_A + N_t$ [29]. However, as modelled in [61] the measured density ρ converges only slowly to the value of $N_A + N_t$ with applied reversed bias and is probably not probed in the experiments presented in this thesis.

When going into *forward* bias the position of x_t shifts closer to the interface. If $x_p < \lambda$ the deep defect does not intersect the Fermi level anymore and thus does not contribute to the capacitance. In that case the evaluated doping density according to Eqn. (5.6) gives N_A - the true doping density.

For bias voltages between these two conditions no meaningful doping density can be evaluated. This is even the case when choosing a test frequency, which the deep defects cannot follow. As the sweep rate of the bias voltage V_b is very low the deep defects can follow this voltage change. Consequently, the space charge distribution is influenced by the deep defects and Eqn. (5.6) is not valid. To measure the true doping density N_A for all bias voltages, a sweep rate of the bias voltage V_b must be chosen, which exceeds the time constant of the deep defect, as explained for instance in Ref. [110].

5.1.1. Determination of V_{bi} and N_A

In this work I used a slow sweep rate of the bias voltage V_b and therefore, the true doping density and built-in voltage can only be obtained in forward bias measurements and is exemplified in

Fig. (5.2). To obtain the doping density and the built-in voltage experimentally the datapoints forming a straight line in forward bias are fitted linearly with Eqn. (5.6). The doping density is obtained from the slope m as

$$m = \frac{2}{q\epsilon_R\epsilon_0 N_A}, \tag{5.8}$$

while the intercept with the abscissa yields the built-in voltage. If not stated otherwise, ϵ_R is assumed to be 10 for the calculations in this thesis.

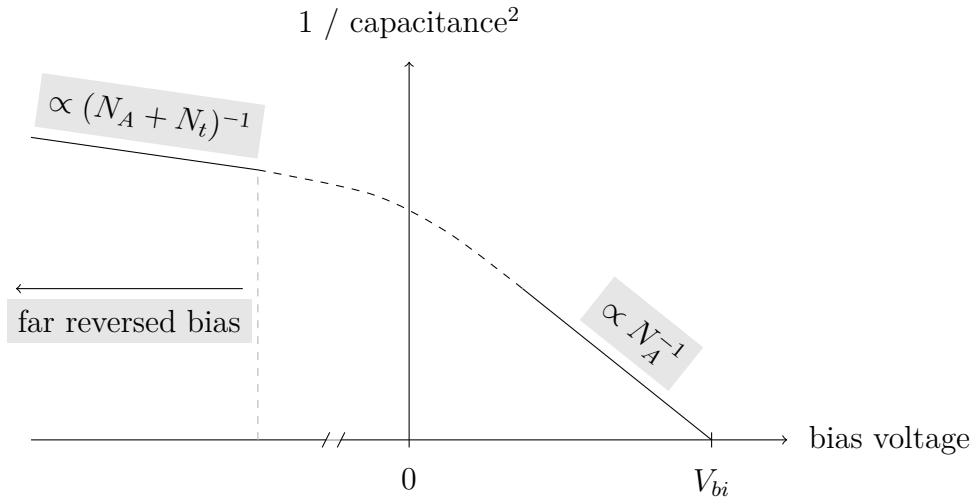


Figure 5.2.: ***Theoretical behaviour of the Mott-Schottky plot with deep defects*** *- The sweep rate of the bias voltage is small so that it is assumed that the deep defects are in equilibrium with the bias voltage. In forward bias the deep defects do not cross the Fermi level anymore and therefore the true doping density N_A is measured. For far reversed bias voltages a defect density of $N_A + N_t$ is measured. Image adapted from [29].*

5.1.2. Influence of deep defects on the built-in voltage

If deep defects are also included into the capacitance measurement not only a wrong doping density is deduced but also a too small built-in voltage is deduced.

In general the capacitance can be expressed as [29, 61]

$$C = \frac{\epsilon_R\epsilon_0 \int_0^\infty \mathrm{d}x\ \delta\rho(x)}{\int_0^\infty \mathrm{d}x\ x\delta\rho(x)} = \frac{\epsilon_R\epsilon_0}{\langle x\rangle}, \tag{5.9}$$

where $\langle x\rangle$ is the first moment of charge response [61]. We assume charge modulation at x_t by Δq_t due to deep defects and at x_p by Δq_p due to the doping defect. Thus, $\delta\rho(x)$ can be written as

$$\delta\rho(x) = \delta(x - x_t)\,\Delta q_t + \delta(x - x_p)\,\Delta q_p \tag{5.10}$$

$$= \delta(x - x_t)\,N_t\Delta x + \delta(x - x_p)\,N_A\Delta x. \tag{5.11}$$

$\delta(x)$ is the Dirac delta function. It is assumed that all the deep defects respond and therefore $\Delta q_t = N_t \Delta x$. Inserting Eqn. (5.11) into Eqn. (5.9) yields a capacitance value including deep defects of

$$C_{dd} = \epsilon_R \epsilon_0 \frac{N_t + N_A}{N_t x_t + N_A x_p}. \tag{5.12}$$

In the case where no deep defects contribute, this expression reduces to

$$C_{SCR} = \frac{\epsilon_R \epsilon_0}{x_p}. \tag{5.13}$$

Note that $C_{dd} > C_{SCR}$ via

$$\frac{N_t + N_A}{N_t x_t + N_A x_p} > \frac{N_t + N_A}{N_t x_p + N_A x_p} = \frac{1}{x_p}. \tag{5.14}$$

Thus, in the presence of deep defects a shift in the Mott-Schottky plot is observed which amounts to

$$\Delta \frac{1}{C^2} = \frac{1}{C_{dd}^2} - \frac{1}{C_{SCR}^2} = \frac{1}{(\epsilon_R \epsilon_0)^2} \left[\left(\frac{N_t(x_p - \lambda) + N_A x_p}{N_t + N_A} \right)^2 - x_p^2 \right] < 0. \tag{5.15}$$

As it was shown in Ref. [61], for low frequency conditions the deep defect can follow the modulation frequency and the measured doping density is $N_A + N_t$. Thus, the Mott-Schottky plot has a slope of $2/(\epsilon_R \epsilon_0 q(N_A + N_t))$. As the consequence, due to the shift of $\Delta 1/C^2$ a shift in the built-in voltage of

$$\Delta V_{bi} = \Delta \frac{1}{C^2} \frac{\epsilon_R \epsilon_0 q(N_A + N_t)}{2} = \frac{q}{2\epsilon_R \epsilon_0} \left[\frac{(N_t(x_p - \lambda) + N_A x_p)^2}{N_A + N_t} - (N_A + N_t) x_p^2 \right] \tag{5.16}$$

is observed. For $N_A \gg N_t$, Eqn. (5.16) equals zero as it would be expected. However, taking for example $N_A = N_t$, $\lambda = x_p/2$, Eqn. (5.16) will result in a shift of V_{bi} of

$$\Delta V_{bi} = \frac{q}{2\epsilon_R \epsilon_0} \left[\frac{9 N_A x_p^2}{8} - 2 N_A x_p^2 \right] = -\frac{7 q N_A x_p^2}{16 \epsilon_R \epsilon_0}. \tag{5.17}$$

For $N_A = 1e16\,\mathrm{cm}^{-3}$, $x_p = 200\,\mathrm{nm}$ and $\epsilon_R = 10$, this amounts to lowered measured built-in voltage of $\Delta V_{bi} \approx -320\,\mathrm{mV}$.

5.2. Admittance spectroscopy

In section 5.1 the voltage dependence of the capacitance was described. However, in the presence of deep defects, the capacitance has also a frequency dependence, which is topic of this section. It was already mentioned in section 5.1 that the charging and discharging of the defect states cannot follow the modulation of the free carriers if the frequency of the test voltage is high enough. Thus, a (smooth) capacitance step occurs when going from low to high frequencies. By measuring this capacitance step with respect to the temperature, several defect parameters can be deduced as for instance the defect energy and the defect density.

The following derivation of the frequency dependence is adapted from Ref. [29] and is shortly sketched here. As mentioned in section 5 the admittance is measured by measuring the complex current of the device by applying a small ac test voltage. The test voltage is modulated with frequency ω, such that $u(t) = u_0 \exp(i\omega t)$. As depicted in Fig. (5.1) the charge is modulated at x_p due to the change in SCR width and at x_t due to the change of charge state of the deep defects. Thus, the current can be written as

$$i(t) = \frac{\mathrm{d}}{\mathrm{d}t}\delta q_p(t) + \frac{\mathrm{d}}{\mathrm{d}t}\delta q_t(t), \tag{5.18}$$

where δq_p and δq_t is the change of charge at x_p and x_t, respectively. Assuming that the shallow acceptors respond instantaneously to the external modulation and thus to the modulation in depletion depth, $\delta q_p(t)$ can be written as

$$\delta q_p(t) = eN_A(x_p)\Delta x_p(t). \tag{5.19}$$

$\delta q_t(t)$ can in general be written as

$$\delta q_t(t) = e\int_0^{x_p} \mathrm{d}x \delta n_t(x,t), \tag{5.20}$$

where $\delta n_t(x,t)$ is the change of the occupation of a deep acceptor state. This change of $\delta n_t(x,t)$ is given by the rate equations and can be written as

$$\frac{\partial}{\partial t}\delta n_t(x,t) = c_p p(x,t)\left[N_t - n_t(x,t)\right] - e_p n_t(x,t), \tag{5.21}$$

where $c_p p(x,t)$ and e_p is the capture and emission coefficient of holes from the defect state. $n_t(x,t)$ denotes the density of defect states occupied by a hole. Making use of the steady state conditions when no modulating voltage is applied, Eqn. (5.21) can be written as

$$\frac{\partial}{\partial t}\delta n_t(x,t) = -f_0(x)\delta n_t(x,t) + c_p\left[N_t - n_{t0}(x)\right]\delta p(x,t) \tag{5.22}$$

with $f_0 = c_p p_0(x) + e_p$. $\delta p(x,t)$ denotes the change of the free holes due to the external voltage modulation. Eqn. (5.22) gives the occupancy of the defects and contains two terms. The first term is the relaxation of the defect back to its steady state with the time constant f_0. The second term, proportional to $\delta p(x,t)$ can be identified as the driving modulation of the free hole tail. The local variation of $\delta p(x,t)$ can be expressed as

$$\delta p(x,t) = p_0(x)\frac{ev(x,t)}{kT}, \tag{5.23}$$

which is valid for $ev(x,t) \ll kT$, where $v(x,t)$ is the local change of potential. Using Poisson's equation (see Eqn. (2.4)), $v(x,t)$ can be expressed as

$$v(x,t) = \frac{1}{\epsilon_R\epsilon_0}\frac{(x_p - x)}{x_p}\left[\epsilon_R\epsilon_0 v(t) - \bar{x_t}\delta q_t(t)\right] + v_t(x,t). \tag{5.24}$$

$v(t)$ is the external modulation voltage and $v_t(x,t)$ the change of potential due to $\delta n_t(x,t)$ and $\bar{x_t}$ the mean distance of charge modulation at the defect site due to $\delta n_t(x,t)$. In order to solve Eqn. (5.22) analytically, the following assumptions need to be made:

1. The mean distance $\bar{x}_t$ of the charging and discharging is independent of time. As $\bar{x}_t \gg \Delta x$ the modulation of charge only occurs in a small region around the point where the Fermi level intersects the defect level, which allows of doing this assumption.

2. $p(x)$ is uniform over $[\bar{x}_t, \bar{x}_t + \Delta x]$, where $p(x)$ is the free hole concentration. With that assumption the time constant of the trap f_0 is the same for all and reads $f_0 = 2e_p$.

3. The potential drop due to $\delta n_t(x,t)$ at $\bar{x}_t$ will be neglected.

With these assumptions Eqn. (5.24) can be written as

$$v(x,t) = \frac{1}{\epsilon_R \epsilon_0} \frac{(x_p - x)}{x_p} \left[\epsilon_R \epsilon_0 v(t) - \bar{x}_t \delta q_t(t)\right] + \Theta(\bar{x}_t - x) \frac{q}{\epsilon_R \epsilon_0} \delta q_t(x - \bar{x}_t), \tag{5.25}$$

where $\Theta(x)$ is the Heaviside step function. $v(x,t)$ is plotted in Fig. (5.3) with (solid red curve) and without (dashed red curve) a contribution of deep defects at $\bar{x}_t$ according to Eqn. (5.25). The potential drop determines the band bending, which is also depicted for a Schottky type contact in Fig. (5.3). The blue curve depicts the band bending in steady state conditions[1] and the green curves with a small voltage $v(t)$. Dependent on whether the deep defects follow the voltage change $v(t)$ the band bending changes and thus also the carrier concentration $p(\bar{x}_t, t)$. This issue is known as the coupling of the deep defects with the free holes, which has an impact on the defect response to an ac voltage modulation [109].

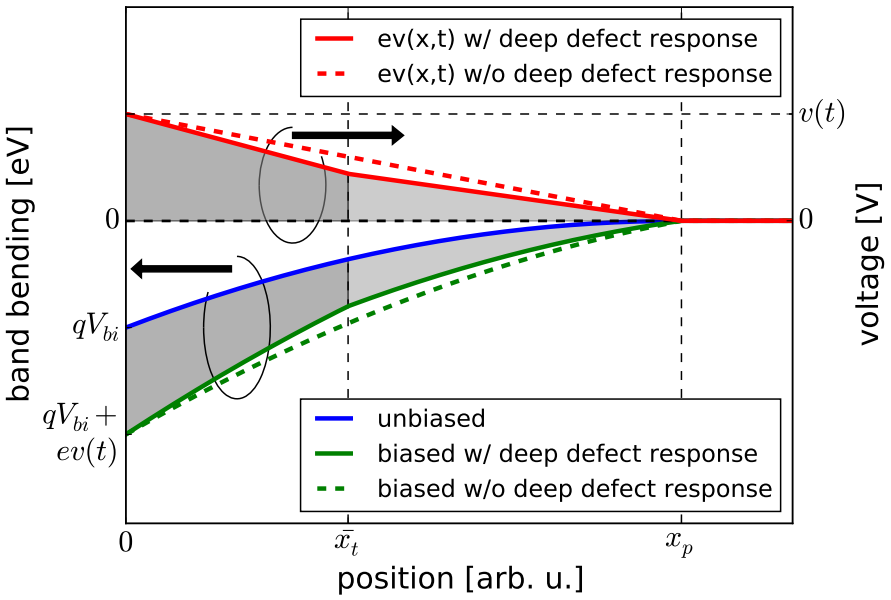


Figure 5.3.: ***Spatial potential drop with a deep defect across SCR*** *- Upper curve: Potential drop $v(x,t)$ with respect to depth into SCR with (solid red curve) and without (dashed red curve) a contribution of deep defects at $\bar{x}_t$. Charge is modulated at x_p and at $\bar{x}_t$, which leads to a local voltage modulation according to Eqn. (5.25).*

[1] The band bending is depicted for a uniform doping density without deep defects and thus results in parabolic bands. However, also deep defects contribute to the band bending. This contribution is neglected for the steady state band bending, because the purpose of this graph is to show the deviation due to a small bias voltage.

A consequence of the assumptions made above is that $\delta q_t(t)$ (see Eqn. (5.20)) can be simplified to

$$\delta q_t(t) = e\delta n_t(t)\Delta x. \tag{5.26}$$

In the representation of Eqn. (5.26) the spatial and the temporal components are separated. The width of δq_t is Δx, while the magnitude δn_t is dependent on the modulation frequency. For low frequencies all traps respond instantaneously and $\delta n_t = N_t$, while at high frequencies $\delta n_t = 0$. With these assumptions the graph in Fig. (5.1) is justified, where δq_t and δq_p take rectangular shapes.

With the help of Eqn. (5.26) the differential equation of $\delta n_t(x,t)$ (Eqn. (5.22)) can be written as a differential equation of $\delta q_t(t)$ and reads

$$\frac{\partial}{\partial t}\delta q_t(t) = -f_t\delta q_t(t) + g_t v(t). \tag{5.27}$$

with

$$f_t = f_0\left(1 + \frac{\bar{x_t}}{x_p}\frac{N_t}{N_A}\right) \qquad \text{and} \qquad g_t = f_0\frac{\epsilon_R\epsilon_0}{x_p}\frac{N_t}{N_A}. \tag{5.28}$$

The solution of Eqn. (5.27) is

$$\delta q_t(t) = \frac{g_t}{f_t + i\omega}v_0\exp(i\omega t). \tag{5.29}$$

As expressed in Eqn. (5.18) the current is given by the change of charge modulation. Expressing $\delta q_p(t)$ in terms of $v(t)$ and $\delta q_t(t)$, the current reads

$$i(t) = \frac{\epsilon_R\epsilon_0}{x_p}\frac{\partial}{\partial t}v(t) + \left(1 - \frac{\bar{x_t}}{x_p}\right)\frac{\partial}{\partial t}\delta q_t(t). \tag{5.30}$$

With Eqn. (5.29) and taking only the imaginary part of Eqn. (5.30) divided by ω (see Eqn. (5.1)) the capacitance is obtained as

$$C(\omega) = \frac{\epsilon_R\epsilon_0}{x_p} + \left(1 - \frac{\bar{x_t}}{x_p}\right)\frac{f_t g_t}{f_t^2 + \omega^2}. \tag{5.31}$$

With

$$C_\infty = \frac{\epsilon_R\epsilon_0}{x_p} \tag{5.32}$$

and

$$\Delta C = \frac{g_t}{f_t}\left(1 - \frac{\bar{x_t}}{x_p}\right) \tag{5.33}$$

Eqn. (5.31) yields

$$C(\omega) = C_\infty + \Delta C\frac{1}{1 + \frac{\omega^2}{f_t^2}}. \tag{5.34}$$

From this representation it is clear that the capacitance follows a (smooth) step like function

from low to high frequencies with a capacitance drop given by ΔC and with an inflection frequency f_t given according to Eqn. (5.28). For $N_A \gg N_t$, f_t reduces to $f_t \approx f_0 = 2e_p$. However, in both cases the inflection frequency is proportional to the emission coefficient e_p of the trap state, which allows the calculation of the trap energy.

5.2.1. Calculation of trap energy

In order to calculate the trap energy it is necessary to make use of the energy and temperature dependence of the emission rate e_p. For the deviation the principle of detailed balance needs to be applied. The trapping and emission processes taking place at a defect site are depicted in Fig. (5.4). Free electrons (holes) are captured from the conduction (valence) band with a rate $R_{e,imp}$ ($R_{h,imp}$) and emitted with the rate $G_{e,imp}$ ($G_{h,imp}$), where the subscripts stands for *impurity*.

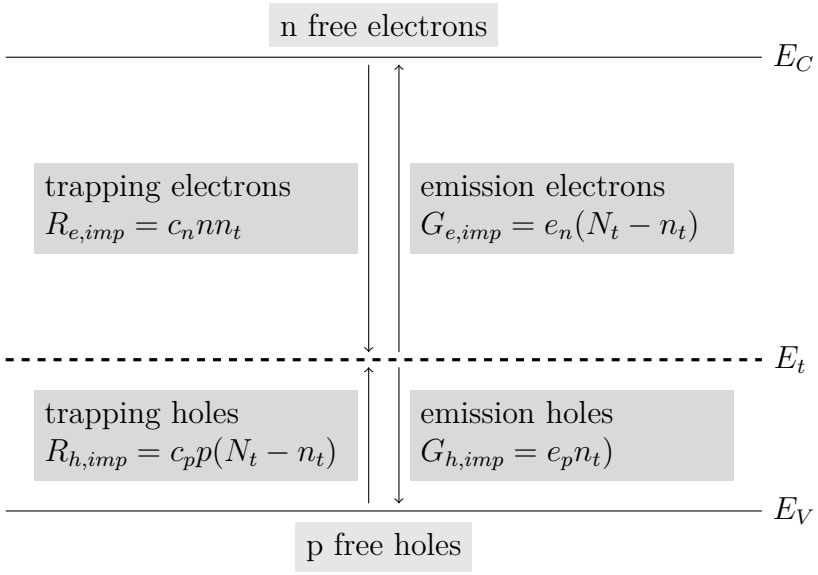


Figure 5.4.: ***Trapping and emission for a deep defect*** *- Trapping of electrons (holes) occurs from the conduction (valence) band with the capture coefficients c_n (c_p). Emission into the respective bands occurs with the emission rates e_n and e_p for electrons and holes, respectively.*

In steady state conditions, the trapping rate equals the emission rate for electrons and holes respectively such that [111]

$$c_n n n_t = e_n(N_t - n_t) \tag{5.35}$$

$$c_p p(N_t - n_t) = e_p n_t, \tag{5.36}$$

where N_t is the defect density and n_t the density of defect states occupied by a hole. Under equilibrium conditions the density of free electrons, free holes and occupied defect states is given by the Fermi-Dirac distribution $f(E)$. Equations (5.35) and (5.36) can be solved for e_n and e_p respectively such that

$$e_n = c_n N_C \exp\left(\frac{E_t - E_C}{kT}\right) = \nu_n \exp\left(\frac{E_t - E_C}{kT}\right) \tag{5.37}$$

$$e_p = c_p N_V \exp\left(\frac{E_V - E_t}{kT}\right) = \nu_p \exp\left(\frac{E_V - E_t}{kT}\right). \tag{5.38}$$

The prefactors of the exponential term are known as the attempt to escape frequencies ν_n and ν_p for electrons and holes, respectively. With f_t from Eqn. (5.28) and knowing $f_0 = 2e_p$, Eqn. (5.37) can be rewritten as

$$f_t = 2\nu_p \exp\left(\frac{E_V - E_t}{kT}\right)\left(1 + \frac{\bar{x_t}}{x_p}\frac{N_t}{N_A}\right). \tag{5.39}$$

Assuming now $N_A \gg N_t$ and taking into account the weak temperature dependence of ν_p of T^2, Eqn. (5.39) reads

$$f_t = f_0 = 2\xi_0 T^2 \exp\left(\frac{E_V - E_t}{kT}\right) \tag{5.40}$$

$$= 2\nu_p \exp\left(\frac{E_V - E_t}{kT}\right). \tag{5.41}$$

Therefore, an Arrhenius plot can be drawn with $\ln f_t T^{-2}$ versus $1/T$, which results in a straight line. The slope of that curve results in the defect energy while the intercept with the ordinate gives $2\xi_0$.

Often, the exact origin of the capacitance step is not known and therefore cannot straight forwardly be attributed to a deep defect. Nevertheless, the inflection frequencies might still be thermally activated but with another exponent of the weak temperature dependence. Thus, the weak temperature dependence is often neglected and ν_p in Eqn. (5.41) is taken to be temperature independent. This approach is valid as the inflection frequency f_t is dominated by the exponential function in Eqn. (5.40).

For the determination of the inflection frequencies from a measured capacitance spectrum, the derivative of the capacitance is plotted versus the frequency (or angular frequency). The derivative of the capacitance is defined in the following as

$$C'(\omega) = \frac{\mathrm{d}C}{\mathrm{d}\log\omega} = \omega\frac{\mathrm{d}C}{\mathrm{d}\omega} = f\frac{\mathrm{d}C}{\mathrm{d}f}. \tag{5.42}$$

In the plot of $C'(\omega)$ versus ω, the capacitance step is represented as a peak with its maximum at the inflection frequency[2].

5.3. Defect distributions

In the previous section the influence of a deep defect state was discussed, which is located at a discrete energy in the bandgap. However, in general these defects are not located at

[2]Note that from Eqn. (5.34) the inflection frequency is given as an angular frequency. Thus, when plotting the derivative versus the frequency f, as I will do it in this thesis, the determined position of the maximum still needs to be multiplied with 2π to obtain f_t.

a discrete energy level but are broadened. Walter et al. [24] developed a method for the evaluation of defect distributions which is discussed in section 5.3.1. However, this analysis is not able to deconvolute overlapping capacitance steps. Thus, I developed a method which allows the analysis of overlapping capacitance steps by fitting the complete temperature dependent capacitance spectrum simultaneously. This fitting procedure is described in section 5.3.2.

5.3.1. Walter analysis

Based on the rate equations as shown in Fig. (5.4) and a small signal perturbation analysis Walter *et al.* [24] derived the following formula for the calculation of the defect density:

$$N_t(E_\omega) = -\frac{2V_{bi}^{3/2}}{x_p\sqrt{q}\sqrt{qV_{bi}-(E_g-E_\omega)}}\frac{\mathrm{d}C}{\mathrm{d}\omega}\frac{\omega}{kT}. \tag{5.43}$$

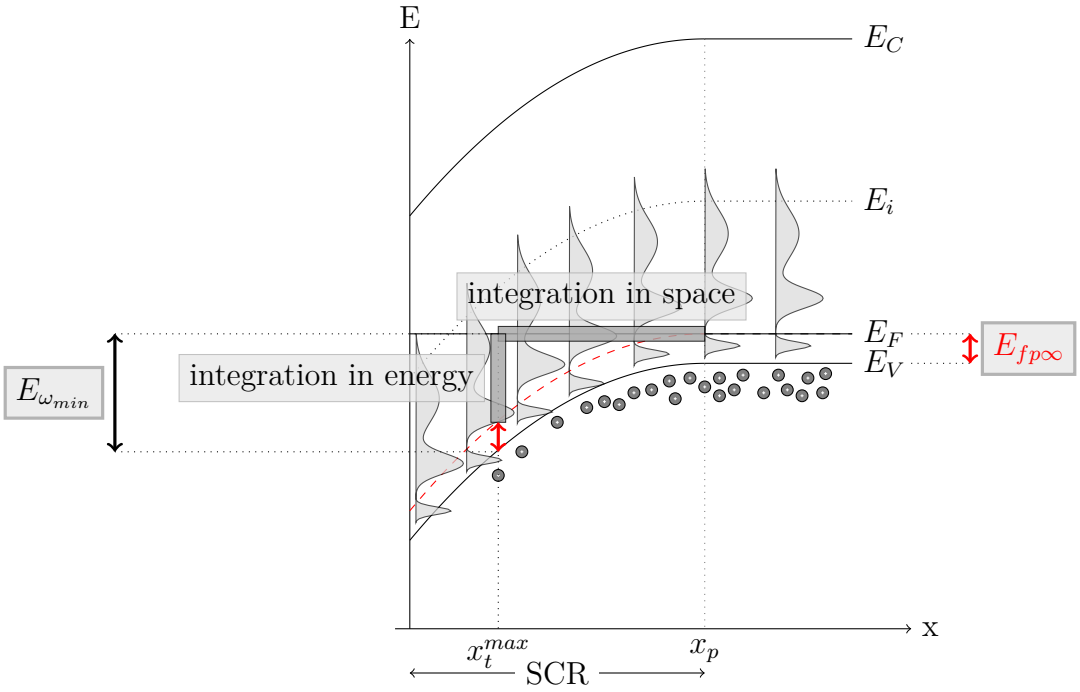


Figure 5.5.: ***Explanation of integration of defect distributions for the calculation of the capacitance*** *- Only defects crossing the Fermi level and with a time constant higher then the modulation frequency contribute to the capacitance. This corresponds either to an integration in space from x_t^{max} to x_p or equivalent to an integration in energy from $E_{fp\infty}$ (dashed red line) to $E_{\omega_{min}}$.*

The sampling character of the defect distribution is given by the term $\mathrm{d}C/\mathrm{d}\omega$ as it is demonstrated in Fig. (5.5) and explained in the following. Contributions to the capacitance arise at points, where the defect distribution crosses the Fermi level and where the time constant of the defect distribution is faster than the modulation frequency. Denoting now f_t as ω and $E_t - E_V$ (for holes) as E_ω, Eqn. (5.41) expresses as

$$\omega = \nu_p \exp(-E_\omega/kT), \tag{5.44}$$

where we say that for a given frequency ω defects up to an energy E_ω are able to respond to the external modulation voltage. For this argument a common attempt to escape frequency ν_p for all defects in that distribution is assumed. Eqn. (5.44) can be solved for E_ω and reads

$$E_\omega = kT \ln(\nu_p/\omega) \tag{5.45}$$

Given a probing frequency ω the defects respond up to an energy E_ω according to Eqn. (5.45). Therefore, defects in the energy range $[E_{fp\infty},\ E_{\omega_{min}}]$ contribute to the capacitance. $E_{fp\infty}$ denotes the distance of the Fermi level in the bulk of the p-type absorber. $E_{\omega_{min}}$ is defined as the maximal probing energy which is measured for the smallest applied frequency ω_{min}. Thus, the integration of capacitance contributions in space from x_p to x_t^{max} can be transformed into an integration of capacitance contributions in energy from $E_{fp\infty}$ to $E_{\omega_{min}}$. The lower limit of the integration $E_{fp\infty}$ is noted as a dashed red line in Fig. (5.5). Therefore, by increasing the modulation frequency by $\mathrm{d}\omega$, defects located at an energy E_ω stop responding and a drop in capacitance is observed. Thus, the term $\mathrm{d}C/\mathrm{d}\omega$ is a measure for the defect distribution with respect to the energy.

In order to plot the defect distribution from a capacitance spectrum, the frequency axis ω needs to be converted into an energy axis according to Eqn. (5.45). To do so, the correct attempt to escape frequency ν_p needs to be chosen such that the curves measured at different temperatures overlap (at the peak maximum). This condition is fulfilled with the correct attempt to escape frequency, as independent of the temperature, the same defect distribution is sampled. If the weak temperature dependence of ν_p is not neglected, of course the correct value for ξ_0 needs to be chosen. As mentioned above, the temperature dependence is dominated by the exponential term in Eqn. (5.40). Thus, with the correct value of ξ_0 the curves measured at different temperatures overlap as well.

Often, information of the built-in voltage and the SCR width are not easily accessible from the measurements, but are needed for the calculation of the defect density in Eqn. (5.43). Thus, to plot the shape of the defect distribution it is sufficient to plot $\frac{\mathrm{d}C}{\mathrm{d}\omega}\frac{\omega}{kT}$ on the ordinate. The term $\frac{\mathrm{d}C}{\mathrm{d}\omega}\frac{\omega}{kT}$ is called the scaled derivative, following the notation given in Ref. [112]. It is given in the unit of capacitance per area per energy. Thus, by integrating the area under the peak of the scaled derivative results in the capacitance drop ΔC of this capacitance step [27]. This determination of the capacitance drop by integrating the area under the peak in the scaled derivative is important for a later comparison with the fitting routine for the assessment of the correct defect density (see section 5.3.3).

An example of the analysis according to the Walter analysis is given in Fig. (5.6). This defect distribution is derived from a sequentially processed solar cell following the CAPRI process [84] with a Cu-poor precursor (see section 3.2). This capacitance spectrum exhibits two low temperature capacitance transitions (see section 5.5.2) and therefore in the Walter analysis two peaks are obtained. Two different attempt to escape frequencies are needed as it is not possible to align both peaks with only one attempt to escape frequency. Thus, according to Eqn. (5.45) two different energy axis are obtained. To fit the peak and consequently to fit the area A under the peak, a Gaussian distribution was used for each peak according to

$$N_t(E) = \frac{A}{\sqrt{2\pi}\sigma} e^{-\frac{(E-E_0)^2}{2\sigma^2}}. \tag{5.46}$$

The obtained fitted defect parameters A, σ and E_0 with the chosen attempt to escape frequency ν_p are listed in Fig. (5.6). Note that the area A describes the capacitance drop ΔC due to

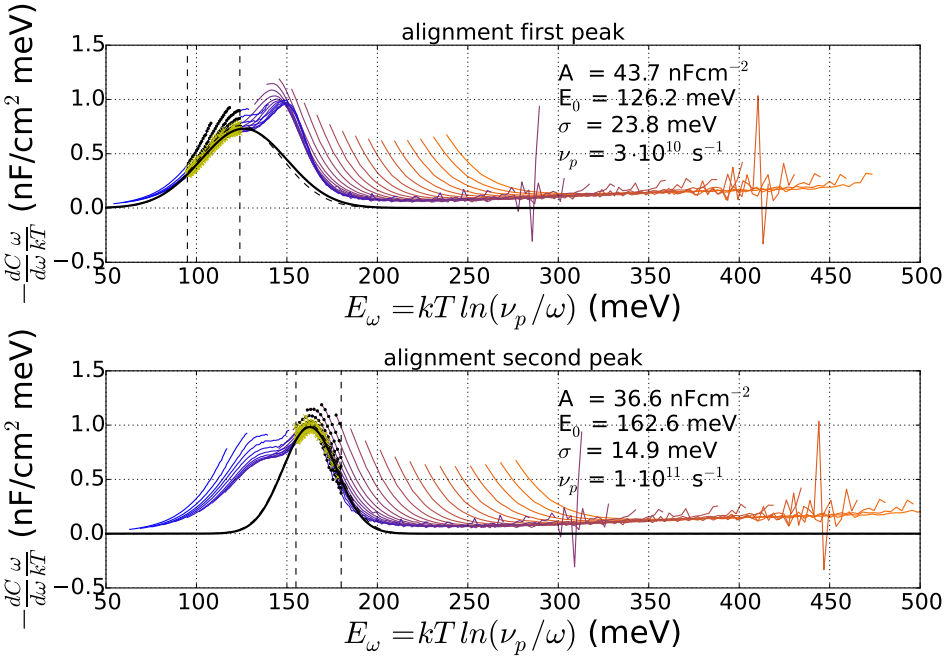


Figure 5.6.: ***Calculated defect distribution from the Walter analysis*** *- Plotted is only the scaled derivative $\frac{\mathrm{d}C}{\mathrm{d}\omega}\frac{\omega}{kT}$ and not the absolute number of the defect density as the built-in voltage and the SCR width from Eqn. (5.43) are a priori not know. Black dots represent datapoints within the fitting limits (dashed lines), while the green datapoints are datapoints used for the fit. Capacitance data from sample AR133 P62 sec5 is used.*

that defect level. As each peak has its own energy axis, it is not possible to fit both peaks simultaneously. Hence, each fit also takes contributions from the other peak, which is not fitted, because these two steps overlap. As a consequence, the capacitance contributions are overestimated resulting in an overestimation of the defect concentration.

5.3.2. Fitting of the capacitance spectrum

In order to solve the problem of deconvoluting the contribution of overlapping capacitance steps, it is possible to fit the capacitance spectra. An approach which is generally used in literature is the fitting of a capacitance - frequency curve with an equivalent circuit [36, 113]. In this analysis the SCR is modelled as a capacitor and a resistor in parallel, while additional discrete defect levels are modelled as RC elements in parallel to the SCR circuit [114, 115]. In order to describe broad capacitance transitions, constant phase elements can be used instead of the resistor [113, 116]. However, not only bulk defects can be included into the model, but also interface defects, inversion layers and back contacts [117]. The drawback of all these models is that the capacitance - frequency curve needs to be fitted for every temperature separately and therefore requires a large set of fitting parameters. Caruso *et al.* incorporated a temperature dependence for these parameters, however, the capacitance spectrum could not be well described by this model [118].

In the following I will describe how it is possible do fit the complete capacitance spectra directly and simultaneously. I have published the derivation and the obtained results from this fitting method in Ref. [27]. However, these findings are recaptured here as important conclusions

about the interpretation of the admittance spectra can be drawn from this analysis.

In order to fit the complete capacitance spectra for all temperatures directly and simultaneously, I made use of Eqn. (5.34). This equation needs to be expressed with its temperature dependent variables as well as expanded for a defect distribution. The only temperature dependent term is the inflection frequency f_t, which is associated to the emission rate (Eqn. (5.41)) as described in section 5.2.1. As I have shown in Ref. [27], the temperature dependent capacitance transition (Eqn. (5.34)) can be written as

$$C(\omega) = C_\infty + \left(1 + \frac{\omega^2}{\nu_p^2 \exp(-2E_t/kT)}\right)^{-1} \frac{N_t}{N_A}\frac{\lambda}{x_p} C_\infty, \tag{5.47}$$

with λ given by Eqn. (5.7)[3]. When assuming not a discrete defect distribution as $\delta(E - E_t)$ but a distribution given by $N_t(E)$, we have to add all contributions at all energies, and thus, the expression for the capacitance can be written as [27]

$$C(\omega) = C_\infty + \frac{C_\infty}{N_A x_p} \int_{E_{fp\infty}}^{E_{fp\infty}+qV_{bi}} \mathrm{d}E \frac{N_t(E)\lambda(E)}{1 + \frac{\omega^2}{\nu_p^2}\exp(2E/kT)}. \tag{5.48}$$

Defects shallower than $E_{fp\infty}$ do not cross the Fermi level and thus cannot contribute to the capacitance. Therefore, the lower limit of integration is chosen to be $E_{fp\infty}$. The upper limit is chosen in the same way since defects deeper than $E_{fp\infty} + qV_{bi}$ do not cross the Fermi level either. Capacitance steps located below the SCR capacitance are not attributed to deep defects but might show the same functional behaviour (see for example section 5.4.2). In that case the lower limit for integration is 0.

In the case of a Gaussian defect distribution around E_t^0 with a standard deviation of σ and a total density per unit volume of N_t^0, the defect distribution with respect to energy is given by

$$N(t) = \frac{N_t^0}{\sigma\sqrt{2\pi}} e^{-(E-E_t^0)/2\sigma^2}. \tag{5.49}$$

Using Eqn. (5.7) and (5.49), Eqn. (5.48) expresses as

$$C(\omega) = E_\infty + \frac{C_\infty N_t^0}{N_A x_p}\left(\frac{2\epsilon_R\epsilon_0}{e^2 N_A}\right)^{1/2} \cdot \left[\frac{1}{\sigma\sqrt{2\pi}} \int_{E_{fp\infty}}^{E_{fp\infty}+qV_{bi}} \mathrm{d}E \frac{e^{-(E-E_t^0)^2/2\sigma^2}\left(E - E_{fp\infty}\right)^{1/2}}{1 + \frac{\omega^2}{\nu_p^2}e^{2E/kT}}\right]. \tag{5.50}$$

Neglecting the weak energy dependence of λ with respect to the exponential term and subsequently describing all energy independent terms by a constant ΔC, Eqn. (5.50) can be written as

$$C(\omega) = C_\infty + \Delta C \left[\frac{1}{\sigma\sqrt{2\pi}} \int_{E_{fp\infty}}^{E_{fp\infty}+qV_{bi}} \mathrm{d}E \frac{e^{-(E-E_t^0)^2/2\sigma^2}}{1 + \frac{\omega^2}{\nu_p^2}e^{2E/kT}}\right] \tag{5.51}$$

For small frequencies, the denominator in the integral equals 1, and thus, the expression in the brackets also equals 1. Hence, the capacitance at low frequencies equals $C(0) = C_\infty + \Delta C$.

[3]Note that in this expression it is already assumed that $N_t \ll N_A$. However, by not writing $f_t = f_0$, Eqn. (5.47) can also be written without this assumption.

For high frequencies, the denominator tends to infinity, and the high frequency capacitance is $C(\infty) = C_\infty$. Therefore, from this deviation ΔC is the capacitance drop due to the broad defect level.

5.3.2.1. Temperature dependence

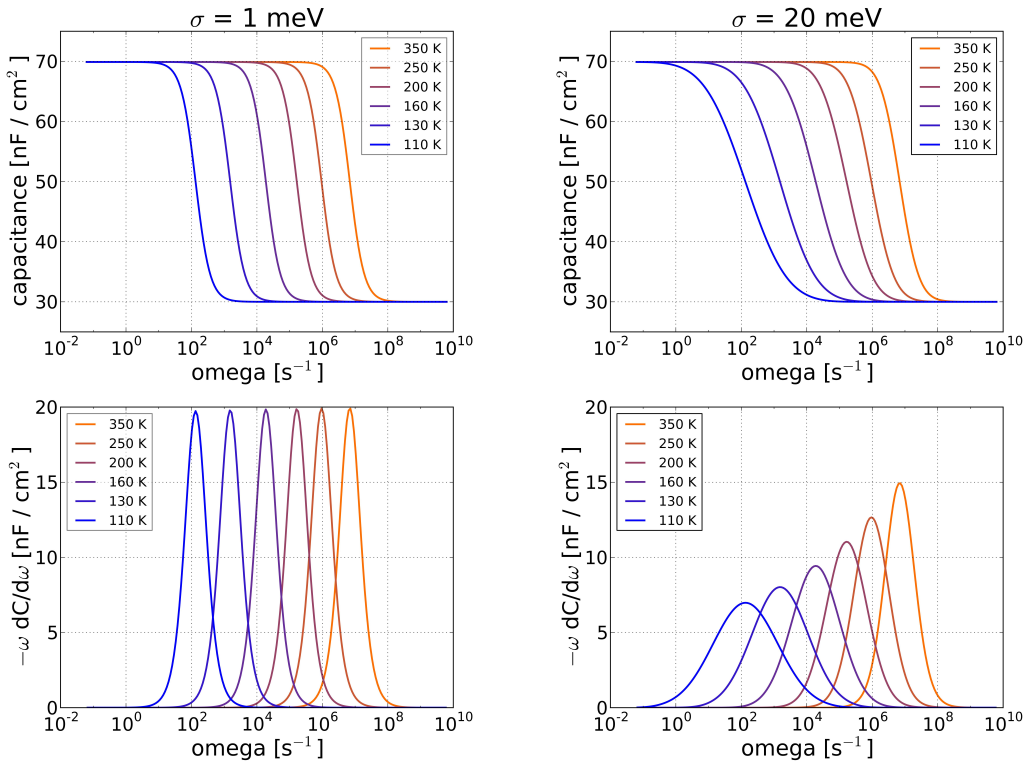


Figure 5.7.: ***Simulation of the capacitance step and its temperature dependence*** *- Left: Capacitance response from a narrow defect distribution. The only temperature dependence is the shift of the inflection frequency according to Eqn. (5.41). Right: Capacitance response from a broad defect distribution. An additional broading of the capacitance with lowered temperature is observed.*

We now have a closer look at the expression (5.51). Fig. (5.7) shows the calculated capacitance values on a wide frequency range for a narrow (left) and a broader (right) Gaussian defect distribution. The other parameters were chosen as $\Delta C = 40\,\mathrm{nF/cm^2}$, $C_\infty = 30\,\mathrm{nF/cm^2}$, $\nu_p = 1 \times 10^9\,\mathrm{s^{-1}}$ and $E_t^0 = 150\,\mathrm{meV}$. As the broad distribution consists of defects spread over a higher energy range, the capacitance step broadens as the distribution of inflection frequencies broadens as well according to Eqn. (5.41).

Another interesting feature when dealing with a broad defect distribution is that a broadening of the capacitance step occurs with respect to the temperature. This behaviour becomes obvious when plotting the derivative of the capacitance step, which expresses as a peak (lower part of Fig. (5.7)). When lowering the temperature, the peak broadens. As a consequence, the peak height must decrease since the integrated area under the peak still has to be equal to ΔC. The broadening can be understood when investigating the temperature dependence of Eqn. (5.51). For a defect state at an energy E the temperature dependence of the capacitance response originates from the inflection frequency given by Eqn. (5.41). In Fig. (5.8) the

energy dependence of the inflection frequency is plotted for two different temperatures. For a logarithmic scale on the ordinate it takes a linear shape with respect to energy with a slope given by $-1/kT$. For a given energy window, represented by the red bar in Fig. (5.8) and representing the width of the defect distribution, the inflection frequencies are wider distributed for low temperatures compared to higher temperatures. Therefore, the capacitance transition also broadens, and thus explains the temperature behaviour of the capacitance step and its derivative shown in Fig. (5.7).

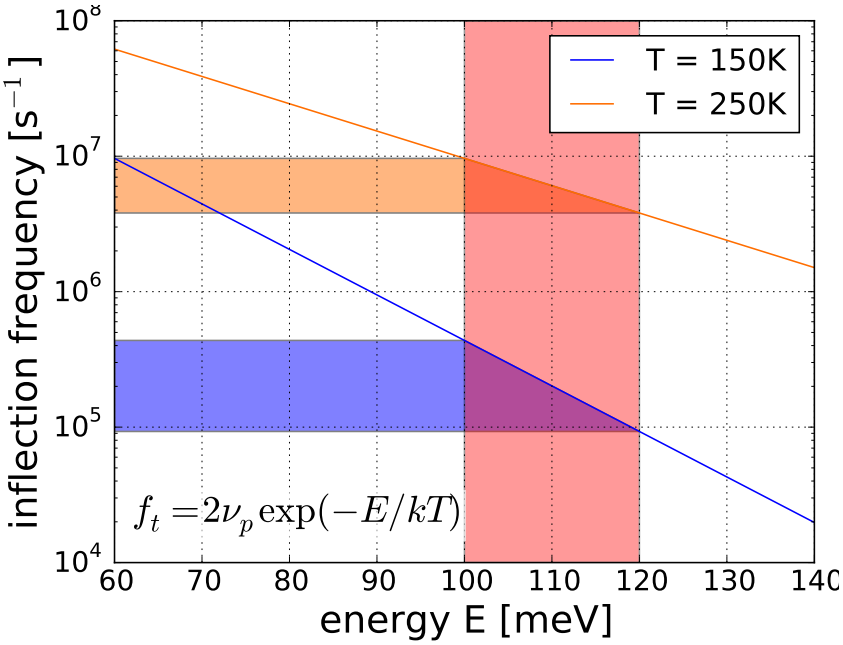


Figure 5.8.: ***Explanation for the temperature dependence of the capacitance response*** *- For a given energy window (red area) the inflection frequencies are distributed wider at low temperatures compared to high temperatures.*

5.3.2.2. Fitting function

As the experimental capacitance data in general consists of several steps, several defect levels need to be added in order to describe the spectrum. As I have shown in Ref. [43], our (sequentially processed) CZTSe devices exhibit three capacitance steps[4]. Thus, the capacitance is written as

$$C_(\omega, T) = C_\infty + \sum_{i=1}^{3} \frac{\Delta C_i}{\sigma_i \sqrt{2\pi}} \int_{E_{fp\infty}}^{E_{fp\infty}+qV_{bi}} \mathrm{d}E \frac{e^{-\left(E-E^0_{t,i}\right)^2/2\sigma_i^2}}{1+\frac{\omega^2}{\nu^2_{p,i}} e^{2E/kT}}. \tag{5.52}$$

The temperature is added as a parameter for the capacitance on the left hand side as a capacitance spectrum is measured for several temperatures and because the capacitance spectra

[4]The solid circles in Fig. (5.9) represent an experimental capacitance spectrum, indicating two low temperature and one high temperature capacitance step.

ought to be fitted for all temperatures simultaneously. Finally, a least square fit is performed minimising the squared residuals of the whole spectrum, i.e. reducing S'

$$S' = \frac{1}{N} \sum_T \sum_\omega |C_{meas}(\omega, T) - C(\omega, T)|^2. \tag{5.53}$$

N denotes the number of data points used for the fitting. To fit the data, the integration limits are adjusted to decrease the time for the calculation. The lower and the upper integration limits for the ith defect are chosen to be $\max(0, E_{t,i} - 3\sigma_i)$ and $\min(E_g, E_{t,i} + 3\sigma_i)$, respectively.

To improve the fit for small shoulders in the derivative, the spectrum of $-\omega \frac{\mathrm{d}C}{\mathrm{d}\omega}$ can also be included simultaneously into the fit. Thus, in general, the squared errors can be written as

$$r_{\omega,T} = \left[w_C \left| C_{meas}(\omega, T) - C(\omega, T) \right| - w_d \left| \omega \frac{\mathrm{d}C_{meas}(\omega, T)}{\mathrm{d}\omega} - \omega \frac{\mathrm{d}C(\omega, T)}{\mathrm{d}\omega} \right| \right]^2 \tag{5.54}$$

with the weights w_C and w_d for the capacitance and its derivative, respectively. For this more general case, the function given in Eqn. (5.55) is minimized

$$S = \frac{1}{(w_C + w_d)\, N} \sum_T \sum_\omega r_{\omega,T}. \tag{5.55}$$

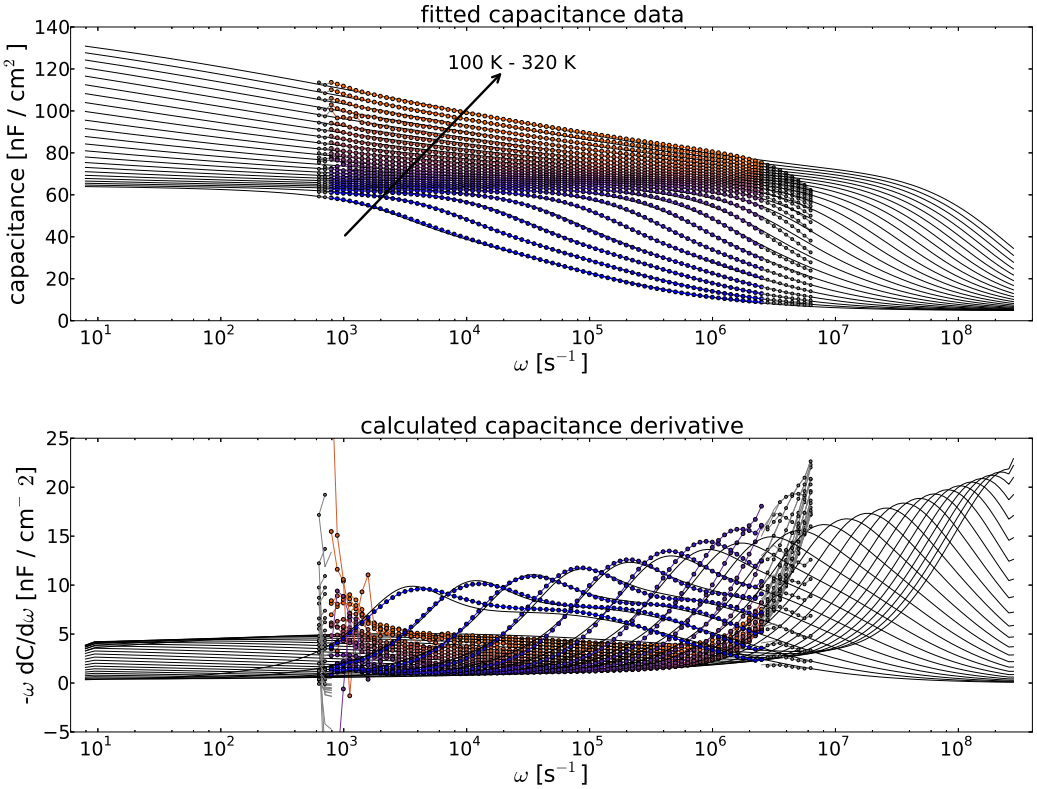


Figure 5.9.: ***Fitted capacitance spectrum*** *- Data for sample AR133 P62 sec5 was fitted according to Eqn. (5.52) including three Gaussian defect levels. Coloured (gray) data points represent measured data (not) used for fitting. Solid black lines show the fit of the data. The fit is extended to lower and higher frequencies to show the theoretical evolution of the spectrum.*

Fig. (5.9) shows an example of the fitted capacitance spectrum. It is the same spectrum as

used for the calculation of the defect distributions following the analysis of Walter *et al.* in section 5.3.1. For the fit w_d is chosen to be 1 and w_C equals 0. However, for less pronounced shoulders in the derivative, values between 1 and 5 are generally chosen for w_C. The high frequency data points shown as gray circles in Fig. (5.9) are excluded from the fit as they are distorted by the series resistance [119, 120]. The parameters for the fit are summarized in table 5.1. Two low energetic defect levels are fitted (i=1 and i=2) producing the overlapping low temperature capacitance step. The rise of capacitance at high temperatures and low frequencies is fitted with a broad deep defect distribution (i=3). A similar capacitance response was observed in CdTe absorber based solar cells and modelled in SCAPS with a deep broad band of acceptor states [121]. To find an indication for reasonable starting parameters, an Arrhenius plot can be made from distinct maxima in the derivative of the capacitance resulting in defect energy and attempt to escape frequency.

Table 5.1.: *Defect values obtained from the fitting routine and the Walter analysis as shown in Fig. (5.9) and Fig. (5.6).*

i	E_t (meV)	σ (meV)	ν_p (s^{-1})	ΔC (nF/cm^2)
			fitting routine	
1	115.2 ± 1.1	20.9 ± 0.5	$(9.1 \pm 0.7) \cdot 10^9$	41.7 ± 1.0
2	164.1 ± 1.8	2.5 ± 1.3	$(9.6 \pm 1.5) \cdot 10^{10}$	10.7 ± 0.7
3	922.1 ± 116.6	334.2 ± 44.0	$(3.8 \pm 0.2) \cdot 10^{13}$	263.9 ± 93.6
			Walter method	
1	126.2 ± 3.5	23.8 ± 0.8	$(3 \pm 1) \cdot 10^{10}$	43.7 ± 1.3
2	162.6 ± 2.3	14.9 ± 0.9	$(1 \pm 2) \cdot 10^{11}$	36.6 ± 4.6
3	N/A	N/A	N/A	N/A

5.3.3. Comparison of evaluation methods

In this section I want to compare the defect parameters obtained by the Walter analysis and the fitting routine. I will elucidate the problems, when dealing with overlapping capacitance steps as it is the case in CZTSe based solar cells [43, 122].

A summary of the obtained defect parameters for the Walter analysis and the fitting routine is given in Tab. 5.1. The defect energies E_t and the attempt to escape frequencies ν_p for the two low temperature capacitance steps are comparable for both evaluation methods. This makes sense because the positions of the maxima in the derivative of the capacitance are defined by the mean energy and the attempt to escape frequency of the defect level according to Eqn. (5.41). For a well behaved defect level this results in a straight line in the Arrhenius plot. For the Walter method it implies that the curves overlap when choosing the correct attempt to escape frequency and when fitting the capacitance data, the positions of the maxima in the derivative overlap with the maxima of the fit.

Comparing the amount of contribution from each individual capacitance step represented by ΔC in Table 5.1 we find a discrepancy. While for the Walter method both capacitance steps contribute roughly the same amount, we find a difference of a factor 4 for the second capacitance step (i=2) from the fitting routine. This can be explained based on the fact that we deal with overlapping capacitance steps. The contribution from each capacitance step cannot be deconvoluted in the Walter method: when plotting each peak on its proper energy axis also contributions from the other peak are present which cannot be accounted for. The peaks cannot be fitted simultaneously since they have different energy axes due to different attempt to escape frequencies. In contrast, in the fitting routine the whole spectrum is fitted simultaneously and thus deconvolutes the capacitance contributions. Therefore, the correct contribution to each capacitance step is assigned. Consequently, it can be stated that the Walter method overestimates the density of states in the case of overlapping capacitance steps. This fact can additionally be verified by looking at the summed contribution of both capacitance steps. The summed contribution of both capacitance steps in the Walter analysis gives $80.3\,\mathrm{nFcm^{-2}}$. This value is much higher than the total capacitance drop for both low temperature capacitance steps together as can be seen from Fig. (5.9).

The evaluated standard deviations σ also differ for both methods. This can be caused by the fact that the Walter method in general overestimates the width of the distribution [24]. Another distortion which can influence the width is again the overlapping character of the two low temperature capacitance steps.

Another advantage over the Walter method is the possibility to quantify the deep broad defect distribution. As it is shown in Fig. (5.6) this capacitance transition at high temperatures does not show an inflection frequency. Thus, it is not possible to reliably fit a Gaussian distribution in this energy range.

5.4. Alternative origins for capacitance steps

In the previous two sections the admittance spectroscopy was discussed in terms of its main purpose, which is the analysis of defect levels in semiconductors. It is the frequency and temperature dependence of the capacitance of a defect level resulting in a drop of the capacitance when going to high frequencies or low temperatures.

However, a deep defect is not the sole origin of a capacitance step, but also other factors may result in a frequency dependence of the capacitance and ultimately give rise to a drop in capacitance. These different origins of a capacitance step will be discussed in the following subsections. For all these discussion the influence of deep defects is neglected such that at low frequencies only the SCR capacitance is measured.

5.4.1. Influence of the series resistance

For the discussion of the series resistance r_S an equivalent circuit for the SCR is necessary. The SCR can be viewed as parallel connection of a capacitor and a resistor as shown in Fig. (5.10a). This circuit is notated in the following as the Cp-G mode. The capacitor represents the SCR capacitance according to Eqn. (5.5) and the shunt resistance R_{sh} describes the leakage current. The calculated admittance from this equivalent circuit is given by

(a) Cp-G mode for the measurement of the capacitance and the conductance.

(b) Addition of a series resistance to the equivalent SCR circuit.

Figure 5.10.: ***Equivalent circuit for the measurement of the capacitance and the conductance*** *- a) shows the generally applied equivalent circuit for the measurement of the capacitance and the conductance as given in Eqn. (5.1). b) adds a series resistance to that circuit which can have a strong influence on the measured capacitance for high frequencies [119].*

$$Y_{Cp-G} = \frac{1}{R_{sh}} + i\omega C_{SCR}. \tag{5.56}$$

Thus, in this ideal case the measured capacitance corresponds to the SCR capacitance and the measured conductance to the conductance of the resistor $1/R_{sh}$. However, in general, a solar cell device also exhibits a series resistance, which may influence the response in the measured frequency range [119]. Therefore, a series resistance needs to be added to the Cp-G model as shown in Fig. (5.10b). With this addition of the series resistance, again the admittance can be calculated and reads

$$Y_{mod} = \frac{1}{R_{sh}} \frac{1 + \frac{r_S}{R_{sh}} + \omega^2 R_{sh} r_S C_{SCR}^2}{\left(1 + \frac{r_S}{R_{sh}}\right)^2 + (\omega r_S C_{SCR})^2} + i\omega \frac{C_{SCR}}{\left(1 + \frac{r_S}{R_{sh}}\right)^2 + (\omega r_S C_{SCR})^2}. \tag{5.57}$$

For reasonable solar cell devices it holds that $r_S \ll R_{sh}$ and thus Eqn. (5.57) reduces to

$$Y_{mod} = \frac{1}{R_{sh}} \frac{1 + \omega^2 R_{sh} r_S C_{SCR}^2}{1 + (\omega r_S C_{SCR})^2} + i\omega \frac{C_{SCR}}{1 + (\omega r_S C_{SCR})^2}. \tag{5.58}$$

Experimentally, not the SCR capacitance C_{SCR} is measured but a value smaller than C_{SCR} due to the distortion of the series resistance, which in the following is notated as the measured capacitance given by $\mathrm{Im}(Y_{mod}/\omega)$. Thus, focusing on the measured capacitance it can be observed from Eqn. (5.58) (as well as from Eqn. (5.57)) that the measured capacitance reduces to zero for high frequencies due to the time constant of the $r_S C_{SCR}$ element. A rough estimate of this time constant for our devices can be made with $C_{SCR} \approx 100\,nF/cm^2$ and a $r_S \approx 1\,\Omega cm^2$ which results in a time constant of $\tau = r_S C_{SCR} = 10^{-7} s$. This value lies outside the measured frequency range and therefore should not influence the measured capacitance profile. However, it has been shown by Kneisel *et al.* that the spectrum above 10^5 Hz can be influenced by the sheet resistance of the window layer for a cell area of 0.5 cm^2 and a contact grid [120].

Additionally, the capacitance spectra are recorded for various temperatures and if the series resistance is not constant with respect to temperature, this circuit response can influence the capacitance spectrum at lowered temperatures. In fact, for CZTSe and CZTS based solar cells, a thermally activated series resistance is observed [34, 37, 43, 49, 55, 123, 124]. In Ref. [122] I

could show that the low temperature capacitance transition is indeed influenced by the series resistance. This issue is further discussed in section 5.5.2.1.

5.4.2. Carrier freeze-out

A carrier freeze-out can be described by a decreasing free carrier concentration with decreasing temperature such that the holes (electrons) from the doping acceptor (donor) state are not excited into the valence (conduction) band anymore [125]. A result of the reduced carrier concentration is an increased series resistance, given (for a p-type semiconductor) by Equations (5.59) and (5.60):

$$r_S = \rho d, \tag{5.59}$$

with

$$\rho = \frac{1}{pq\mu_p}. \tag{5.60}$$

d is the thickness of the absorber, p the free hole concentration and μ_p the hole mobility. For compensated semiconductors, p can be expressed as [44]

$$p = \left(\frac{N_A - N_D}{gN_D}\right) N_V \exp\left(-\frac{E_A}{kT}\right), \tag{5.61}$$

where N_D denotes the compensating donor density and g the degeneracy factor of the valence band. The weak temperature dependence of the mobility in Eqn. (5.60) can be neglected with respect to the exponential term in p. Eqn. (5.59), (5.60) and (5.61) can then be inserted into Eqn. (5.58) and the measured capacitance in case of a carrier freeze-out results as

$$C = \frac{C_{SCR}}{1 + \frac{\omega^2}{\eta_0^2}\exp\left(\frac{2E_A}{kT}\right)} \tag{5.62}$$

with

$$\eta_0 = \frac{q\mu_p N_V}{dgC_{SCR}} \frac{N_A - N_D}{N_D}. \tag{5.63}$$

Eqn. (5.62) takes the same form as Eqn. (5.51), the capacitance response of a deep defect, for $\sigma \to 0$. The low frequency capacitance corresponds to the SCR capacitance.

Unlike suggested by Eqn. (5.62), the capacitance at high frequencies does not equal zero, as it is still possible to measure the geometrical capacitance of the absorber layer C_{geo}^{abs}. In this case the complete absorber layer acts as a dielectric and the charge modulation takes place at the back and at the front contact (window layer) so that the solar cell device behaves like a parallel plate capacitor. Thus, the geometrical capacitance is given by

$$C_{geo}^{abs} = \frac{\epsilon_R \epsilon_0}{d}. \tag{5.64}$$

5.4.3. Back contact barrier

A back contact barrier arises, if the back contact (in general Mo for CZTSe and CIGSe based solar cells) is not ohmic, which means that a SCR also develops at the back contact. Such an additional SCR at the back contact can be modelled as an additional diode in opposite direction to the (main) junction diode for dc conditions [126]. For ac conditions as in admittance spectroscopy, this second SCR at the back contact expresses as another RC element as shown in Fig. (5.11) [117, 126]. This equivalent model is also one of the possible explanations for the N1 capacitance step in CIGSe based solar cells [127].

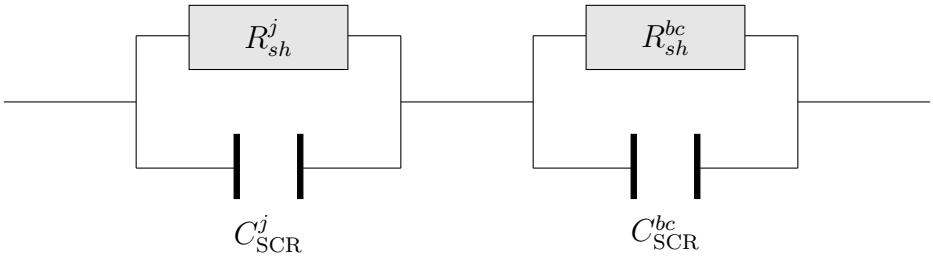


Figure 5.11.: ***Equivalent circuit for ac measurements of a Schottky like contact with a back barrier*** *- Superscript j denotes main junction with the front contact. The superscript bc stands for the back contact barrier.*

As derived by Niemegeers *et al.* [126], the frequency dependence of the circuit shown in Fig. (5.11) expresses as

$$C(\omega) = \frac{C^j_{SCR} {G^{bc}_{sh}}^2 + C^{bc}_{SCR} {G^j_{sh}}^2 + \omega^2 C^{bc}_{SCR} C^j_{SCR} (C^{bc}_{SCR} + C^j_{SCR})}{(G^{bc}_{sh} + G^j_{sh})^2 + \omega^2 (C^{bc}_{SCR} + C^j_{SCR})^2}. \tag{5.65}$$

At zero bias the current is not limited by the back contact and thus $G^{bc}_{sh} \gg G^j_{sh}$ [126]. Therefore, we can rewrite the expression (5.65) to

$$C(\omega) = \frac{C^j_{SCR} {G^{bc}_{sh}}^2 + \omega^2 C^{bc}_{SCR} C^j_{SCR} (C^{bc}_{SCR} + C^j_{SCR})}{{G^{bc}_{sh}}^2 + \omega^2 (C^{bc}_{SCR} + C^j_{SCR})^2} \tag{5.66}$$

From the above expression it can be observed that the capacitance makes a transition from low to high frequencies from C_j to $C_c C_j/(C_c + C_j)$, respectively. This implies that at low frequencies the junction capacitance is measured, while at high frequencies the series connection of the junction and the back contact capacitance is measured. Additionally, the inflection frequency can be deduced as

$$\omega_0 = \frac{G^{bc}_{sh}}{C^j_{SCR} + C^{bc}_{SCR}}. \tag{5.67}$$

and thus, it has the same activation as the back contact conductance, G^{bc}_{sh}.

The current over a Schottky barrier assuming thermionic emission is given by [44]

$$J(V) = A^* T^2 \exp\left(-\frac{\Phi_B}{kT}\right)\left[\exp\left(\frac{qV}{kT}\right) - 1\right]. \tag{5.68}$$

Thus, the conductance at the back contact G^{bc}_{sh} for small voltages can be written as

$$G_{sh}^{bc} = \frac{qA^*T}{k}\exp\left(-\frac{\Phi_B}{kT}\right). \tag{5.69}$$

Inserting this equation into (5.66) yields an expression for the capacitance with respect to temperature and frequency as

$$C(\omega,T) = \frac{C_{SCR}^{j}\left(\frac{qA^*T}{k}\right)^2\exp\left(-\frac{2\Phi_B}{kT}\right) + \omega^2 C_{SCR}^{bc}C_{SCR}^{j}\left(C_{SCR}^{bc}+C_{SCR}^{j}\right)}{\left(\frac{qA^*T}{k}\right)^2\exp\left(-\frac{2\Phi_B}{kT}\right) + \omega^2\left(C_{SCR}^{bc}+C_{SCR}^{j}\right)^2}. \tag{5.70}$$

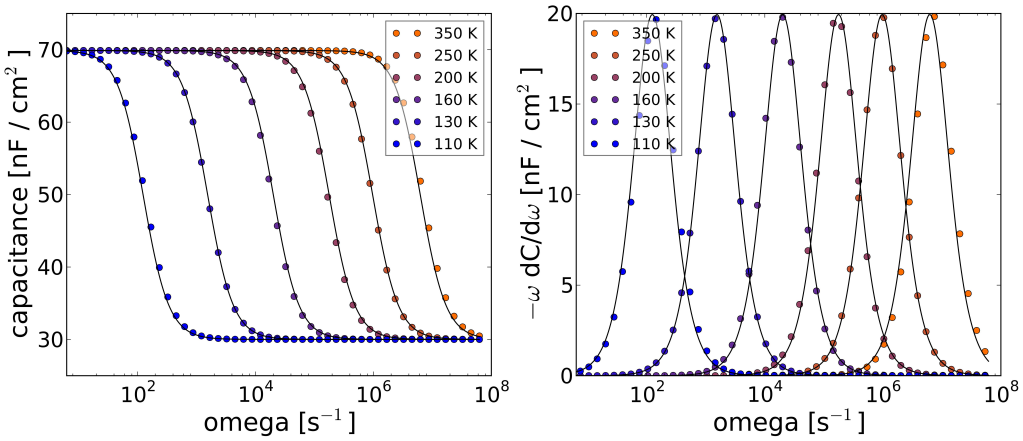
Eqn. (5.70) can be used to fit the complete capacitance spectrum with respect to frequency and temperature. This expression differs from the expressions derived for a deep defect or a carrier freeze-out and thus yields a different shape. In order to see how these functions differ from each other a capacitance spectrum according Eqn. (5.51) was simulated and subsequently fitted by Eqn. (5.70). Fig. (5.12a) shows the result for a very narrow defect distribution with $\sigma = 1\,\text{meV}$ and Fig. (5.12b) the result for a defect distribution with $\sigma = 10\,\text{meV}$. The parameters used for simulating the capacitance response of a defect distribution and the obtained fit parameters for the back barrier are summarized Tab. 5.2. As can be observed, the back barrier fits the response of an (almost) discrete defect level very well. However, when assuming a defect distribution as it is the case shown in Fig. (5.12b), the response of the back barrier deviates due to the temperature dependence of a broad defect distribution as discussed in section 5.3.2.1. This behaviour might be modelled with a distributed back barrier. In that case the barrier height does not have a single energy Φ_B but is distributed for example according to a Gaussian distribution. However, this derivation was not carried out so far and will not be discussed in this thesis.

Table 5.2.: *Parameters for simulating the capacitance response of Fig. (5.12) and the obtained fitting results for a back barrier. Clearly, the broadening of the capacitance step due to a higher value of σ cannot be reproduced by the model of a back barrier.*

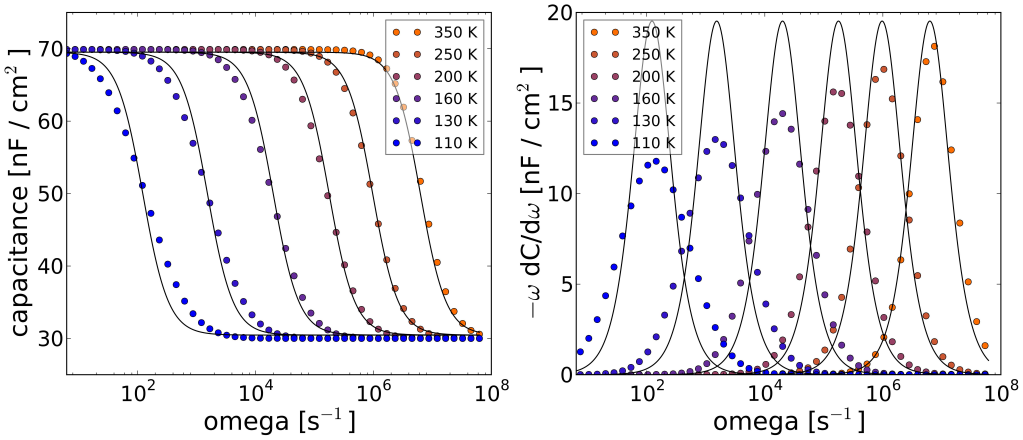
	defect distribution					back barrier (fitted)			
	ΔC (nF/cm^2)	C_∞ (nF/cm^2)	ν_p (s^{-1})	σ (meV)	E_0 (meV)	C_{SCR}^{j} (nF/cm^2)	C_{SCR}^{bc} (nF/cm^2)	A^*	Φ_B (meV)
(a)	40	30	$1\cdot10^9$	1	150	69.5	54.2	$1.30\cdot10^{-9}$	165.8
(b)	40	30	$1\cdot10^9$	10	150	69.5	54.2	$1.30\cdot10^{-9}$	165.8

5.4.4. Inversion layer or interface defects

As has been pointed out by Niemegeers *et al.* [108] an inversion layer at the (CdS) buffer/absorber interface can also produce a capacitance step [128] even in the absence of interface defects. For that model not only the absorber layer needs to be considered but also the buffer layer. As-



(a) Simulation with a defect width of $\sigma = 1$ meV.



(b) Simulation with a defect width of $\sigma = 10$ meV.

Figure 5.12.: ***Simulation of defect response fitted with a back barrier*** *- Simulations were done with a narrow (a) and a broader (b) defect distribution. As observed from the fit, the model for the back barrier with a discrete barrier height does not reproduce the widening of the capacitance step with respect to temperature as shown in (b).*

suming interface defects or an inversion layer, the charge modulation due to the small ac bias voltage occurs at the absorber SCR edge and at the absorber/buffer interface. In that case the capacitance is given by [128]

$$C_{lf} = \frac{\epsilon_R \epsilon_0}{x_p}. \tag{5.71}$$

If the interface defect or the transport of electrons through the buffer layer cannot follow the ac bias voltage, the charge modulation does no longer occur at the absorber/buffer interface but on the n-type doped side of the junction and consequently reads [128]

$$C_{hf} = \frac{\epsilon_R \epsilon_0}{x_p + x_n}, \tag{5.72}$$

where x_n is the position of the charge modulation at the n-side of the junction. Also it is assumed that all the involving layers have the same dielectric constant ϵ_R. Consequently, a capacitance step is observed from C_{lf} to C_{hf} when going from low to high frequencies. Assuming the buffer layer to be completely depleted, this extension to the n-side is proportional to the thickness of the buffer layer. From Eqn. (5.71) and (5.72), the extension of the SCR width into the n-side can be calculated and results in [128]

$$x_n = \epsilon_R \epsilon_0 \left(\frac{1}{C_{hf}} - \frac{1}{C_{lf}} \right). \tag{5.73}$$

The results for samples with varying CdS buffer layer thicknesses is presented in section 5.7.2. If the observed capacitance step is due the extension of the SCR width to the n-side of the junction and if the CdS layer is completely depleted, the extension should be proportional to the CdS layer thickness and follow Eqn. (5.73). Fig. (5.13) exemplifies the position of the charge modulation in the case of an inversion layer.

5.4.5. Mobility freeze-out

A mobility freeze out is another reason explaining a capacitance step as it was shown by Reislöhner *et al.* [129]. The capacitance step arises due to a decreasing mobility at low temperatures when hopping conduction prevails. As a consequence of the decreasing mobility, the time constant for the diffusion of carriers prior to the capture process or the time constant for the drift of carriers after emission process exceeds the time constant of the modulation voltage.

Hopping conduction can occur in compensated semiconductors at low temperatures. For a p-type absorber layer this means that part of the acceptors are emtpy of holes as they recombined with electrons from the compensating donors. Conduction then occurs via the partly occupied acceptor states. The diffusion coefficient is then given by [130]

$$D = R^2 p = R^2 \nu_{ph} \exp\left(-2\alpha R - \frac{\Delta E}{kT} \right), \tag{5.74}$$

with R the hopping distance, i.e. the mean distance between two hopping sites, and p the hopping rate per unit time. ν_{ph} is the phonon frequency associated with the hopping process. The exponential term involves two terms: the first one $\exp(-2\alpha R)$ is determined by the overlap of the wavefunctions with the Bohr radius $a_0 = 1/\alpha$. The second term $\exp(-\Delta E/kT)$ is the Boltzmann factor for the energy difference between the two (nearest neighbour) hopping sites.

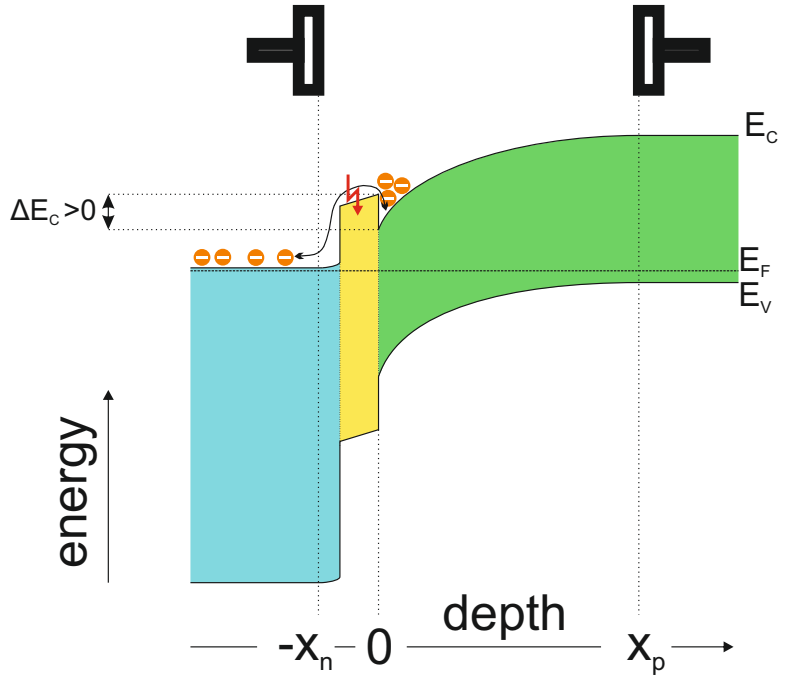


Figure 5.13.: ***Capacitance measurement without transport over CdS layer with an inversion layer*** *- For high frequencies the electron transport over the CdS hindered and thus the charge is modulated at the buffer/window interface and at the SCR edge in the absorber layer as indicated by the parallel plates of the capacitor. For low frequencies the charge transport over the CdS layer is possible and the negative charge can be stored in the inversion layer.*

The energy difference between two hopping sites may arises from a fluctuating potential due to the compensation [131] or also from an energetically distributed defect level.

However, in the model of variable range hopping, the hopping can occur over a much larger distance than R, lets say mR, with $m \gg 1$. Then the hole has m^3 as many possible hopping sites and thus is expected to find a site with an energy closer to its own so that the energy difference is reduced to $\Delta E/m^3$ [131]. The hopping probability can then be written as

$$p = \nu_{ph} \exp\left(-2\alpha m R - \frac{\Delta E}{m^3 kT}\right). \tag{5.75}$$

Eqn. (5.75) has a maximum if the term in the exponent has a minimum, which occurs for [131]

$$m = \left(\frac{3\Delta E}{2\alpha R kT}\right)^{1/4}. \tag{5.76}$$

Inserting Eqn. (5.76) into Eqn. (5.75) results in a hopping probability of

$$p = \nu_{ph} \exp\left(-const.\,(\alpha R)^{3/4}\,(\Delta E/kT)^{1/4}\right). \tag{5.77}$$

Thus, the diffusion constant can be written as

$$D = D_0 \exp\left(-\frac{B}{T^{1/4}}\right), \tag{5.78}$$

where D_0 is weakly temperature dependent ($D_0 \propto T^{1/2}$) and B a constant containing the density of states at the Fermi level [130, 132].

As it was shown by Reislöhner *et al.* [129], in the case of a mobility freeze-out the inflection frequency of the capacitance step is then proportional to the diffusion constant, i.e.

$$\omega_{infl} \propto D. \tag{5.79}$$

Therefore, instead of an usual Arrhenius diagram as in the case for a deep defect, a plot of $\ln(\omega T^{1/2})$ versus $T^{-1/4}$ needs to be drawn in order to obtain a straight line. The factor $T^{1/2}$ in the logarithm originates from the weak temperature dependence of D_0.

Reislöhner *et al.* [129] suggested that such a capacitance step can even occur before the final freeze-out condition of $\omega CR = 1$ [125] is met. The final drop to the geometrical capacitance then occurs if the condition of $\omega CR = 1$ is fulfilled [129]. The reason for that can either be an on going mobility freeze-out, i.e. a decreasing mobility, or a carrier freeze-out [129].

However, it needs to be pointed out that in the case of hopping conduction the free carriers are already frozen out, i.e. hopping conduction dominates compared to band conduction. If then the diffusivity freezes-out via Eqn. (5.78), charge transport is not possible anymore and only the geometrical capacitance is measured. As a result only one capacitance step is observed. However, compared to a carrier freeze-out, the frequency and temperature dependence of the capacitance step may change.

5.5. On sequentially processed absorbers

In this section I want to present the results obtained from CV and admittance measurements on the sequentially processed solar cells. The absorber layers were grown according to the CAPRI process [84] as described in section 3.2.

5.5.1. Capacitance voltage curves

Fig. (5.14) shows Mott-Schottky plots for 6 different samples measured at room temperature (red squares) and at low temperatures (blue circles). The low temperature value was chosen such that the capacitance reading at 1 kHz is not yet influenced by the low temperature capacitance transition observed in admittance spectroscopy (see section 5.5.2). As described in section 5.1, the data is fitted in small forward bias (solid lines) in order to reduce contributions from deep defect states. According to Eqn. (5.6) the built-in voltage V_{bi} and the doping density N_A of the absorber are obtained. With these two values the SCR capacitance can be calculated by Eqn. (5.6). This calculated value corresponds to the value of the fit of the Mott-Schottky plot at zero bias. These calculated values for the SCR capacitance are further discussed in section 5.5.2 and are helpful for the interpretation of the admittance spectra. The parameters obtained from the CV measurements are summarized in Tab. 5.3

It can be observed that the built-in voltages vary among these samples. However, this scattering in the built-in voltage can be explained by the variation of the doping density as can be seen in Fig. (5.15). For higher doping densities the Fermi level in the bulk of the p-type absorber shifts closer to the valence band, i.e. $E_{fp\infty}$ decreases.

The built in voltage is linked to $E_{fp\infty}$ via [50]

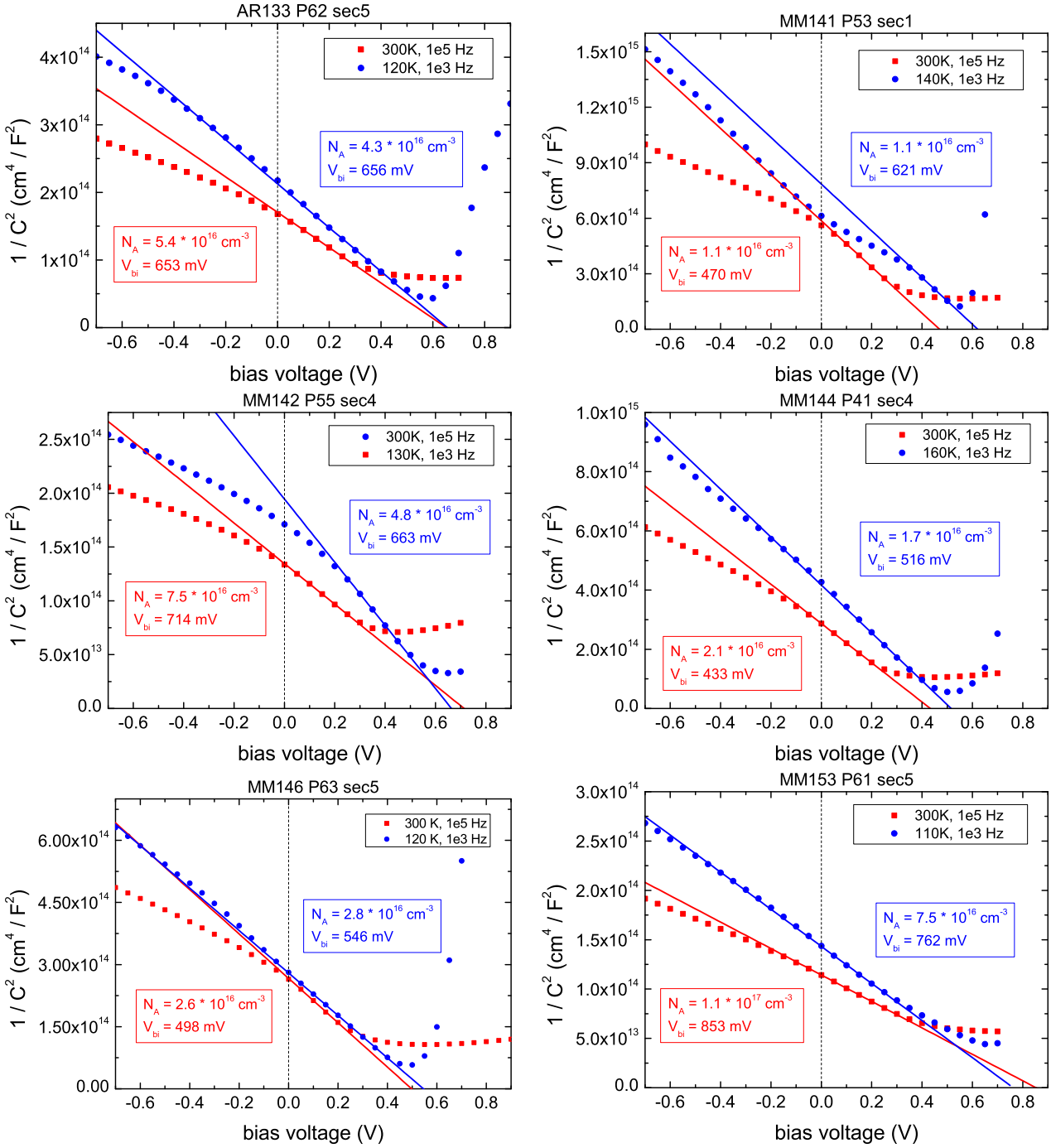


Figure 5.14.: ***Mott-Schottky plots for sequentially processed solar cells*** *- For each sample a CV curve was measured at 300 K (red squares) and at low temperatures (blue circles). A straight line in small forward bias is fitted to obtain the doping density N_A and the built in voltage V_{bi}.*

Table 5.3.: *Deduced values for V_{bi} and N_A from the Mott-Schottky plots shown in Fig. (5.14).*

sample	300 K			low temperature		
	V_{bi} (mV)	N_A (cm^{-3})	C_{SCR} (nF/cm^2)	V_{bi} (mV)	N_A (cm^{-3})	C_{SCR} (nF/cm^2)
AR133 P62 sec5	653	$5.4 \cdot 10^{16}$	76.6	656	$4.3 \cdot 10^{16}$	68.2
MM141 P53 sec1	470	$1.1 \cdot 10^{16}$	40.7	621	$1.1 \cdot 10^{16}$	35.4
MM142 P55 sec4	714	$7.5 \cdot 10^{16}$	86.3	663	$4.8 \cdot 10^{16}$	71.7
MM144 P41 sec4	433	$2.1 \cdot 10^{16}$	58.6	516	$1.7 \cdot 10^{16}$	48.3
MM146 P63 sec5	498	$2.6 \cdot 10^{16}$	60.8	546	$2.8 \cdot 10^{16}$	60.3
MM153 P61 sec5	853	$1.1 \cdot 10^{17}$	95.6	762	$7.5 \cdot 10^{16}$	86.5

$$qV_{bi} = E_g - E_{fp\infty} - E_{fn\infty} + \Delta E_C. \tag{5.80}$$

$E_{fn\infty}$ is the distance of the Fermi level from the conduction band in the bulk of the n-type semiconductor and ΔE_C is the conduction band offset. $E_{fp\infty}$ can be expressed by the free carriers as

$$N_A = p = N_V \exp\left(-\frac{E_{fp\infty}}{kT}\right). \tag{5.81}$$

where it was assumed that all doping acceptors are ionized. Solving Eqn. (5.81) for $E_{fp\infty}$ and inserting it into Eqn. (5.80) yields

$$qV_{bi} = E_g - E_{fn\infty} + \Delta E_C + kT \ln \frac{N_A}{N_V} \tag{5.82}$$

$$= E_g - E_{fn\infty} + \Delta E_C - kT \ln N_V + kT \ln N_A \tag{5.83}$$

Eqn. (5.83) points out that the built-in potential is linearly dependent on $\ln N_A$ with a slope of kT. Fig. (5.15) shows a plot of the built-in voltage versus the doping density. A linear behaviour is observed with a smaller slope for low temperatures than for room temperature measurements as predicted by Eqn. (5.83). The open symbols indicate data points which deviate from the linear behaviour and were excluded for the linear fit. Additionally, it needs to be noted that the data points for low temperatures were not recorded all at the same temperature, but nevertheless in a close temperature range (110 K - 160 K, c.f. Fig. (5.14)). This could result in some scattering of the data points. The fitted thermal energy kT_{fit}, which is obtained from the slope of the fit exceeds the actual experimental thermal energy, which is 26 meV and 11 meV for the measurement at room temperature (300 K) and at low temperatures (130 K), respectively. Thus, there needs to be another dominating effect causing the increase of the built-in voltage with respect to the doping density. However, this issue was not further investigated in the framework of my thesis.

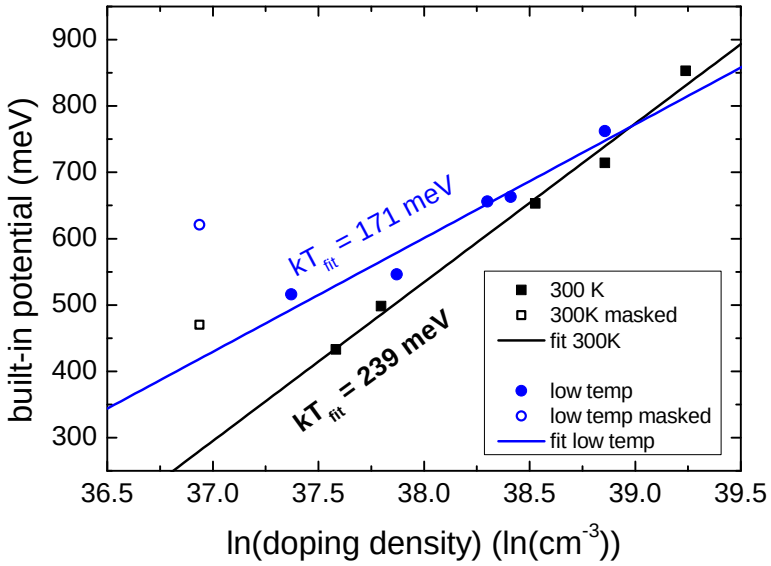


Figure 5.15.: ***Impact of the doping on the built-in voltage*** *- If the doping density increases, $E_{fp\infty}$ decreases and thus, the built-in voltage increases. Built-in voltages and doping densities were estimated by CV measurements at 300 K (black squares) and at low temperatures (blue circles).*

5.5.2. Admittance

Fig. (5.16) shows the capacitance spectra for the same six sequentially processed solar cells as presented in section 5.5.1. All of these spectra can be characterized by a high temperature capacitance transition spanning the whole frequency range and a low temperature capacitance transition. The dashed red and blue lines indicate the calculated SCR capacitance from 300 K and low temperature CV measurements (see section 5.5.1). These values deduced from CV measurements indicate that the SCR capacitance is located above the low temperature capacitance transition.

The derivative $-f\frac{\mathrm{d}C}{\mathrm{d}f}$ of the capacitance spectrum shown in Fig. (5.17) exposes a main peak with a shoulder at higher frequencies. This indicates that the capacitance transition at low temperatures consists of two capacitance steps. As the high frequency step is only represented as a shoulder and does not show a distinct maximum it becomes evident that these capacitance steps overlap. This fact is additionally visible in the C-f graphs as there is no plateau between these two capacitance steps. Throughout this thesis the whole capacitance drop at low temperatures is denoted with "low temperature transition", while the notation of "capacitance step" implies one specific step, for example one of the two low temperature capacitance steps. The origin and the evaluation of these overlapping capacitance steps if further discussed in the next section 5.5.2.1

The high temperature capacitance transition covers the whole measured frequency range. It is characterized as a monotonic increase in capacitance with decreasing frequency and increasing temperature. Such a transition was already observed in CdTe based solar cells and could be modelled by SCAPS 1d as a deep broad defect distribution [121]. The impact of this deep defect distribution on the solar cell performance is discussed in detail in section 5.5.2.2.

Within this thesis, the capacitance steps are sometimes referenced by numbers. The high temperature capacitance step is referred to as the capacitance step 3, while the low temperature

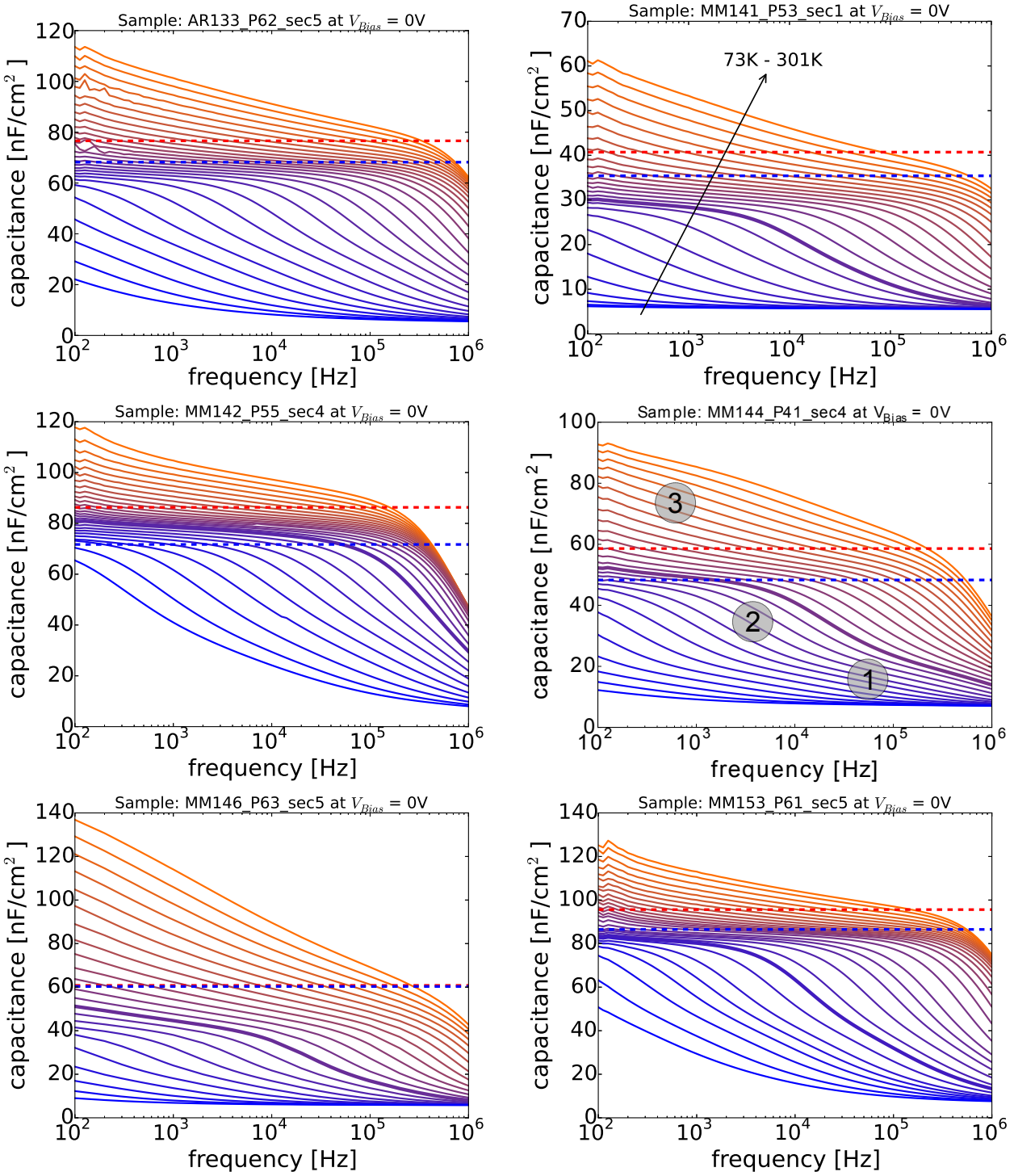


Figure 5.16.: ***Capacitance spectra for sequentially processed solar cells*** *- Shown is the frequency dependence of the capacitance for several temperatures. Red and blue dashed lines indicate the calculated SCR capacitance from CV measurements for 300 K and for low temperatures, respectively. Thick solid line represents the C(f) curve, which was measured at the same temperature as the low temperature CV curve.*

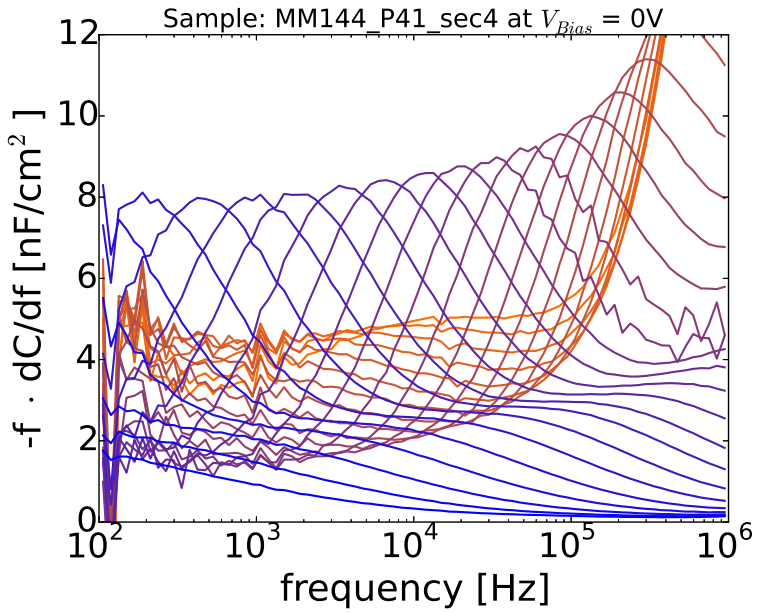


Figure 5.17.: ***Derivative of a capacitance spectrum*** *- Each capacitance step in the C-f plot is represented as a peak in the plot of the derivative. The shoulder at higher frequencies and low temperatures indicates that the low temperature transition actually consist of two capacitance steps.*

capacitance transition is made up by the capacitance steps 1 and 2. The assignment of the numbers to the capacitance step is visualized in Fig. (5.16) for a sample where the individual steps are clearly visible.

5.5.2.1. Evaluation of the low temperature capacitance transition

In section 5.5.2 it has been pointed out that both of the low temperature capacitance steps occur below the SCR capacitance and thus cannot be attributed to a deep defect. However, the functional behaviour of a carrier freeze-out and that of a back barrier are quite similar to that of a deep defect, as it was shown in section 5.4. Therefore, in the following I will evaluate the low temperature capacitance steps as if the inflection frequencies arise from a thermally activated behaviour.

In order to evaluate the (two low temperature) capacitance steps, three different methods are available.

1. An Arrhenius plot of the inflection frequencies can be made, where the slope of such a graph results in the activation energy and the intercept with the ordinate in the attempt to escape frequency (weak temperature dependence is neglected), as described in section 5.2.1. However, this is only possible if distinct maxima in the derivative of the capacitance are visible. Since these two capacitance steps overlap and one of the steps is only visible as a shoulder, this approach is only possible for one of the steps. Also, this approach does not give any information about the capacitance drop which could be used to calculate the defect density.

2. The Walter analysis allows for plotting the defect distribution with respect to the energy.

As shown in Fig. (5.6), by choosing the correct attempt to escape frequency ν_p, it is also possible to make the curves align at the shoulder. Thus, with this method it is possible to determine the defect energies and the attempt to escape frequencies. Even though the capacitance steps overlap, the defect energies can be determined quite accurately, while the contributions cannot be evaluated correctly in this case (see section 5.3.3).

3. The fitting routine yields the correct attempt to escape frequencies and defect energies, as well as it aligns the maxima of the fit with the measured maxima of the derivative. Also the correct contributions from each capacitance step are governed, as the complete spectrum is fitted simultaneously. Thus, in order to draw any conclusions about the individual drop in capacitance or defect densities, the fitting routine needs to be applied, while for the assessment of the defect energy (and attempt to escape frequency) also the Walter method can be used.

For the following analysis, the Walter method is used to estimate the defect energies. As it is shown in Fig. (5.6), the lower energetic capacitance step is still visible as a shoulder in the representation of the scaled derivative versus energy. From that plot the position of the peak maximum can be deduced by fitting the curves with a Gaussian distribution.

As it was pointed out in section 5.4.1 the series resistance can have a strong influence on the capacitance measurement and therefore needs to be considered for the interpretation of the capacitance spectrum. The series resistance was deduced from IVT measurements and it was demonstrated that the series resistance is thermally activated (see section 6.2).

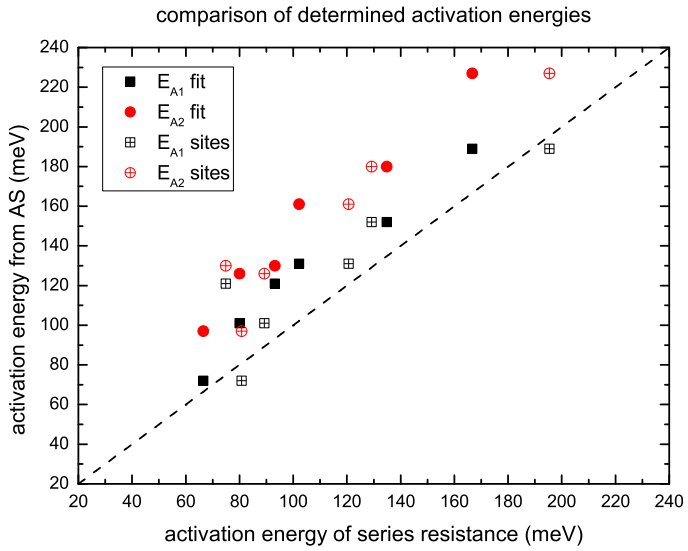


Figure 5.18.: ***Comparison of activation energies from admittance spectroscopy and the series resistance*** *- Black squares and red circles denote the activation energies deduced from admittance spectroscopy of the capacitance step 1 and 2, respectively. Solid and open symbols denote the activation energies for the series resistance deduced from the iv-fit routine and the Sites method, respectively.*

Fig. (5.18) compares the deduced activation energies from the series resistance with the activation energies of the two low temperature capacitance steps (for the sequentially processed

samples). From the admittance measurements two capacitance steps are observed resulting in two activation energies named E_{A1} (black symbols) and E_{A2} (red symbols), where E_{A1} denotes the capacitance step with the lower energy, corresponding to the step at higher frequencies (or lower temperatures) (see Fig. (5.16)). The series resistance was deduced by two different methods: the Sites method [71, 72] (open symbols) and the iv-fit routine [70] (full symbols). From Fig. (5.18) it becomes clear that there is a correlation between the activation energy of the series resistance and the activation energies deduced from admittance spectroscopy. However, as E_{A1} is closer to the activation energy of the series resistance, I have attributed in Ref. [43] the last capacitance step to the series resistance.

Another approach can be used to see the influence of the series resistance on the admittance spectrum, by calculating the frequency, until which the measured capacitance is not yet influenced by the series resistance according to Eqn. (5.57) and as I have shown in Ref. [122]. From Eqn. (5.57) the measured capacitance is obtained from the imaginary part and is

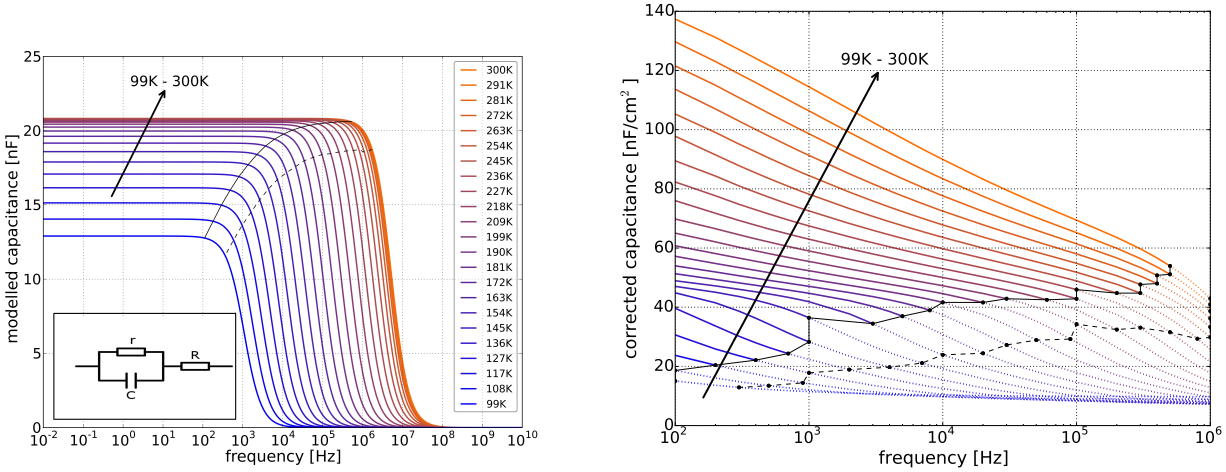
$$C_{\mathrm{meas}} = \frac{C_{lf}}{\left(1 + \frac{r_S}{R_{sh}}\right)^2 + (\omega r_S C_{lf})^2}. \tag{5.84}$$

C_{lf} denotes the low frequency capacitance and is the value just above the low temperature capacitance transition. With the values for the series and the shunt resistance, the capacitance response from the equivalent circuit can be calculated as it is shown in Fig. (5.19a) using a value of $C_{lf} = 41.2\,\mathrm{nF/cm^2}$. The solar cell area is $0.51\,\mathrm{cm^2}$. The temperature dependent values for the shunt and the series resistance are taken from IVT measurements. As seen from Fig. (5.19a), the response of the circuit lies well inside the measured frequency range (between 1e2 Hz and 1e6 Hz) and thus distorts the measured capacitance values. For each temperature the solid and dashed black lines indicate the frequency, where the measured capacitance deviates from C_{lf} by 1 % and by 10 %, respectively. These frequencies are also noted in the corresponding capacitance spectrum shown in Fig. (5.19b). As it is clearly visible in Fig. (5.19b), these frequencies lie directly in the low temperature capacitance step. Thus, the low temperature capacitance transition is in fact influenced by the series resistance. In connection with the comparison of the activation energies (see Fig. (5.18)), it can be stated that the energetic lowest lying capacitance step is due to the series resistance. Therefore, the assignment of this capacitance step to a deep defect is excluded. A further discussion is given in section 5.7.

The other capacitance step number 2 was not attributed so far. A discussion about an inversion layer or an interface defect is given in section 5.7.2, where the CdS buffer layer thickness was varied. Also a mobility freeze-out is a reasonable explanation as elucidated in section 5.7.1.

5.5.2.2. Evaluation of the high temperature capacitance transition

I now turn to the high temperature capacitance transition, which spans the complete frequency range at elevated temperatures. This transition shows generally no inflection frequency and therefore it is impossible to make an Arrhenius plot. The Walter method cannot be applied either as it is difficult to align the curves with the correct attempt to escape frequency. Hence, in order to quantify this transition the fitting routine is applied. The high temperature capacitance transition is well fitted with a Gaussian broad deep defect distribution, as can be seen for sample AR133 P62 sec5 in Fig. (5.9). The fit parameters for the six capacitance spectra shown in Fig. (5.16) are listed in Tab. 5.4



(a) Response of circuit shown in Fig. (5.10b) *(b) cirtical frequencies in capacitance spectrum*

Figure 5.19.: ***Effect of series resistance on admittance spectrum.*** *- The solid and dashed lines indicate a derivation from the low frequency capacitance of 1 % and 10 %, respectively, as calculated according to Eqn. (5.84). Data was analysed for sample MM146 P63 sec5.*

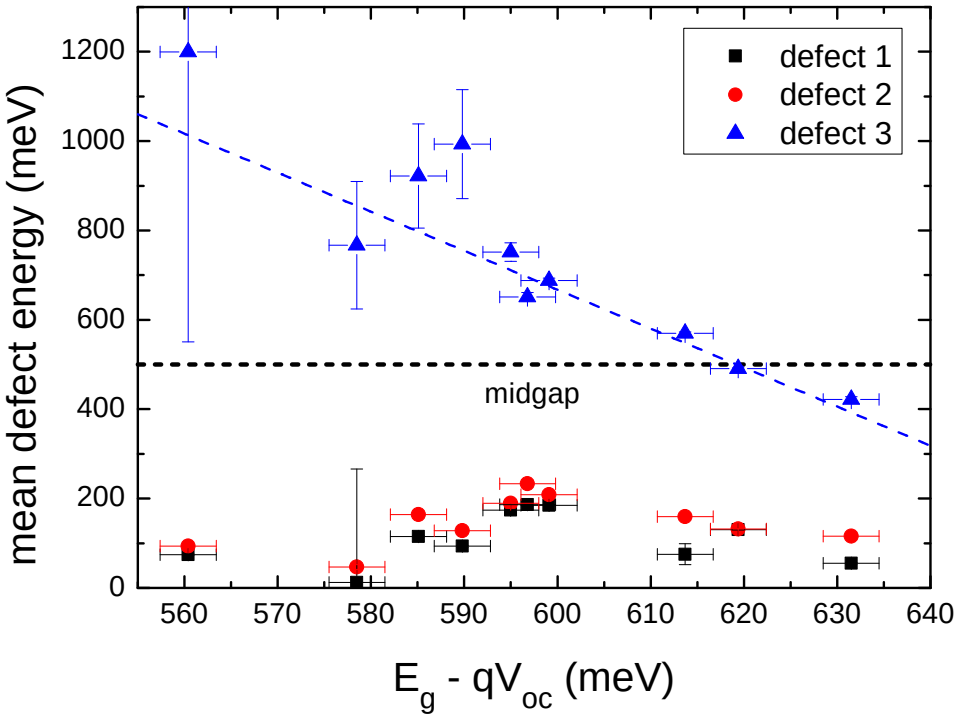


Figure 5.20.: V_{oc} ***deficit versus mean defect energy*** *- While no correlation between the V_{oc} deficit and the two lower energetic defect levels is observed, there is a clear correlation with the broad deep defect distribution. The closer the mean energy of the deep defect distribution shifts to the valence band, the higher is the V_{oc} deficit.*

Table 5.4.: *Parameters for fitting the capacitance spectra shown in Fig. (5.16) with three Gaussian defect distributions.*

parameter	unit	AR133	MM141	MM142	MM144	MM146	MM153
E_{A1}	meV	117	175	78	130	186	93
ν_1	s^{-1}	1.0e10	1.2e11	3.2e9	9.8e9	5.6e10	2.7e9
σ_1	meV	21.1	19.3	19.0	36.1	25.0	19.6
ΔC_1	nF/cm^2	41.6	12.8	48.6	27.3	19.8	50.3
E_{A2}	meV	164	190	92	132	234	128
ν_2	s^{-1}	9.6e10	1.4e11	2.3e9	1.1e9	5.5e11	9.6e9
σ_2	meV	2.8	0.68	2.7	7.4	1.9	1.9
ΔC_2	nF/cm^2	10.7	3.1	13.5	13.8	8.7	21.0
E_{A3}	meV	896	752	1233	491	651	993
ν_3	s^{-1}	2.1e13	1.1e13	7.2e11	1.4e13	6.0e13	2.0e12
σ_3	meV	325.9	237.8	549.7	109.9	197.2	363.7
ΔC_3	nF/cm^2	240.7	132.6	647.8	53.1	213.0	352.8

A deep defect close to midgap acts as an effective Schockley-Read-Hall recombination centre [44] which has a detrimental impact on the quasi Fermi level splitting [45] and limits the V_{oc} [50]. Fig. (5.20) shows a plot of the fitted mean defect energies with respect to the open-circuit voltage deficit $E_g - qV_{oc}$. The bandgap was estimated by linearly fitting the long wavelength slope of the EQE graph. The given error bars for the defect energies are taken from the fit errors. Errors for $E_g - qV_{oc}$ can either occur by measuring the V_{oc} or by the extrapolation of the long wavelength regime of the EQE. As seen from Fig. (5.20), a clear correlation between the V_{oc} deficit and the mean defect energy of the deep broad defect distribution exists. This correlation also suggests that the capture cross sections for electrons and holes might not be equal. If the capture cross sections were equal, the recombination rate and hence also the V_{oc} deficit take their maximum for a defect at midgap. However, as the highest V_{oc} deficit is observed for a defect below midgap, i.e. closer to the valence band, it could be concluded that the electron capture cross section is higher than the hole capture cross section. However, it needs to be stressed that there is only one data point with a defect energy below the midgap position. Thus, in order to draw a more reliable conclusion about the capture cross sections, more data points are needed in this energy range.

For the two lower energetic capacitance steps no correlation with the V_{oc} deficit could be deduced.

With the above mentioned correlation of the V_{oc} deficit with the fitted mean defect energy it can be concluded that the high temperature capacitance transition is due to a deep broad defect distribution. This hypothesis is backed up by the literature where such a transition in CdTe was already attributed to a deep defect level [121].

Still, one important point to discuss is the high mean defect energies for low V_{oc} deficits.

As an example the sample MM142_P55_sec4 is taken, whose capacitance spectrum is shown in Fig. (5.16) and which was fitted with a mean defect energy of 1233 meV (see Tab. 5.4), which is not reasonable for an absorber with a bandgap energy of 1.0 eV. From Fig. (5.16) the high temperature capacitance transition can be described by an increasing capacitance with decreasing frequency, as pointed out before. However, also the derivative of the capacitance is increasing with decreasing frequency, meaning that there is no inflection frequency for this transition within the measured frequency and temperature range. Thus, only the tail of the defect distribution is sampled, which renders the determination of the maximum of the Gaussian distribution erroneous - visible by the large fitting error in Fig. (5.20). Especially, the fitted attempt to escape frequency is small for such a deep defect distribution, meaning that only small energies are sampled according to Eqn. (5.45). Using a minimal frequency of 100 Hz and a temperature of 320 K, the maximal sampled defect energy evaluates to $E_{100Hz}(320K) \approx 594\,\text{meV}$, which proves that only the tail of the distribution is fitted. Consequently, the spectrum could also be described with an exponential tail from one of the band edges, such as

$$N(E) = \frac{N_0}{kT^*} \frac{1}{1 - \exp\left(-\frac{E_g}{kT^*}\right)} \exp\left(-\frac{E_g - E}{kT^*}\right). \tag{5.85}$$

Eqn. (5.85) describes an exponential defect distribution from the conduction band, which interacts with holes from the valence band. kT^* is the characteristic energy with which the defect distribution decreases towards midgap. The prefactors in front of the exponential term are included so that the distribution is normalized and yields a total number of defect states per unit volume of N_0. Fig. (5.21) compares the fitted spectra of the sample MM142_P55_sec4 using a deep defect distribution (upper graph) and using a bandtail from the conduction band (lower graph). Note that admittance spectroscopy cannot distinguish between electron and hole traps.

As seen from Fig. (5.21), the spectra are fitted similarly well. For both fits the weight of the capacitance and its derivative was taken to be $w_C = 1$ and $w_d = 2$. The S value (Eqn. (5.55)) after the fit with a Gaussian distribution is $9.3 \cdot 10^{-19}$, while for the fit with a bandtail a slightly better fit is achieved with a S value of $8.6 \cdot 10^{-19}$. Fig. (5.21) shows that the spectrum could therefore also be fitted with a bandtail. The characteristic energy for the fit of the bandtail is $kT^* \approx 252\,\text{meV}$.

The reason for using a Gaussian distribution is that in some spectra the levelling off of the capacitance with low frequencies and high temperatures is observed, as for example for sample MM144_P41_sec4 (see Fig. (5.16)). However, even though the capacitance levels off at these frequencies and temperatures, the origin does not need to be the absence of defects at the sampled energies. Another reason might be that the sampling energy lies above $E_{fp\infty} + V_{bi}$. Thus the defect level does not cross the Fermi level anymore and does not contribute to the capacitance, as described in section 5.3.2.

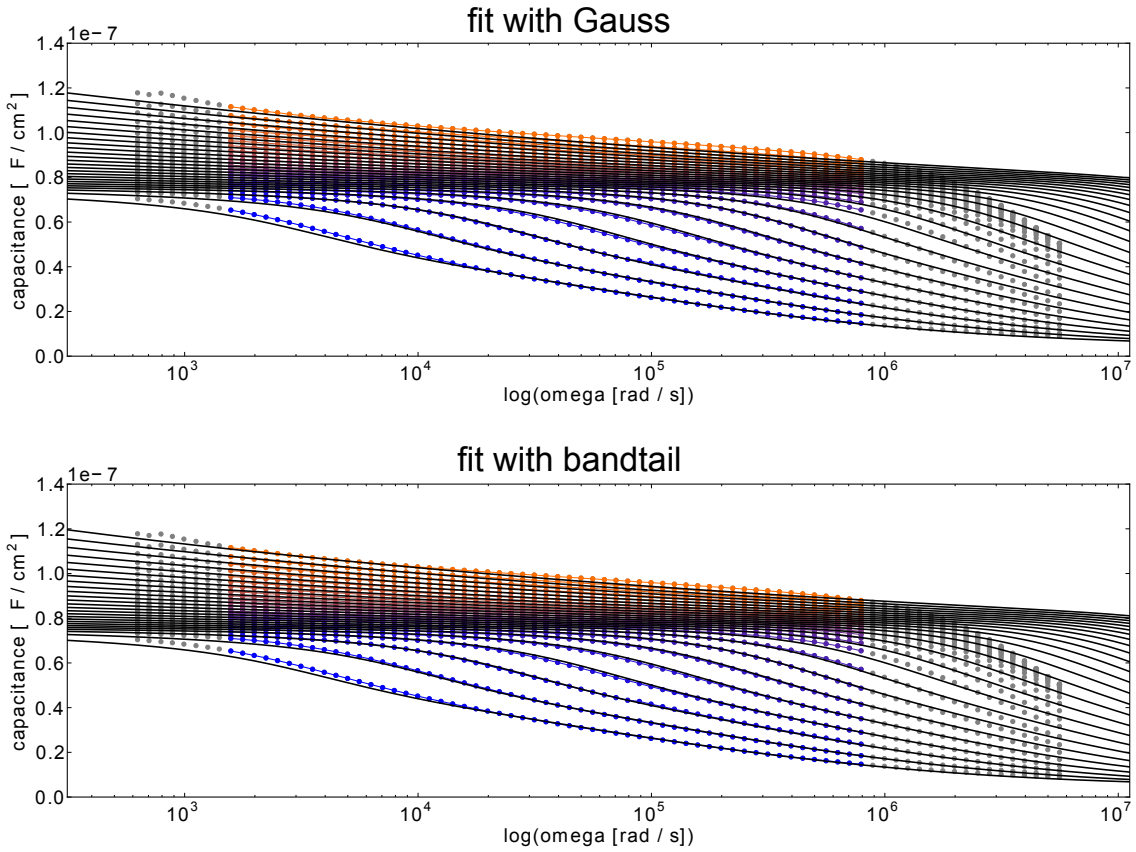
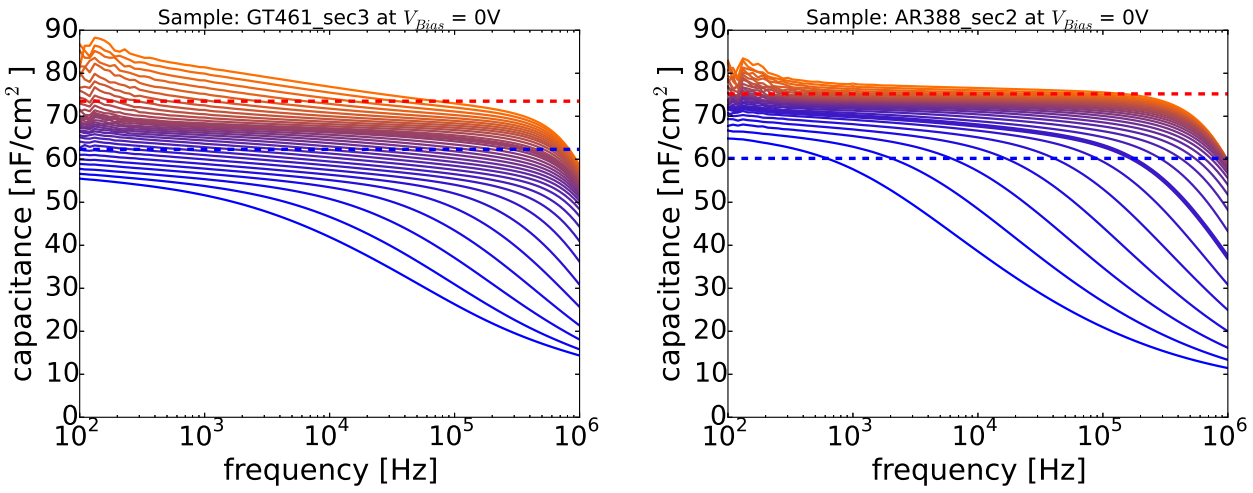


Figure 5.21.: ***Comparison of fitting results for a bandtail and a Gaussian distribution*** - *Both figures show a similar good fit to the measured capacitance data. However, a slightly better fit could be achieved using a bandtail with a S-value of* $8.6 \cdot 10^{-19}$ *compared to a S-value of* $9.3 \cdot 10^{-19}$ *for the fit with a Gaussian distribution.*

5.6. On co-evaporated absorbers

Section 3.3 presented the growth of absorber layers via a high temperature co-evaporation process. These samples differ in their electronic properties from the ones grown by the sequential process. However, the results from section 5.5 can be used to understand the capacitance spectra of the co-evaporated devices more readily. A problem of the high temperature co-evaporated absorber layers is that they exhibit a high doping, which is discussed in section 5.6.1. The doping density can be reduced by an additional low temperature heat treatment and leads to improved collection properties. This will be subject of section 5.6.2.

5.6.1. As grown absorber layers



(a) from single-stage process

(b) from multi-stage process

Figure 5.22.: ***Capacitance spectra from devices with as grown co-evaporated absorbers*** *- The low temperature capacitance transition is similar for both samples. However, the sample from the single stage process shows to a small extent also the high temperature capacitance transition. This transition was only measured on a few samples. Thick line indicates the temperature, where the CV measurement at low temperatures was carried out. CV measurements for these two samples are shown in section D.1, Fig. (D.1).*

For the sequentially processed absorbers, the low temperature capacitance transition always consists of two overlapping capacitance steps, characterized by a clear shoulder in the spectrum of the derivative of the capacitance. However, this is generally not the case for the co-evaporated samples.

Some of these samples show a double capacitance step, as for example one of the as grown samples shown in Fig. (5.24) (graph on the bottom left). However, this clear double capacitance step is only observed for a few co-evaporated samples. For the other samples this double capacitance step cannot be clearly observed due to two reasons:

First, only the onset of the low temperature capacitance transition is observed (see Fig. (5.22)). This means that even if it is possible to deduce the inflection frequencies for the lowest temperatures, the high frequency sides of their peaks in the derivative are not completely visible,

since they lie outside the measured frequency range. Therefore, it is not possible to observe a potential shoulder in the derivative.

For some samples, the complete peak (of the derivative) lies inside the measured frequency range. However, no clear shoulder is observed. This peak in the derivative is for some samples symmetric and therefore indicates clearly only one capacitance step. However, for some other samples the peak appears a bit asymmetric either to higher or to lower frequencies. Thus, the existence of a second capacitance step cannot clearly be revealed for many samples and hence not ruled out.

Typical capacitance spectra of solar cells finished from as grown absorber layers are shown in Fig. (5.22). Fig. (5.22a) and Fig. (5.22b) refer to absorber layers grown by a single- and a multi-stage process, respectively (see Ref. [19] and section 3.3 for the growth process).

These two spectra have in common that they do not exhibit a pronounced low temperature capacitance step, which is a common characteristic of the sequentially processed solar cells, as mentioned in section 5.5.2. From an Arrhenius plot of the low temperature capacitance transition of the sample shown in Fig. (5.22a) an activation energy of $E_A \approx 19\,\mathrm{meV}$ can be deduced. Following the interpretation from literature [31] and assigning the last capacitance step to a carrier freeze-out, results in a doping acceptor state with an activation energy of 19 meV. This activation energy is much smaller compared to those for the sequentially processed solar cells and therefore points to a different doping acceptor state. However, there are also hints that this capacitance step arises due to a mobility freeze-out, which is further discussed in section 5.7.

The high temperature capacitance transition in these samples is almost absent when compared to the sequentially processed absorbers. Still, a continuous rise of capacitance with decreasing frequency is observed for the sample originating from the single stage process. This transition at high temperatures was only observed for a few samples grown by the single stage process (c.f. Fig. (5.22a)). These few samples were grown immediately after the MBE chamber was used for CIGSe deposition and could possibly result from the incorporation of impurities as the chamber was not perfectly clean. Samples deposited at a later time did not show this transition anymore. The exact origin of this deep defect distribution (or bandtail) is not known so far.

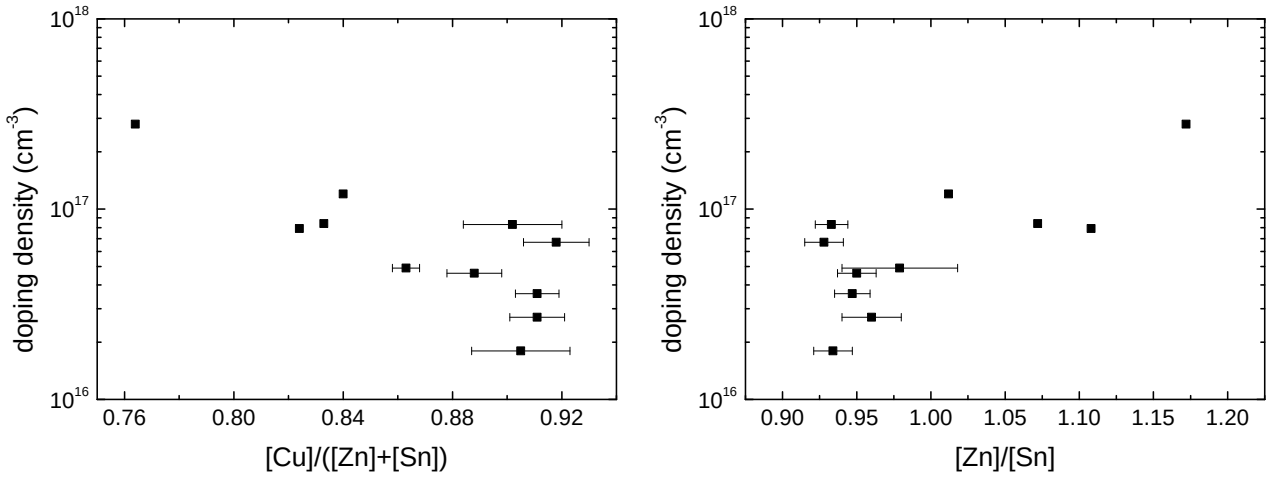
The doping density and the built-in voltage was determined from CV measurements in the same way as for the sequentially processed solar cells. The calculated SCR capacitance is noted in Fig. (5.22) as a blue and a red dashed line for cold and room temperature CV measurements. From these values of the SCR capacitance it is clear that the SCR capacitance is situated above the low temperature capacitance transition also for the co-evaporated samples.

Fig. (5.23) shows the doping densities for various co-evaporated samples with the single- and the multi-stage process. Fig. (5.23a) indicates that the more Cu-poor the absorber layer is, the higher is the doping density showing the opposite trend as found by Gunawan *et al.* [133]. However, there is still a large scatter for absorber layers with a [Cu]/([Zn] + [Sn]) ratio between 0.9 and 0.92. Comparing the doping density with the [Zn]/[Sn] ratio (Fig. (5.23b)), it is found that the sample with the highest [Zn]/[Sn] ratio yields the highest doping density in accordance to the findings of Brammerts *et al.* [134]. However, apart from this datapoint no correlation can be deduced and again a large scattering around a [Zn]/[Sn] ratio of 0.95 is observed. A complete comparison between growth parameters and the doping density was not yet performed.

For solar cell devices, it is desirable to achieve a doping density which does not exceed $1 \cdot 10^{16}\,\mathrm{cm}^{-3}$ [50]. For higher doping densities, tunnelling enhanced recombination gets severe

Table 5.5.: *Deduced values for V_{bi} and N_A from CV measurements for the two samples shown in Fig. (5.22).*

sample	300 K			low temperature		
	V_{bi} (mV)	N_A (cm^{-3})	C_{SCR} (nF/cm^2)	V_{bi} (mV)	N_A (cm^{-3})	C_{SCR} (nF/cm^2)
GT461 sec3	885	$6.7 \cdot 10^{16}$	73.5	834	$4.6 \cdot 10^{16}$	62.3
AR388 sec2	990	$7.9 \cdot 10^{16}$	75.2	711	$3.6 \cdot 10^{16}$	60.2



(a) Doping density versus [Cu]/([Zn] + [Sn]) ratio. *(b) Doping density versus [Zn]/[Sn] ratio.*

Figure 5.23.: ***Doping density versus composition*** *- Doping densities were determined from low temperature CV measurements. The samples originate from the single- and multi-stage co-evaporation process.*

and deteriorates J_0 and therefore V_{oc}. Additionally, a smaller SCR is detrimental for the field assisted collection of charge carriers. In the following section I will describe an annealing procedure which enables the reduction of the doping density and with that the collection properties of the solar cell device.

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5.6.2. Impact of annealing after co-evaporation

As described in section 5.6.1 the as-grown absorber layers have a too high doping reaching almost values of $1 \cdot 10^{17}\,cm^{-3}$. In this section two different annealing procedures are presented, both capable of reducing the doping density of these absorber films. A consequence of a lower doping is a wider SCR width and a better collection for long wavelength photons, which ultimately increases J_{sc}.

In the following I will consider absorber layers from two different co-evaporation processes. From each process one absorber layer was directly finished to a solar cell device, while another

absorber layer from each process underwent an additional heat treatment prior to solar cell finishing. Two different heat treatments were applied:

low temperature heat treatment The absorber layer was annealed for 18 h under vacuum with a base pressure of $1 \cdot 10^{-8}$ mbar at a temperature of 180 °C.

high temperature annealing treatment The absorber layer was annealed in the same way as the annealing procedure for the sequentially grown absorber layers (see section 3.2). It includes an annealing in a graphite box at 520 °C for approximately 30 minutes in 1 mbar H_2/N_2 with the addition of SnSe and Se.

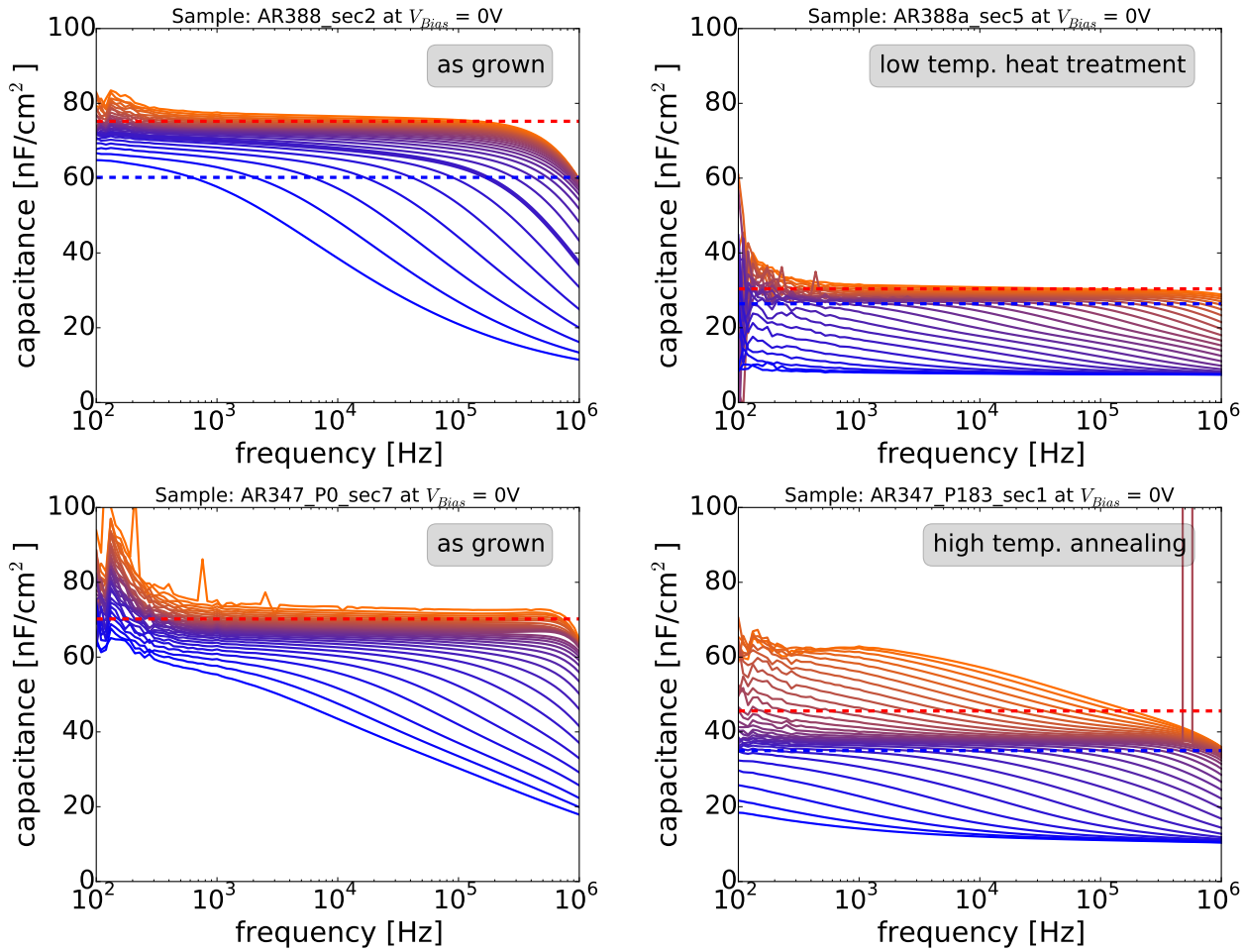


Figure 5.24.: ***Impact of different heat treatments on the capacitance spectrum*** *- Left hand side shows the spectra from the solar cells originating from the as grown absorbers. Right graphs show the spectra after the absorber layers underwent an additional heat treatment. Upper right shows the low temperature heat treatment, lower right the high temperature annealing.*

Fig. (5.24) depicts the admittance spectra for these absorber layers before (left graphs) and after (right graphs) the respective heat treatment. The dashed lines again indicate the calculated SCR capacitance from CV measurements at low temperatures (blue) and at room temperature (red). For sample AR347_P0_sec7 no cold CV measurement could be performed due to contacting problems and therefore only the measured room temperature SCR capacitance is marked.

Table 5.6.: *Deduced values for V_{bi} and N_A from CV measurements for the samples presented in Fig. (5.24).*

	300 K			low temperature		
sample	V_{bi} (mV)	N_A (cm^{-3})	C_{SCR} (nF/cm^2)	V_{bi} (mV)	N_A (cm^{-3})	C_{SCR} (nF/cm^2)
as grown	990	$7.9 \cdot 10^{16}$	75.2	711	$3.6 \cdot 10^{16}$	60.2
low temp. heat treatment	745	$9.7 \cdot 10^{15}$	30.4	698	$6.9 \cdot 10^{15}$	26.4
as grown	1.84	$1.3 \cdot 10^{17}$	70.2	N/A	N/A	N/A
high temp. annealing	1.41	$4.1 \cdot 10^{16}$	45.6	673	$1.2 \cdot 10^{16}$	35.0

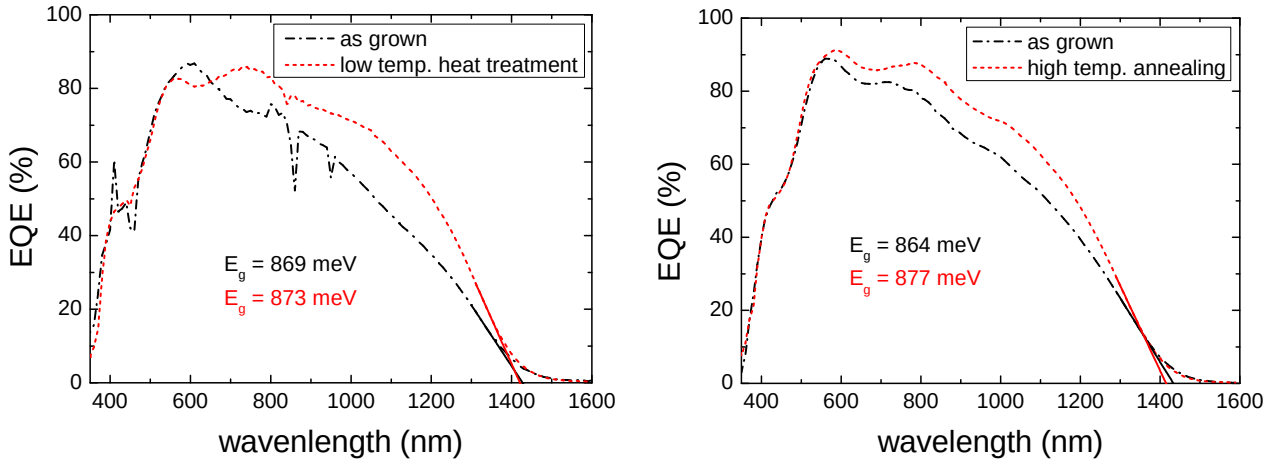
5.6.2.1. Improved collection properties

One observation is that the SCR capacitance significantly drops after the heat treatment, which results from a decrease in the doping density. The built-in voltages and the doping densities are summarized in Tab. 5.6. Due to the lowered doping density, the SCR widens (see Eqn. (2.10)) and therefore the collection properties should increase. The measured EQE for all these four solar cell devices is plotted in Fig. (5.25). Fig. (5.25a) shows the spectra for the as grown (dashed dotted black line) and the low temperature treated (dashed red line) solar cell and similarly shows Fig. (5.25b) the curves for the high temperature annealing and the respective as grown sample. Clearly, the samples, where the absorber layer underwent an additional heat treatment, show a higher EQE response in the high wavelength regime accompanied with a steeper slope towards the bandgap. Thus, these absorber layers have superior collection properties compared to the as grown solar cells.

The bandgap has been deduced by the extrapolation of the linear part at long wavelengths, as indicated by the solid lines in Fig. (5.25). Noticable is a small shift of the bandgap to higher energies after the low temperature heat treatment as well as after the high temperature annealing. These shifts might be due to a small amount of ordering [22]. However, compared to a change in the bandgap of 110 meV between the completely ordered and disordered state [22], this influence of the ordering is neglected.

5.6.2.2. Incorporation of deep defect distribution

Another observation from Fig. (5.24) is that the sample after the high temperature annealing procedure shows the rise of capacitance with decreasing frequency and increasing temperature, which was attributed to a detrimental deep defect distribution as I have shown in section 5.5.2.2 and have published in Ref. [27]. This deep defect distribution was not measured in the as grown sample and is therefore attributed to the annealing process. The V_{oc} for this sample drops after the low temperature heat treatment from 311 mV to 242 mV. This drastic reduction of the V_{oc} can be explained solely by the deep defect distribution. This sample is included in the graph of the V_{oc} deficit versus mean defect energy (Fig. (5.20)) and corresponds to the datapoint with the highest V_{oc} deficit and the lowest mean defect energy. It lies on the line with the already



(a) low temperature heat treatment *(b) high temperature annealing*

Figure 5.25.: ***Impact of annealing on collection properties*** *- EQE spectra before (black dash dotted line) and after (red dashed line) a heat treatment. Solid lines indicate a linear fit to extrapolate the bandgap energy. The spikes in Fig. (5.25a) are due to measurement artefacts.*

existing datapoints. Thus it is concluded that the origin of the deep defect distribution is the same and is attributed to the annealing process usually used for the sequentially processed absorber layers.

5.6.2.3. Low temperature capacitance step

As it was shown in section 5.6.2.1, the doping density decreases after the heat treatment, which is reflected by a lowered SCR capacitance. However, this lowered SCR capacitance comes along with a pronounced capacitance transition, i.e. the drop of capacitance occurs already at higher temperatures. Note that the annealed samples show an almost flat capacitance with respect to frequency at the lowest temperatures. Another change of the capacitance spectrum is that after the high temperature annealing the capacitance transition consists of a double step, similar to the sequentially processed samples. The graphs of the derivative are shown in Fig. (D.2).

The origin of the double capacitance step is still unclear, and will be further discussed in section 5.7. Here, I want to point out the transition of the capacitance drop, which occurs already at higher temperatures. This can be traced back to higher activation energies for both of the low temperature capacitance steps after the heat treatment compared to the activation energy obtained for the as grown samples. The energetic lower lying capacitance step drives the capacitance down to the geometrical capacitance and was so far attributed to a carrier freeze-out [31]. For this capacitance step I measured activation energies above 80 meV for the sequentially processed samples [43]. Following the interpretation of Gunawan *et al.* [31] would imply a change of the doping defect after the heat treatment. The as grown absorber layers have a doping defect situated roughly 20 meV above the valence band. After a heat treatment this 20 meV defect level is absent and the doping defect is an acceptor situated at least 80 meV above the valence band and has a lower density. However, the carrier freeze-out is not the only process which could bring the measured capacitance to the geometrical one. Also a mobility freeze-out [129] might be a possible explanation (see section 5.7).

5.7. Interpretation of the low temperature capacitance transition

5.7.1. Mobility freeze-out

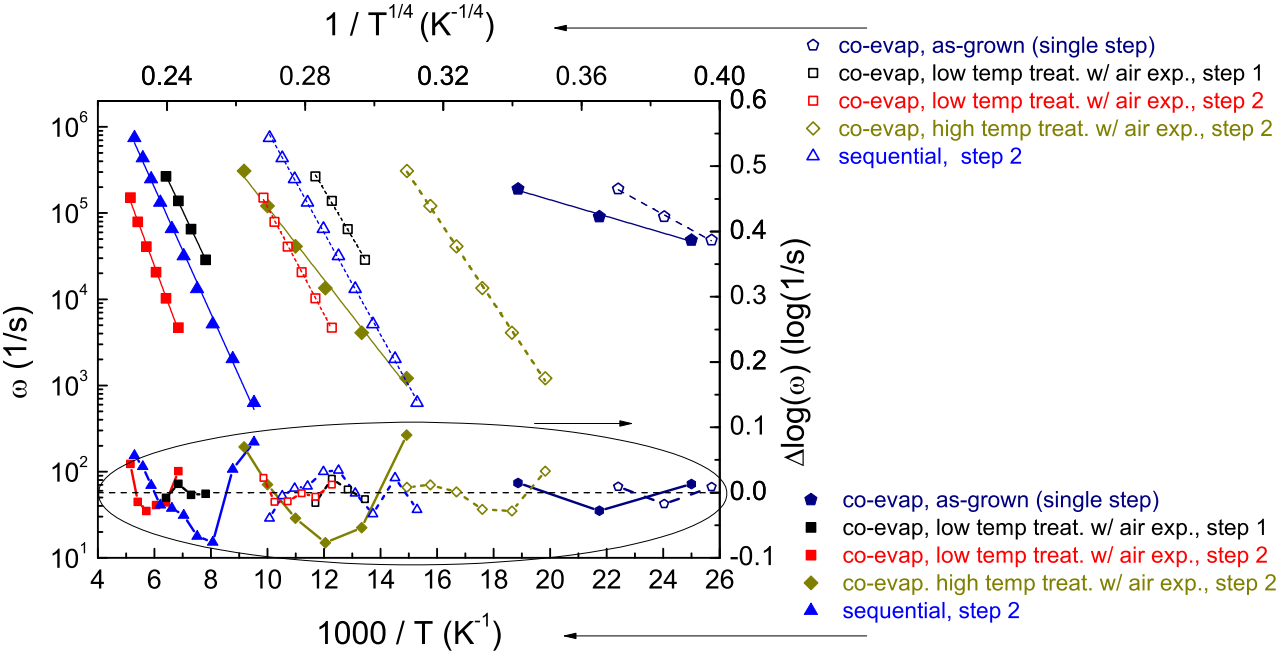


Figure 5.26.: ***Comparison of carrier freeze-out and mobility freeze-out*** *- Plotted are the inflection frequencies (left ordinate) versus a T^{-1} scale (bottom abscissa) and versus a $T^{-1/4}$ scale for a carrier freeze-out and a mobility freeze-out, respectively. The right ordinate shows the residuals for a linear fit indicating a U-shape of the inflection frequencies for the Arrhenius representation (T^{-1} scale) and a straight behaviour for the mobility freeze-out representation ($T^{-1/4}$ scale).*

In section 5.5.2.1 it was shown that for the sequentially processed solar cells the last capacitance step is due to the series resistance. A carrier freeze-out results in a thermally activated series resistance and can explain the drop of capacitance to the geometrical one [31,125], consistent with the observations made for our CZTSe solar cells. However, also a mobility freeze-out could be responsible for the drop of the capacitance to the geometrical one (see section 5.4.5) and the rise of the series resistance at low temperatures, which is subject to this section.

Fig. (5.26) shows the usual Arrhenius representation (bottom abscissa) as well as the representation used in the case of a mobility freeze-out (top abscissa) of the inflection frequencies (left ordinate). The inflection frequencies were taken from the capacitance step 2, which shows a distinct maximum in the derivative. For one sample the capacitance step 1 also showed a maximum in the derivative and the inflection frequencies are plotted in Fig. (5.26) as well.

In the case of a carrier freeze-out, the datapoints on an Arrhenius plot should yield a straight line, while in the case of a mobility freeze-out the datapoints form a bent curve. The datapoints were linearly fitted for the $1/T$ (solid lines) and for the $1/T^{1/4}$ (dashed lines) abscissa and the corresponding residuals were plotted on the right ordinate. From the U-shape of the residuals it becomes obvious that the datapoints plotted in the Arrhenius representation form a bent

curve. For the curves plotted versus the $1/T^{1/4}$ axis, the residuals scatter around zero and thus indicate a straight line for the inflection frequencies. This finding hints that the mobility freeze-out is a possible explanation of the capacitance step 2.

In contrast to Reislöhner *et al.* [129], I have pointed out in section 5.4.5 that the mobility freeze-out results in a drop of the capacitance to the geometrical one and that no final capacitance step can occur due to carrier freeze-out. This means that if the capacitance step 2 is interpreted as a mobility freeze-out the question arises where the final capacitance step stems from. However, it has to be noted that a bent Arrhenius diagram not necessarily results from a mobility freeze-out. Also thermally assisted tunneling through a conduction band spike at the absorber/buffer interface results in a bent Arrhenius diagram [135] and cannot be ruled out at the moment. In this scenario the capacitance step would be due to an interface defect sate.

5.7.2. CdS thickness variation

In section 5.4.4 it was demonstrated that a capacitance step can occur if the SCR on the n side increases. This increase of the SCR can be calculated from the drop of the capacitance according to

$$x_n = \epsilon_R \epsilon_0 \left(\frac{1}{C_{hf}} - \frac{1}{C_{lf}} \right), \tag{5.86}$$

and should correspond to the thickness of the buffer layer (if the buffer layer is completely depleted). This theory can be checked experimentally by measuring the capacitance spectrum of samples with different CdS buffer layer thicknesses. The growth of these samples is presented in section 3.4 and the corresponding IV analysis can be found in section E.1.

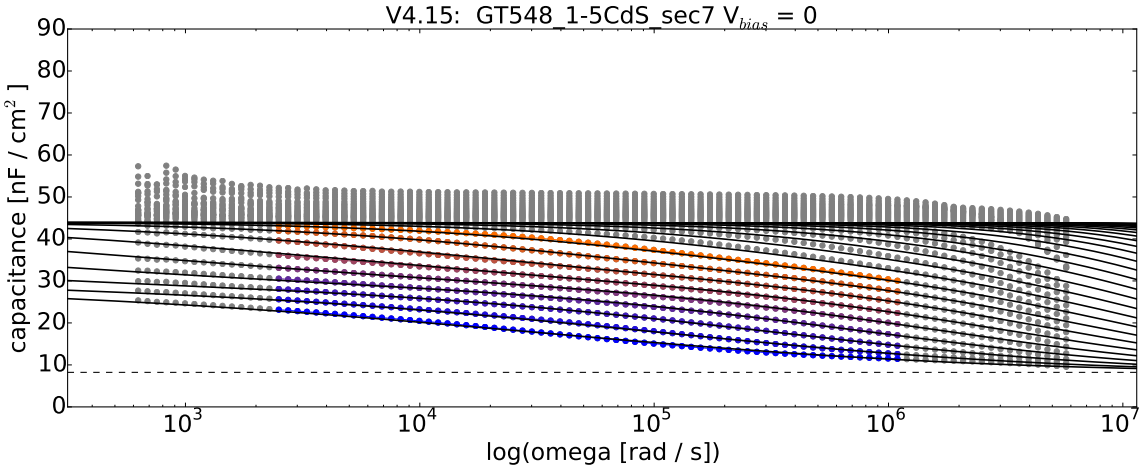


Figure 5.27.: ***Fitted capacitance spectrum from a sample of the CdS thickness series*** *- Coloured circles denote datapoints which are taken into account for the fitting. Note that the high temperature data is not included for the fitting as the capacitance is not frequency dependent at these temperatures.*

A fitted capacitance spectrum of the sample with 1.5 CdS runs is shown in Fig. (5.27). It is fitted with two Gaussian defect distributions to describe the low temperature capacitance transition. The high temperature capacitance data is not frequency dependent and is therefore

not included into the fit (grey data points). The dashed black line shows the fitted geometrical capacitance. A comparison of all four fits of the sample series with 0.5, 1.0, 1.5 and 2.0 CdS runs and their respective fit parameters are presented in section E.2. The fitted values ΔC_2, ΔC_1 and C_{inf} can then be used to calculate C_{hf} and C_{lf} as required for Eqn. (5.86). If capacitance step 1 is responsible for the increase of the SCR width on the n side then $C_{hf} = C_{inf}$ and $C_{lf} = C_{inf} + \Delta C_1$. If capacitance step 2 is the origin then $C_{hf} = C_{inf} + \Delta C_1$ and $C_{lf} = C_{inf} + \Delta C_1 + \Delta C_2$ [5]. x_n from Eqn. (5.86) is then written for step 1 and step 2 respectively as

$$x_{n,1} = \epsilon_R \epsilon_0 \left(\frac{1}{C_{inf}} - \frac{1}{C_{inf} + \Delta C_1} \right) \tag{5.87}$$

$$x_{n,2} = \epsilon_R \epsilon_0 \left(\frac{1}{C_{inf} + \Delta C_1} - \frac{1}{C_{inf} + \Delta C_1 + \Delta C_2} \right). \tag{5.88}$$

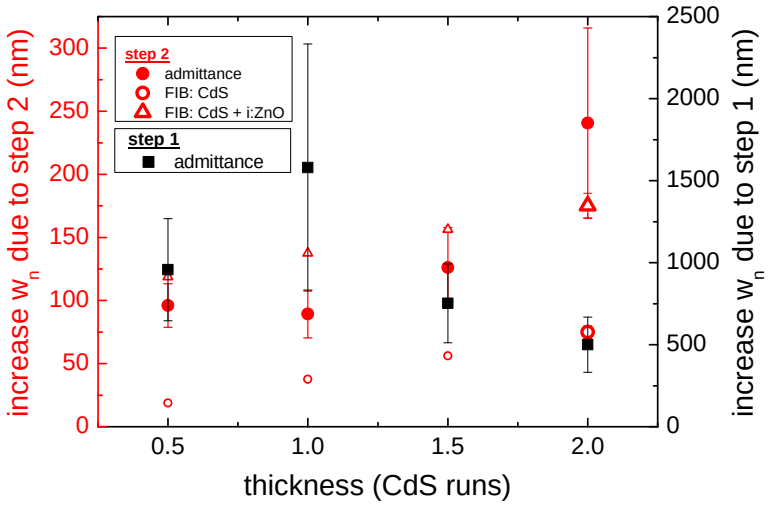


Figure 5.28.: ***Correlation of admittance step with CdS thickness*** *- If the transport over the CdS layer is hindered, the charging and discharging in the n-side shifts from the hetero interface absorber/buffer to the window/buffer interface. From the capacitance drop the shift of the position of the charging/discharging on the n-side can be calculated.*

Using Eqn. (5.86), the expected increase of the SCR width on the n side of the junction are calculated, which is shown in Fig. (5.28). ϵ_R is set to 10 for the calculation. Errors of $x_{n,1/2}$ are calculated according to

$$\Delta x_{n,1} = \epsilon_R \epsilon_0 \sqrt{\left(\frac{\partial x_{n,1}}{\partial C_{inf}} C_{inf}^{err} \right)^2 + \left(\frac{\partial x_{n,1}}{\partial \Delta C_1} \Delta C_1^{err} \right)^2} \tag{5.89}$$

$$\Delta x_{n,2} = \epsilon_R \epsilon_0 \sqrt{\left(\frac{\partial x_{n,2}}{\partial C_{inf}} C_{inf}^{err} \right)^2 + \left(\frac{\partial x_{n,2}}{\partial \Delta C_1} \Delta C_1^{err} \right)^2 + \left(\frac{\partial x_{n,2}}{\partial \Delta C_2} \Delta C_2^{err} \right)^2}. \tag{5.90}$$

[5] Compare Fig. (5.16) for the assignment of the numbers to the capacitance steps

C_{inf}^{err}, ΔC_1^{err} and ΔC_2^{err} are the errors for C_{inf}, ΔC_1 and ΔC_2, respectively and are all assumed to be $2\,\mathrm{nF/cm^2}$.

The capacitance step 1 is ruled out for being the origin of a possible shift of the SCR width as the obtained values (black squares, right scale) are an order of magnitude higher than the expected CdS buffer layer thickness. The values of the increase of x_n calculated from the capacitance step 2 on the other hand (red circles, left scale) are in the same order of magnitude as the thickness of CdS buffer layers. However, these calculated values exceed the nominally thickness of the CdS buffer layers (between 25 nm and 100 nm) by a factor of 2. For the sample with 2.0 CdS runs an cross section has been cut by a focused ion beam (FIB), which is shown in Fig. (2.2b). From that cross section a 75 nm thick CdS buffer layer and a 100 nm thick intrinsic ZnO layer were deduced. These values are added to Fig. (5.28) as a thick open red circle (CdS thickness) and triangle (CdS thickness + i:ZnO thickness). FIB measurements for the other samples are currently still pending. However, the CdS thickness for these samples is derived by assuming a linear growth rate with time (and fixing the thickness to 75 nm with 2.0 CdS runs). This data is shown as small open red circles and triangles).

Thus, from Fig. (5.28) it can be concluded that if the capacitance step is due to an increase of the SCR on the n side, it cannot be explained solely by the CdS buffer layer. One solution could be an extension of the SCR up to the Al:ZnO/i:ZnO interface (open red triangles). But the experimental data is also not conclusive in that case.

5.8. Summary

In this section I want to summarize the results of capacitance measurements on sequentially processed and co-evaporated based CZTSe solar cells. The CZTSe based solar cells generally exhibit two capacitance transitions. One occurs at high temperatures and spans the complete frequency range and the other occurs at low temperatures, which commonly consists of two overlapping capacitance steps. From CV measurements it could be deduced that the SCR capacitance is situated above the low temperature capacitance transition. The two low temperature capacitance steps can therefore not be attributed to a deep defect.

It was shown that the two low temperature capacitance steps cannot correctly and completely evaluated with the common methods found in literature. The problem lies in the overlapping nature of these two capacitance steps. A fitting routine was proposed enabling the simultaneous fitting of the complete capacitance spectrum. It deconvolutes the capacitance steps and yields the correct contribution to the capacitance from each individual step, which is not possible by the Walter analysis.

The assignment of each individual low temperature capacitance step cannot certainly be made as several reasons exist for a capacitance drop below the SCR capacitance.

The final capacitance step (step 1) drops to the geometrical capacitance. From measurements of solar cells with a varying CdS buffer layer thickness (c.f. section 5.7.2) it is excluded that this capacitance step arises from an increase of the SCR on the n side. Therefore, this final capacitance step is attributed either to a mobility freeze-out or carrier freeze-out.

For the second low temperature capacitance step (step 2) I have shown in section 5.7.1 that the Arrhenius plot is generally bent. Reislöhner *et al.* [129] attributed this effect to a mobility freeze-out. However, as discussed above, this step is not likely to arise from a mobility freeze-out (or carrier freeze-out), as these phenomena are more likely to be attributed to the final capacitance step (step 1). However, a bent Arrhenius plot could also be a sign

of thermally assisted tunnelling from interface states through the CdS buffer layer conduction band spike [135]. In the case that the interface defect does not respond anymore, the drop of capacitance should correlate to the increase of the SCR on the n side [127] as described in section 5.4.4. However, as I have shown in section 5.7.2 the increase of the SCR width cannot alone stem from the CdS buffer layer. The experiment suggests the possibility that the intrinsic ZnO layer also adds to the increase of the SCR on the n side in this model. Nevertheless the experimentally deduced values for the thickness of the CdS buffer layer and the intrinsic ZnO layer are not in good agreement with the values deduced from admittance spectroscopy either, even though a trend can be observed. As discussed in section 5.4.3 also a back contact barrier could account for a capacitance step below the SCR capacitance. As no roll-over effect is observed in IVT measurements for the samples presented here (see chapter 6), this possibility is not discussed further.

One intriguing point however is that the activation energies of the two low temperature capacitance steps vary generally simultaneously among the samples as it is shown in Fig. (5.18). Currently this phenomenon is not yet understood, but this correlation implies one physical origin for both of these capacitance steps.

The high temperature capacitance transition could be described and fitted with a broad deep defect distribution which is detrimental to the V_{oc}. A plot of the V_{oc} deficit and the mean depth of the defect distribution showed a clear correlation: with decreasing depth of the defect distribution the V_{oc} deficit increases. It could be shown that this defect distribution is incorporated during the annealing procedure which is used for the sequential process of the absorber growth.

A difference between the co-evaporated and the sequentially processed absorbers is that the co-evaporated ones exhibit a higher doping density. This doping density could be decreased with an additional heat treatment. Interpreting the last capacitance step due to carrier freeze-out, the change of doping density can be attributed to a change of the doping defect. Prior to the treatment the co-evaporated absorbers have a doping acceptor situated roughly 20 meV above the valence band. After the heat treatment the absorber layers have a doping acceptor at least 80 meV above the valence band. On the other hand, interpreting the final capacitance step by a mobility freeze-out would suggest that the density of states at the Fermi level is lower for the co-evaporated samples than for the sequentially processed samples.

CHAPTER

SIX

CHARACTERIZATION OF SOLAR CELLS BY TEMPERATURE DEPENDENT IV MEASUREMENTS

As shown in section 2.3, the parameters J_0, A, r_S and R_{sh} can be obtained from an IV curve at a fixed temperature. With the measurement of the IV curve at several temperatures, not only the temperature dependence of these parameters can be obtained, but also the parameters J_{00} and E_A, which define J_0 (see Eqn. (2.13)). Especially the knowledge of E_A is of high importance in order to be able to distinguish between dominant interface or bulk recombination. Dominant bulk recombination should result in an activation energy which equals the bandgap [61]. Dominant interface recombination on the other hand can (but not necessarily have to) result in activation energies smaller than the bandgap [62]. This phenomenon may especially occur for heterojunction based solar cells such as CZTSe or CIGSe as the interface with the CdS buffer layer exhibits potentially many defect states. Lattice mismatch as well as segregation of certain elements (like Zn, H or O [136]) could induced defect levels and thus can dominate the recombination current.

The analysis of the temperature dependent IV curves is given in section 6.1. Section 6.1 not only introduces the standard analysis methods but also points out certain processes, which are not observed for measurements at room temperature but only at low temperatures.

The measurement results for sequentially processed and co-evaporated absorbers is given in section 6.2 and 6.3, respectively. A summary for both types of solar cells and an interpretation of the IVT measurement is given in section 6.4.

6.1. Temperature dependent IV analysis

6.1.1. Dominant recombination pathway

The activation energy of the dominant recombination path is given by the temperature dependence of J_0 according to Eqn. (2.13). In order to deduce this activation energy experimentally, several approaches exist, which are used in literature. Within this thesis, I will focus on only one method, which is the extrapolation of the V_{oc} to 0 K following Eqn. (6.1) (see also section 2.3)

$$V_{oc} = \frac{E_A}{q} - \frac{AkT}{q} \ln\left(\frac{J_{00}}{J_{ph}}\right). \tag{6.1}$$

A discussion about the validity of Eqn. (6.1) is presented in section C.1. It is concluded that the experimentally linear relationship of V_{oc} with temperature (at least for T > 200 K) and the subsequent deduced activation energy close to bandgap give reasonable plausiblity for the allowed application of Eqn. (6.1).

6.1.2. Series resistance

Another important issue is the evolution of the series resistance. As I have shown in Ref. [122] and also adressed in section 5.4.1 the knowledge of the series resistance is important as it impacts the measured admittance signal at low temperatures. In literature many groups report an increasing series resistance for CZTSSe devices when going to low temperatures [31, 34, 37, 55, 123, 137, 138]. However, the origin of the series resistance is still unresolved. Gunawan *et al.* attributed the thermally activated series to a back barrier [123]. This model was revised in a later manuscript, where the series resistance was attributed to carrier freeze-out [31]. Oueslati *et al.* demonstrated that the activation energy of the series resistance can be changed by changing the back contact to the absorber layer and thus hints to a back barrier as the origin of the series resistance [49].

In either case, carrier freeze-out or a back barrier, the series resistance is thermally activated as will be shown below. A consequence of the high series resistance is the suppression of the diode current, which is generally observed for the IV curves at low temperatures.

However, in addition to these already well studied models for the series resistance, in section 6.1.2.4 I want to propose another model, which was so far not mentioned in literature for the origin of the series resistance in CZTSSe devices. This model assigns the drop of the diode current at low temperatures to a barrier at the front contact, which impedes the injection of electrons in forward bias. This model is also capable of explaining the observed red kink as well as the violation of the super position principle for illuminated and dark IV curves.

6.1.2.1. Back barrier

When dealing with a back barrier, the back contact is a Schottky contact. For far enough forward bias, the current is then limited by the transport of holes over the back barrier and part of the voltage drops over the back barrier [126]. The total current over the back barrier is then given by [44, 126]

$$J_{bb} = A^* T^2 \exp\left(-\frac{q\Phi_b}{kT}\right)\left[1 - \exp\left(-\frac{qV_C}{kT}\right)\right]. \tag{6.2}$$

A^* is the effective Richardsen constant, V_C the voltage drop over the back barrier and Φ_b the barrier height of the Schottky contact. For small voltages V_C the exponential function with the voltage dependence can be Taylor expanded [139] and the resistance due to the back contact follows as [123, 140]:

$$R = \frac{V_C}{J_{bb}} = \frac{qA^*T}{k}\exp\left(\frac{q\Phi_b}{kT}\right). \tag{6.3}$$

From Eqn. (6.3) it follows that the series resistance is thermally activated. It needs to be noted that for higher values of V_C, the differential series resistance tends to infinity as the current saturates due to the back barrier [126].

6.1.2.2. Carrier freeze-out

As described in section 5.4.2, the series resistance arises due to a decreasing density of free majority carriers [125]. Using Eqn. (5.59), (5.60) and (5.61), the series resistance is given by

$$r_S = \frac{d}{q\mu_p}\frac{gN_D}{(N_A - N_D)N_V}\exp\left(\frac{E_A}{kT}\right). \tag{6.4}$$

The weak temperature dependence of the prefactor originates from the mobility, which a priori is not known, and from N_V.

6.1.2.3. Evaluation of the activation energy

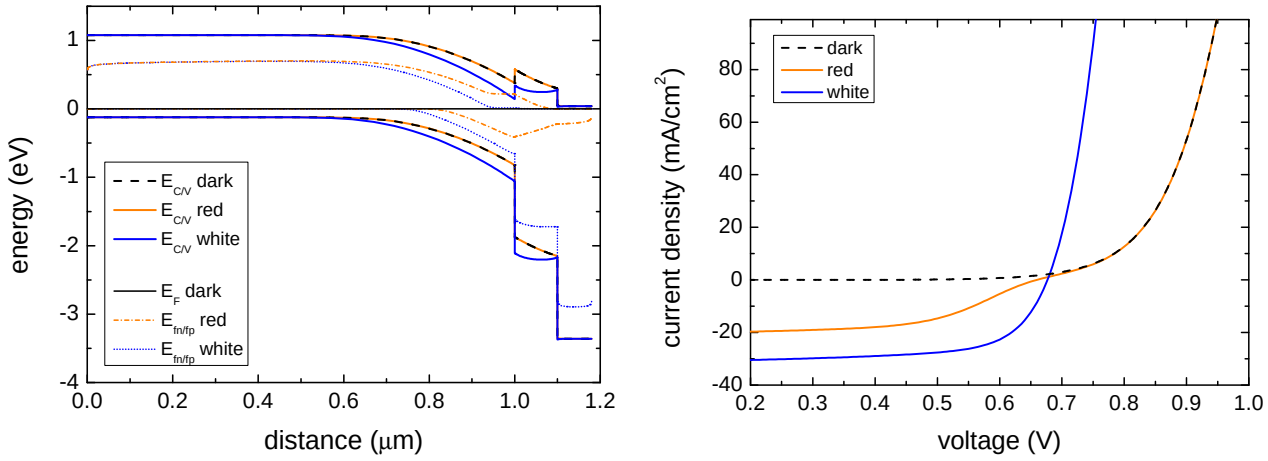
As it was shown in sections 6.1.2.1 and 6.1.2.2, the series resistance is thermally activated. By drawing an Arrhenius plot in the form of $\ln r_S$ versus $1/T$, the datapoints should yield a straight line and the activation energy is governed by the slope of a linear fit. In general, also the weak temperature dependence of the prefactor needs to be considered in a way that $\ln r_S T^m$ is plotted on the ordinate, where m denotes the exponent of the weak temperature dependence of the prefactor. However, the origin of the series resistance is generally not know and therefore, the term T^m is neglected.

6.1.2.4. Electronic doping of CdS

Electronic doping is a term describing the type behaviour of a semiconductor under illumination if for example a high density of deep defects are present [141,142]. In the case of the CdS buffer layer these deep defects can be compensating acceptor like states.

In the dark (or without generation in the CdS layer), the free electrons are trapped in the deep acceptor states and the net *fixed* charge density is small. In that case a substantial fraction of the built-in potential drops over the CdS [143]. With the generation of photo carriers in the CdS layer, the occupation of the deep defect is given by the rate equations of the capture and emission processes [111]. If $\sigma_p \gg \sigma_e$, i.e. the capture cross section for holes is much larger than the capture cross section for electrons, the deep acceptor state is mainly occupied by holes and thus is neutral and the *fixed* charge in the CdS layer is increased. Under these conditions the heterojunction behaves like a n^+p junction and the main part of the built-in voltage drops over the absorber layer.

An example of the band diagram for different kind of illumination conditions is shown in Fig. (6.1a). The band diagram is simulated with SCAPS [121]. Simulation parameters are given in Tab. 6.1. Exceptions from these values are the electron affinity of the CdS and the CdS thickness, which were set to 4.3 eV and 0.1 μm, respectively. Under white light illumination, the deep acceptors are occupied by photo generated holes and the net fixed charge is increased. Under these conditions, the buffer/absorber junction behaves like a n^+p junction. Without generation of photo carriers in the CdS (under dark conditions or under red light illumination), the fixed charge density in the CdS is small and a considerable amount of the built-in voltage drops over the CdS layer. This leads to a higher barrier for the injection of electrons from the window layer and to a smaller SCR width in the absorber and thus to a series resistance effect. This model also explains the red kink effect, which can be characterized by a loss of the photo current in the 4th quadrant of the IV curve under red light illumination. This red kink effect is often observed in CIGSe based solar cells, but was also found for CZTSe devices [144,145].



(a) Band diagram *(b) IV curves*

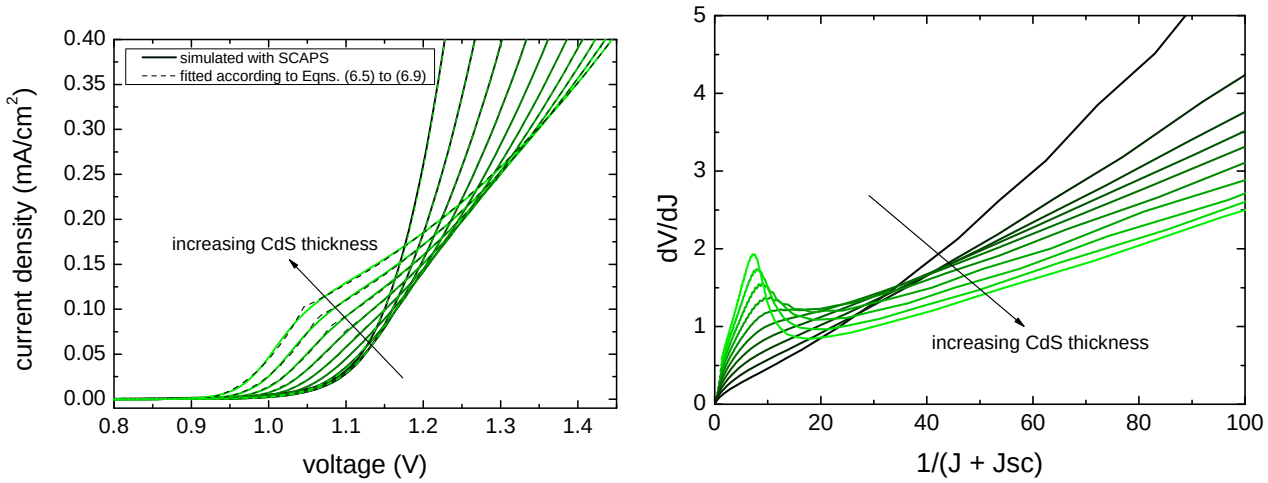
Figure 6.1.: ***Simulated band diagram and IV curves for a compensated CdS buffer layer with SCAPS*** *- (a) In the dark and under red light illumination (no generation in CdS), the net fixed charge in the CdS layer is low and a considerable amount of the built-in voltage drops over the CdS layer. Under white light illumination however, the deep acceptors in the CdS are occupied by photogenerated holes and thus increases the net fixed charge. In that case the junction operates as a n^+p junction. (b) Simulated IV curves for the three illumination conditions. For red light illumination the spectrum was cut-off at 600 nm.*

Fig. (6.1b) shows the corresponding IV curves simulated at 250 K. It shows the dark IV curve (dashed black line) and the IV curves under red (wavelengths $\lambda > 600$ nm) and white light illumination (orange and blue solid line, respectively). First, it is clearly visible that the red kind effect is well reproduced. Second, a cross-over between the dark and the white light illuminated IV curve is observed, which can be attributed to the afore mentioned increased barrier for injected electrons.

Thus, it is clear that the interface to the window layer, or more specific, the (CdS) buffer layer, may act as a barrier for injected electrons. According to Ref. [50], such a barrier might have a voltage dependence and thus would result in a non linear electronic element which is in series with the main diode. Due to the voltage dependence of the barrier, also a bump in the dark IV curve can occur. As will be shown in section 6.2.1, such a bump is also observed experimentally.

To study the effect of the CdS buffer layer on the IV curves, simulations were carried out with SCAPS [121], where the (compensated) CdS buffer layer thickness was varied. The simulation results are depicted in Fig. (6.2a). The other parameters for the simulation are given in Tab. 6.1. As observed from Fig. (6.2a), the dark IV curves do exhibit a bump, which is more pronounced the thicker the CdS buffer layer is.

In order to account for the voltage dependence of the barrier at the front contact, which is in series with the main diode, the total IV curve can be modelled as two diodes in series as shown in Fig. (6.3) [50]. It consists of two diodes, each connected in parallel with a shunt resistance and a series resistance. The current density J flows through all of these three elements such that the following three equations need to be fulfilled for an externally applied voltage V, which drops over the complete circuit:



(a) IV curves *(b) Evaluation with Sites method*

Figure 6.2.: ***Simulation and fit of IV curves with different CdS thicknesses*** *- IV data was simulated with SCAPS in the dark at 120 K for different CdS thicknesses. Simulation parameters are given in Tab. 6.1.*

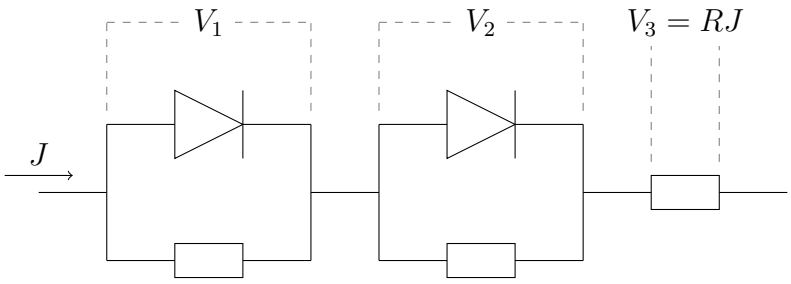


Figure 6.3.: ***Equivalent circuit for dc measurements of a solar cell with a secondary barrier.*** *- The secondary barrier (for instance at the front contact) is represented as a second diode in series to the main junction diode. A voltage V is applied to the complete circuit with the potential drops of V_1, V_2 and V_3 over the two diodes and the series resistance, respectively.*

Table 6.1.: *Simulation parameters for the graphs shown in Fig. (6.2). Batch parameter was the CdS buffer layer thickness. No interface defects were introduced.*

parameters	absorber	buffer	window
thickness (μm)	1.0	0.025 - 0.15	0.08
bandgap (eV)	1.2	2.45	3.4
electron affinity (eV)	4.5	4.35	4.55
shallow donor density (cm^{-3})	-	$1 \cdot 10^{17}$	$5 \cdot 10^{17}$
shallow acceptor density (cm^{-3})	$5.5 \cdot 10^{15}$	-	-
defect type	neutral	single acceptor (-/0)	-
capture cross section electrons(cm^2)	$1.0 \cdot 10^{-15}$	$1.0 \cdot 10^{-15}$	-
capture cross section holes(cm^2)	$1.0 \cdot 10^{-15}$	$1.0 \cdot 10^{-12}$	-
energetic distribution	single	single	-
energy level above E_V (eV)	0.6	0.6	-
total density (cm^{-3})	$1.0 \cdot 10^{18}$	$9.0 \cdot 10^{16}$	-

$$J = J_{0,1}\left[\exp\left(\frac{qV_1}{A_1 kT}\right) - 1\right] + \frac{V_1}{R_{sh,1}} \tag{6.5}$$

$$J = J_{0,2}\left[\exp\left(\frac{qV_2}{A_2 kT}\right) - 1\right] + \frac{V_2}{R_{sh,2}} \tag{6.6}$$

$$V = V_1 + V_2 + r_S J. \tag{6.7}$$

These three equations form a coupled system with three variables, $V1$, $V2$ and J, which need to be solved for a certain set of diode parameters, such as diode quality factors, saturation current densities, shunt resistances and the series resistance. In order to express one of the diodes, say diode 1, with a voltage dependent barrier $\Phi(V)$, $J_{0,1}$ can be written as

$$J_{0,1} = J_{00}\exp\left(-\frac{\Phi(V)}{kT}\right). \tag{6.8}$$

For simplicity a linear voltage dependence of the barrier height is assumed as depicted in Fig. (6.4). For a certain voltage V_0, the voltage independent part Φ_∞ remains, which is for example the conduction band offset between the window and the buffer layer. The function shown in Fig. (6.4) can be described as

$$\Phi(V) = \Phi_\infty + \Theta(V_0 - V)\Phi_{var}\frac{V_0 - V}{V_0}, \tag{6.9}$$

where Φ_{var} describes the voltage dependent barrier height and $\Theta(V_0 - V)$ denotes the Heaviside step function.

With Eqns. (6.5) to (6.9), an IV curve can be fitted. The fitting routine solves the system of equations (Eqn. (6.5) to Eqn. (6.7)) for each voltage and each iteration and adjusts the fitting

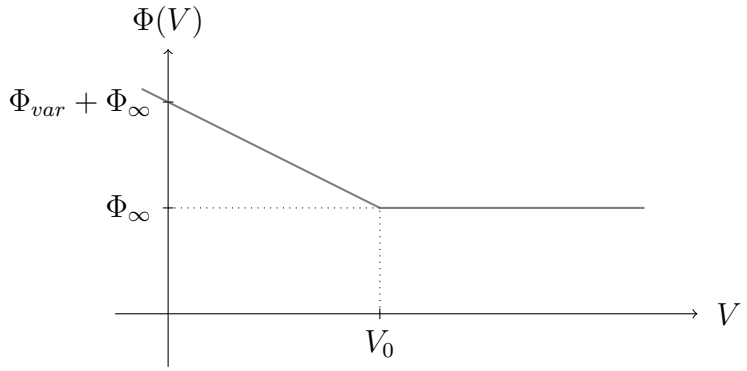


Figure 6.4.: *Voltage dependent barrier* *- For zero bias voltage the barrier height is $\Phi_{var} + \Phi_\infty$ and decreases linearly for higher forward bias voltages, which describes the voltage dependent part of the barrier. For bias voltages higher than V_0, the barrier height is given only by its voltage independent part Φ_∞.*

parameters for the two diodes, the two shunt resistances and the series resistance. The dashed lines in Fig. (6.2a) are fits to the simulated IV curves with SCAPS, which show that the bump in the dark IV curves is well described by the proposed model.

The simulated curves with SCAPS were further investigated with the Sites method [71, 72] as described in section 2.3.3.1. The plot of J^{-1} versus $\mathrm{d}V/\mathrm{d}J$ is shown in Fig. (6.2b). As the curves were simulated without illumination and without a shunt conductance, the other terms on the abscisssa can be omitted (see section A.1). Clearly, a bump is observed for small values of J^{-1}. Such a bump was previously assigned to a barrier in forward bias [72]. In this example it arises due to the blocking of injected electrons by the CdS buffer layer as can be seen by the increased magnitude of the bump with thicker CdS buffer layers.

6.2. On sequentially processed absorbers

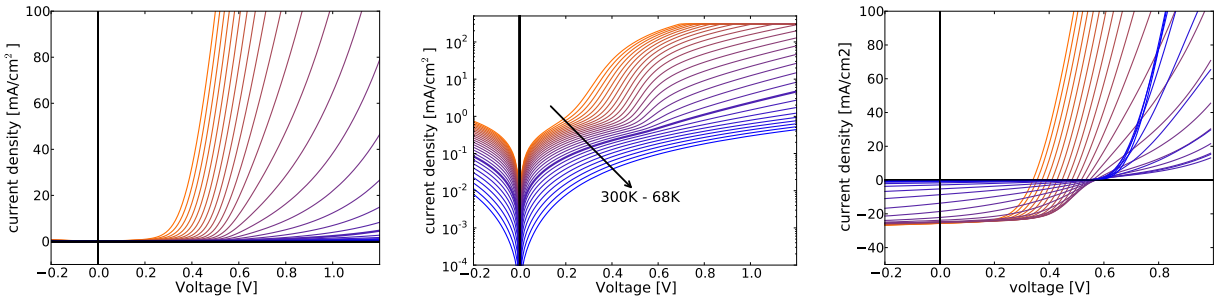
An IVT measurement of a sequentially processed solar cell is shown in Fig. (6.5a) and (6.5b) under dark conditions on a linear and a logarithmic abscissa, respectively and in Fig. (6.5c) under illumination. The colour code for the variation of temperature is for all samples and measurements the same and is indicated in Fig. (6.5b).
From these figures, three generally observed features can be pointed out:

1. In the dark, the forward current drops to almost zero at low temperatures. In Ref. [43] I have shown that the series resistance is thermally activated with energies between 70 and 200 meV.

2. The photo current decreases to zero when going to low temperatures.

3. The forward current under illumination decreases strongly at low temperatures. However, this drop is not as pronounced as in the case of the dark curves. Interestingly, for some samples, the diode current under illumination is recovered for the lowest temperatures, as it is the case shown in Fig. (6.5c).

In the following I want to set the focus on the model of a blocking barrier at the front contact for the origin of these effects. In another publication I have discussed the possibility of carrier



(a) dark, linear ordinate (b) dark, logarithmic ordinate (c) illuminated, linear ordinate

Figure 6.5.: *IVT measurement for a sequentially processed solar cell* - *Under dark conditions an increase of the series resistance is observed when decreasing the temperature. Under illumination (c), a loss of photo current and a drop of the forward diode current occurs at low temperatures.*

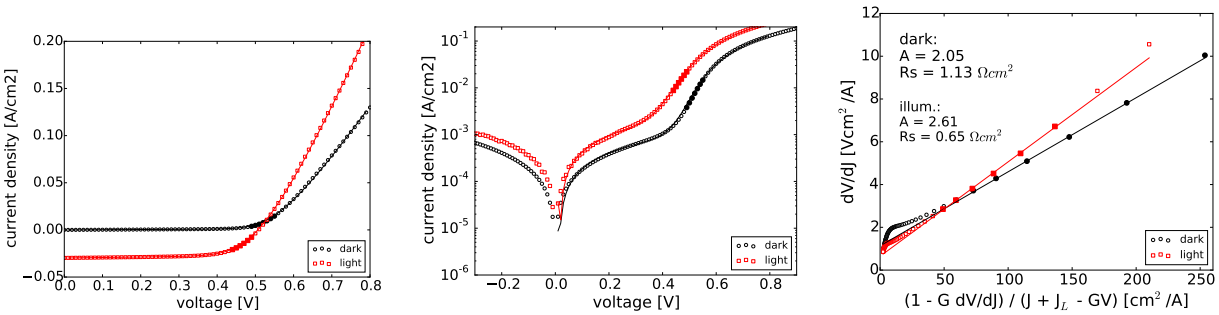
or mobility freeze-out [41]. This model of a freeze-out will be recaptured and discussed in section 6.4.

6.2.1. Loss of forward diode current

At high temperatures the solar cell shows a proper one diode behaviour, indicated by a shunt resistance around zero bias, a diode behaviour between 0.2 V and 0.4 V and the presence of a series resistance at higher forward bias voltages. Decreasing the temperature, the onset of the exponential voltage dependence is shifted to higher voltages due to the thermally activated behaviour of J_0 according to Eqn. (2.13). When decreasing the temperature further, also the bending of the curve at far forward bias increases (see Fig. (6.5b)) which can be attributed to an increasing series resistance (c.f. Fig. (2.4b)). The series resistance was determined with the iv-fit routine and the Sites method, as described in section 2.3.3.1. I have shown in Ref. [43] that the series resistance is thermally activated with activation energies between 70 meV and 200 meV. These values are consistent with values reported in literature for CZTSSe devices on Mo, where activation energies between 99 meV and 135 meV are observed [34, 49, 123].

However, an open question is still the origin of the thermal activation of the series resistance. In Ref. [41] I have assigned the series resistance at low temperatures to carrier or mobility freeze-out. If either p or μ_p increases exponentially by lowering the temperature, the series resistance increases according to Eqn. (5.60). As I have mentioned in Ref. [122], also indications for a blocking barrier are observed experimentally, which will be discussed in the following.

Hegedus *et al.* [72] pointed out that the presence of a blocking barrier (in far forward bias) can be exposed by plotting $\mathrm{d}V/\mathrm{d}J$ versus $(1 - G\mathrm{d}V/\mathrm{d}J)/(J + J_L - GV)$ (see section A.1). In that representation such a blocking barrier is presented as a bump for small values of $(1 - G\mathrm{d}V/\mathrm{d}J)/(J + J_L - GV)$. For CdTe based solar cells this bump is attributed to a back contact barrier [72]. As the hole current over the back barrier is thermally activated, it may be negligible at room temperature, may however limit the current flow at low temperatures. Two graphs from the analysis of the solar cell parameters according to the Sites method [71, 72] are shown in Fig. (6.6). The dark (black data points) and illuminated (red data points) IV curves were recorded at 195 K and are shown on a linear and a logarithmic scale in Fig. (6.6a) and (6.6b), respectively. The solid data points highlight the voltage range, where a diode behaviour is



(a) Selection from IV curve (linear scale)

(b) Selection from IV curve (logarithmic scale)

(c) Sites analysis

Figure 6.6.: ***Evaluation of sequentially processed sample by IV fit and the Sites method*** *- IV curves were recorded at 195 K. (a) and (b) show the IV curves and the selection of the diode behaviour (solid symbols). (c) shows the plot of* $\mathrm{d}V/\mathrm{d}J$ *of the Sites analysis. For both curves a bump is observed. The bump for the dark curve is stronger pronounced compared to the illuminated curve.*

observed (data points lie on a straight line for a logarithmic ordinate). Fig. (6.6c) shows the graph of $\mathrm{d}V/\mathrm{d}J$ versus $(1 - G\mathrm{d}V/\mathrm{d}J)/(J + J_L - GV)$. Obviously, a bump occurs for small values of $(1-G\mathrm{d}V/\mathrm{d}J)/(J+J_L-GV)$, which points to a blocking barrier in (far) forward bias. Comparing the magnitude of the bump for the dark and illuminated curve it can be inferred that the barrier under dark conditions is stronger pronounced. Still, even in the presence of a barrier, the diode parameters can be obtained. As indicated by the solid symbols, the datapoints describing the diode like behaviour of the solar cell yield a straight line which can be fitted to deduced r_S and A[1].

As mentioned above, some papers exist in literature, which ascribe the thermally activated series resistance to a blocking back barrier [49]. However, a back barrier would also imply a roll-over for the dark and illuminated IV curves [126], which is not observed experimentally. Also, the IV curves from CZTSSe devices in Ref. [140], where the blocking back barrier was initially proposed for kesterite based devices, do not show a roll over but rather a red kink. A red kink for CZTSe based solar cells was also observed by Buffière *et al.* [144] and Redinger *et al.* [145]. In both studies the red kink occurs for light with photon energies below the bandgap of CdS. A common model for CIGSe based solar cells for this kind of behaviour is the compensation of the CdS layer by a large amount of deep acceptor states with asymmetric capture cross sections [142, 143, 147, 148]. This model is described in section 6.1.2.4 on the electronic doping of the CdS buffer layer. It explains the cross-over effect observed for the illuminated and the dark IV curve as well as the difference between the dark and illuminated curves in Fig. (6.6c), i.e. the smaller bump under illumination. Additionally, the sequentially processed samples investigated here are prepared similarly to the sample described in [145], which shows a red kink if no carriers are photo generated in the CdS buffer layer. The only difference of the growth process used for the samples presented here is that SnSe chunks were introduced in the hot zone during annealing (see section 3.2) instead of the $SnSe_2$ capping layer.

Fig. (6.7) shows IV curves measured at 300 K under different illumination intensities. Lower

[1] With the knowledge of these parameters, it is possible to deduce a barrier height if the blocking behaviour is due to a back barrier [146]. However, this analysis was not carried out in the framework of this thesis.

light intensities were obtained by the attenuation of the illumination with neutral density filters. The transmittance of these filters is given in the legend of Fig. (6.7). It is observed that the higher the illumination intensity the higher is the injection current at high forward bias voltages, which is qualitatively consistent with the model of a compensated CdS buffer layer.

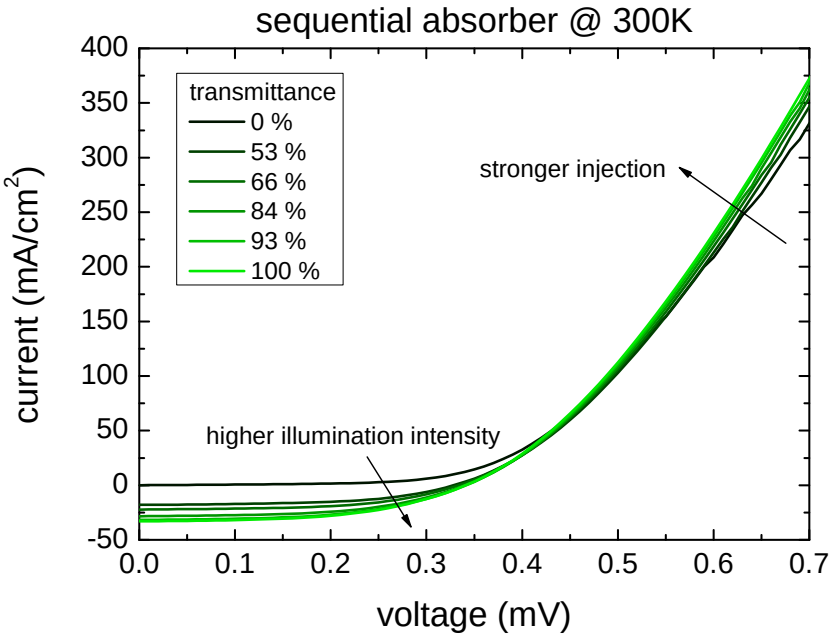


Figure 6.7.: ***Illumination dependent IV curves of a sequentially processed solar cell*** *- Attenuation of the illumination was realised via neutral density filters. The IV curves show a higher injected forward current for higher illumination intensities. This phenomenon can be explained by the model of a compensated CdS buffer layer as the barrier for injected electrons is lowered with generation of carriers in the CdS buffer layer.*

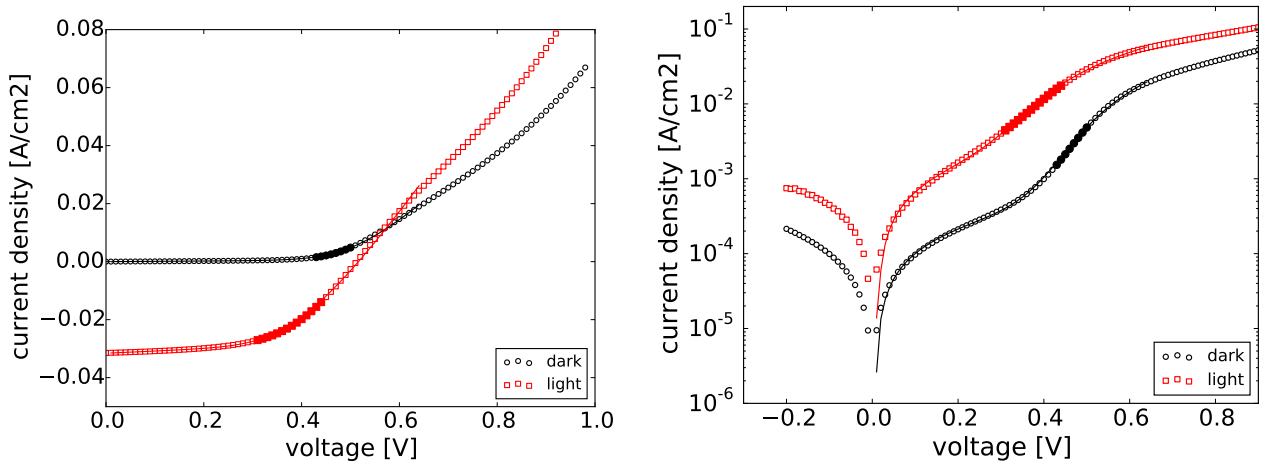
Table 6.2.: *Comparison of activation energies for the series resistance under light and dark conditions for sequentially processed samples.*

	unit	AR133	MM141	MM142	MM144	MM146	MM153
E_A^{dark}	(meV)	105	165	64	92	171	83
E_A^{light}	(meV)	105	138	56	96	170	81

From the considerations above, the activation energy for the series resistance under illumination should be lower than the activation energy under dark conditions. These activation energies for the same six samples as presented in section 5.2 are compared and listed in Tab. 6.2. Apparently, the activation energies are similar, independent of the illumination. However, this might also be due to the application of the one-diode model is not appropriate. Fig. (6.8) shows IV curves of a sequentially processed sample at low temperatures for a linear (Fig. (6.8a)) and a logarithmic (Fig. (6.8b)) ordinate. It is visible that the IV curves exhibit a bump at roughly

0.6 V under illumination as well as under dark conditions. Plotting the IV curve on a logarithmic scale as shown in Fig. (6.8b) it becomes apparent that data points at high forward bias do not show an ohmic resistance but rather form a straight line, indicating a diode like behaviour. These IV curves resemble the simulated IV curves shown in Fig. (6.2a). Thus, the blocking of the forward diode current can very well be described by a barrier at the front contact. Also note that the analysis of the series resistance is made for voltages smaller than 0.6 V as indicated by the solid symbols in Fig. (6.8), which could explain why similar activation energies of the series resistance are obtained independent of illumination (see Tab. 6.2).

Another important point of this model is that the collection function cannot be calculated as described in section B. Due to the illumination dependent injection current, the collection efficiency at V_{oc} would be highly underestimated.



(a) On linear scale *(b) On logarithmic scale*

Figure 6.8.: ***Evaluation of IV data at low temperatures*** *- Sample MM146 measured at 200 K under illumination (red symbols) and in the dark (black symbols). For both curves a bump in the IV curve is observed which could be due to a secondary barrier.*

6.2.2. Loss of photo current

As mentioned in section 6.2 and shown in Fig. (6.5c), also the photo current is lost at low temperatures. Fig. (6.9) exemplifies that this loss of the photo current comes along with the increase of the series resistance and the levelling off of the V_{oc} when decreasing the temperature. This behaviour is present in all sequentially processed samples. A barrier for the photo current could be located at the hetero interface. Due to a conduction band spike, the electrons need to be thermally excited to pass this barrier. However, as has been shown by Redinger *et al.* [55], the photo current loss is also observed for SSe devices. Even for devices based on pure S containing absorbers, i.e. CZTS, the photo current loss is observed [124]. It was shown that these (pure S containing) devices exhibit a cliff like conduction band alignment [52] and therefore no barrier for the photo generated electrons due to the CdS buffer layer. Furthermore, Redinger *et al.* showed that a higher concentration of ZnSe at the front contact leads to a stronger increase of the series resistance [55]. This observation is consistent with the findings of Wätjen *et al.*, who showed the blocking behaviour of ZnSe at the hetero interface [149]. Yoo *et al.* [150]

demonstrated a blocking behaviour of ZnSe at the surface to the window layer for absorbers based on $CuInSe_2$.

Such a barrier induced by an intermediate ZnSe layer at the surface would therefore act as a barrier for photo generated carriers as well as a barrier for the diode current. However, the blocking behaviour does not necessarily have to be situated at the hetero interface. In fact, as could be shown by Schwarz *et al.* [151] the sequentially processed absorbers presented here exhibit a nanometer sized ZnSe network in the bulk of the absorber. Thus, it is reasonable to assume that a barrier due to the ZnSe network is present in the bulk and is responsible for the blocking of the (diode- and photo-) current.

However, at this point, the location and therefore also the origin of the blocking barrier cannot be determined. Still, it seems that the barrier which is responsible for the drop of the diode current also causes the loss of the photo current, which in turn means that this barrier is not due to the CdS buffer layer for the sequentially processed devices.

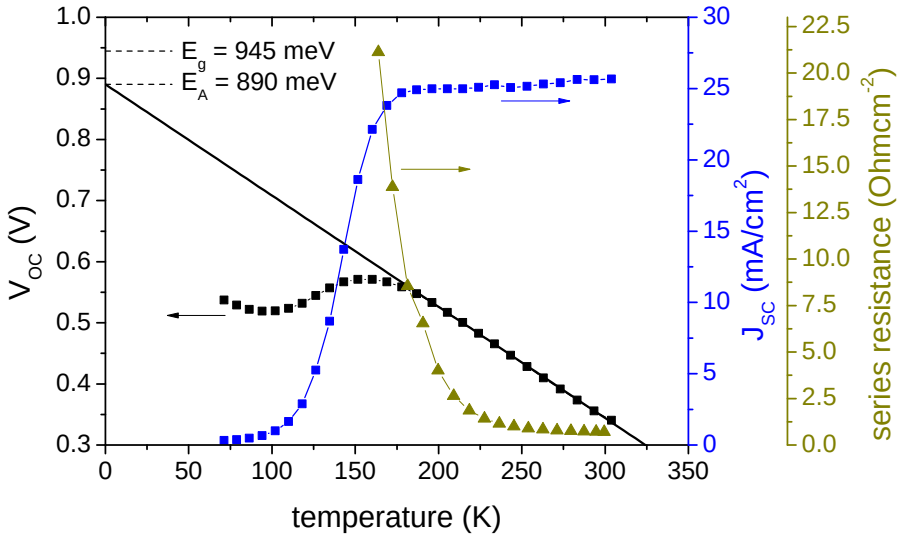


Figure 6.9.: V_{oc}**,** J_{sc} ***and*** r_S ***data versus temperature*** *- It is apparent that the loss of the photo current goes along with the increase of the series resistance and the levelling off of the open circuit voltage when decreasing the temperature. This kind of behaviour is present in all sequentially processed devices. The linear part of* V_{oc} *at high temperatures above 200 K was linearly fitted and extrapolated to 0 K to obtain the activation energy of* J_0*. The bandgap energy* E_g *was determined by an EQE measurement.*

6.2.3. Dominant recombination pathway

The activation energy of the dominant recombination pathway may be extracted by the extrapolation of V_{oc} to 0 K. As discussed in section C.1 and shown in Fig. (6.9) the V_{oc} follows a straight line at high enough temperatures (above 200 K). The obtained value for E_A yields a value of 890 meV for the sample presented here and lies roughly 50 meV below the bandgap as deduced from an EQE measurement. A value for E_A slightly below the bandgap is generally observed for all samples as depicted in Fig. (6.17). However, as these values are slightly below the bandgap, it is difficult to assign the dominant recombination path to interface or

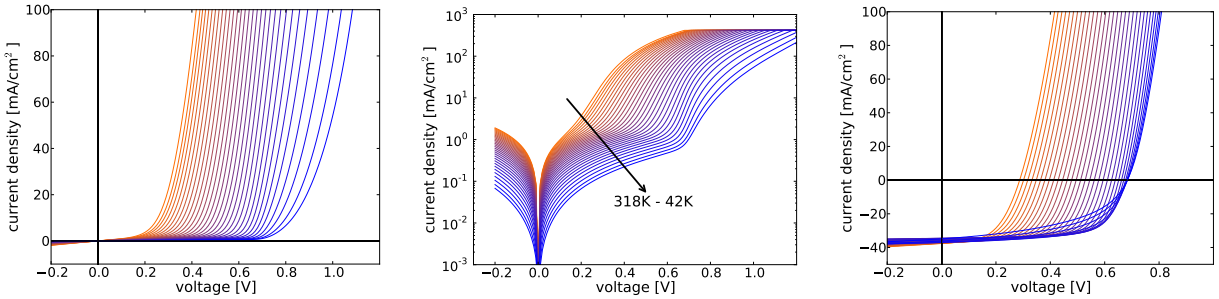
bulk recombination. As mentioned in section C.1, a prerequisite for the analysis is a temperature independent diode quality factor which is not met. Thus, even though the V_{oc} versus temperature plot is linear, the slope might be lowered and thus could result in underestimated activation energies.

However, for these pure Se based devices, the activation energy is close to the bandgap. This behaviour is generally not observed for SSe based devices [55, 103, 123, 124, 152], where the deduced activation energy differs significantly from the bandgap such that it is concluded that these devices are limited by interface recombination. Hence, no clear conclusion can be drawn regarding the dominant recombination pathway for the sequentially processed samples presented here.

6.3. On co-evaporated absorbers

In this chapter I will present the results from IVT measurements for co-evaporated samples. First I will discuss the measurements on solar cells prepared from as grown absorbers in section 6.3.1. As pointed out in section 5.6 about capacitance measurements an additional heat treatment changes the behaviour compared to the as grown samples. The low temperature heat treatment is also reflected in the IVT measurements as I have shown in Ref. [41]. These findings will be presented in section 6.3.2.

6.3.1. As grown



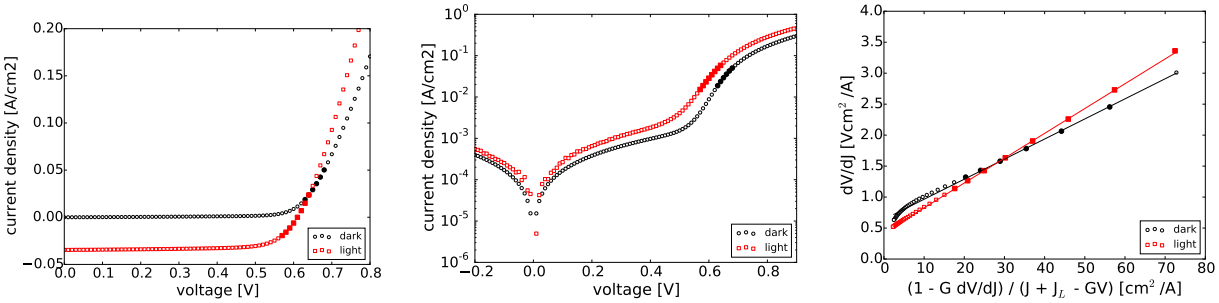
(a) dark measurement (linear scale) *(b) dark measurement (logarithmic scale)* *(c) illuminated measurement (linear scale)*

Figure 6.10.: ***IVT curves of a co-evaporated sample*** *- Temperature dependent IV curves under dark conditions on a linear (a) and logarithmic (b) current density scale. The IV curves under illumination are shown in (c).*

A typical IVT measurement for a solar cell from an as-grown absorber is shown in Fig. (6.10), which clearly differs from the behaviour observed for the sequentially processed samples presented in section 6.2 (c.f. Fig. (6.5)).

The solar cell shows a proper diode behaviour even at low temperatures. Note the wider measured temperature range compared to the sequentially processed sample presented in Fig. (6.5). Only at the lowest temperatures the onset of the rise of the series resistance and the reduction of the photo current is observed. This could indicate that the barrier responsible for the loss of the diode and photo current in the sequentially processed samples is also present

in the co-evaporated samples but with a considerably lower barrier height. In the plot of $(1 - G\mathrm{d}V/\mathrm{d}J)/(J + J_L - GV)$ versus $\mathrm{d}V/\mathrm{d}J$ shown in Fig. (6.11c), again a bump for the dark curve is observed indicating a barrier in forward bias. This bump is not present under illumination.



(a) Selection from IV curve (linear scale)

(b) Selection from IV curve (logarithmic scale)

(c) Sites analysis

Figure 6.11.: ***Evaluation of as grown co-evaporated sample according to Sites method*** *- IV curves were recorded at 125 K. (a) and (b) show the selection of the voltage range where the diode behaviour is observed (solid symbols). (c) shows the plot of* $\mathrm{d}V/\mathrm{d}J$ *of the Sites method. Clearly, a small bump in the dark is observed, while the illuminated curve shows a straight behaviour.*

An Arrhenius plot of the series resistance under dark conditions yields a straight line for temperatures below 125 K as shown in Fig. (6.12). The series resistance was evaluated using the Sites method[2]. From the slope of a linear fit an activation energy of 11 meV is obtained. This activation energy is significantly smaller than the ones obtained for the sequentially processed samples.

Fig. (6.13) shows a plot of IV curves acquired under different light intensities via neutral density filters. As for the case of the sequentially processed samples (c.f. Fig. (6.7)) a higher forward diode current is obtained with higher illumination intensities.

All these findings so far indicate an illumination dependent barrier for the as grown co-evaporated devices, which could be explained by the model of an electronic doping of the CdS buffer layer as presented in section 6.1.2.4.

6.3.1.1. Buffer layer thickness variation

Fig. (6.14a) shows IV curves in the dark and under illumination from devices processed with different CdS buffer layer thicknesses (c.f. section 3.4 for the growth of these devices). The curves were recorded at ≈ 40 K, which is the lowest temperature for the IVT measurements. The lowest temperature was chosen, since due to the low barrier height as mentioned above, the rise of the series resistance is not observed at higher temperatures. The dark curves in Fig. (6.14a) (solid lines) show a shift of the onset of the exponential diode current with thicker CdS layers. In contrast, the illuminated curves (dashed lines) do not show this behaviour but an onset at essentially the same voltage. The thickness variation of the CdS buffer layer including deep compensating acceptor states was simulated by Pudov *et al.* [153]. These simulated IV curves show the same behaviour as the experimental ones shown in Fig. (6.14a).

[2]The ivfit routine yields a rather constant series resistance. This phenomenon is due to the failure of the fit at low temperatures as it is shown in section C.3.

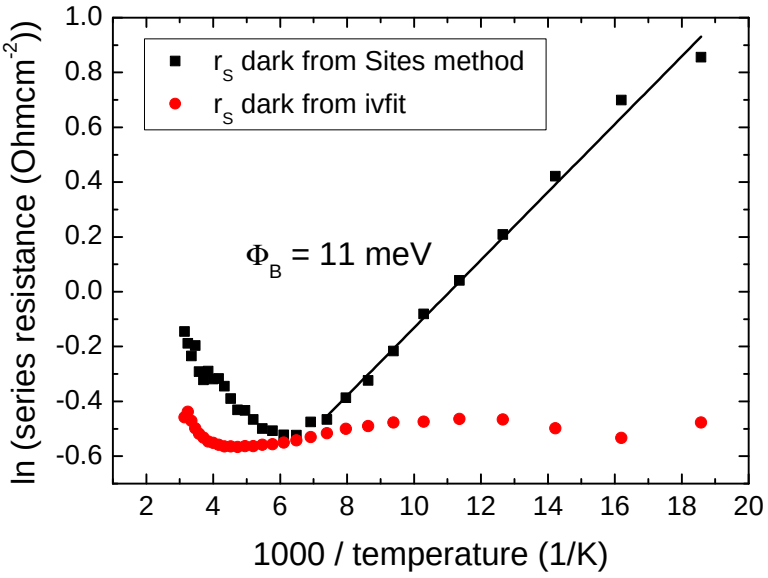


Figure 6.12.: ***Arrhenius plot of the series resistance for a co-evaporated as grown solar cell*** *- With the evaluation by the Sites method a thermally activated series resistance is obtained with an activation energy of 11 meV.*

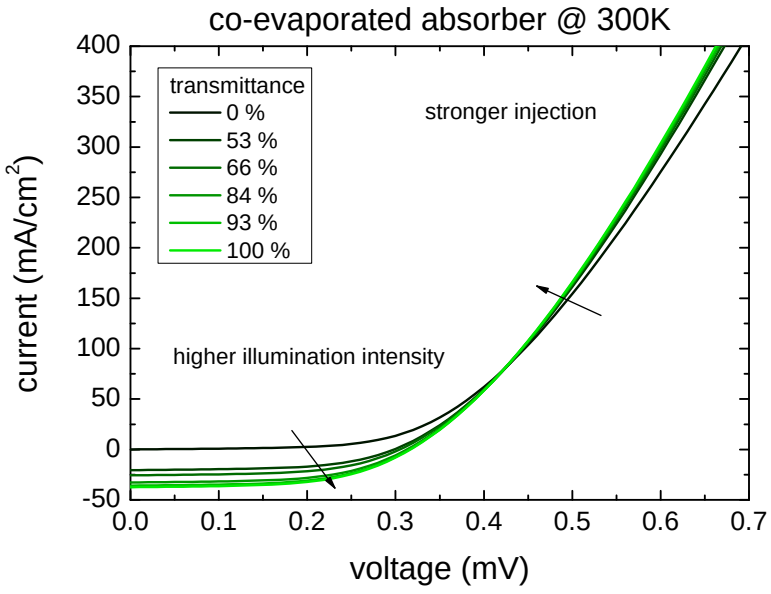
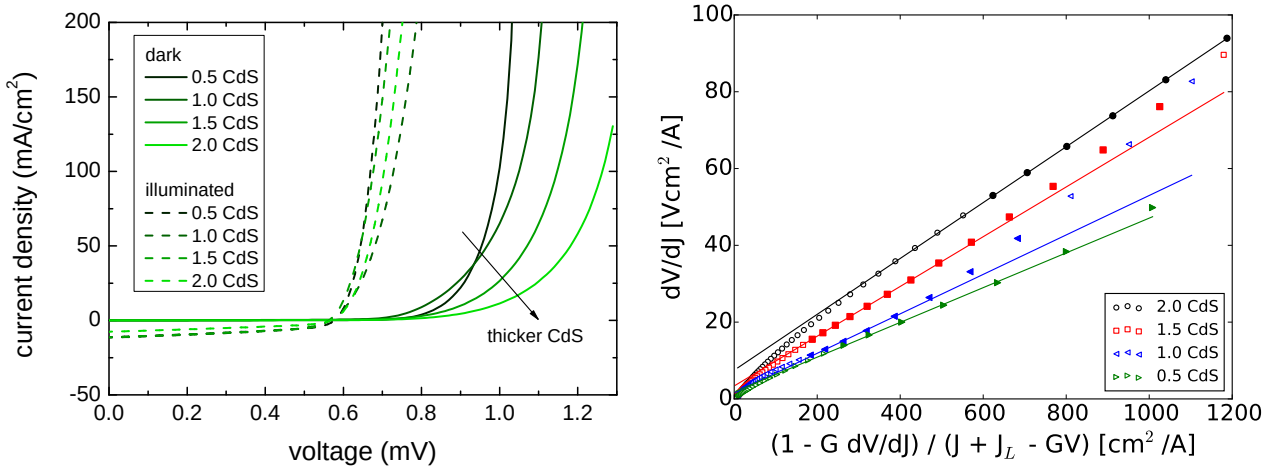


Figure 6.13.: ***Illumination dependent IV curves at 300 K*** *- For higher illumination intensities a higher injected forward current is obtained similar as for sequentially processed samples (c.f. Fig. (6.7)).*

The dark IV curves shown in Fig. (6.14a) were further investigated with the Sites method. The plots of $\mathrm{d}V/\mathrm{d}J$ versus $(1 - G\mathrm{d}V/\mathrm{d}J)/(J + J_L - GV)$ are shown in Fig. (6.14b). Even though the bump is only weakly pronounced the non linear behaviour for small values of $(1-G\mathrm{d}V/\mathrm{d}J)/(J+J_L-GV)$ is clearly visible and increases with thicker CdS buffer layers. This shape is mimicked for the simulated curves with thin CdS buffer layers shown in Fig. (6.2b). However, it needs to be mentioned that one feature differs from the simulated IV curves in Fig. (6.2b) (Sites plot), which is the cross over of the curves. This cross over is not observed for the experimental curves shown in Fig. (6.14b).

Apart from the not observed cross-over effect in the Sites evaluation, the behaviour of the illuminated and dark IV curves of devices from co-evaporated absorbers can be explained by the model of a compensated CdS buffer layer as discussed in section 6.1.2.4. Note that the samples with a varying CdS thickness underwent an additional in-situ heat treatment as described in section 3.4 [3].



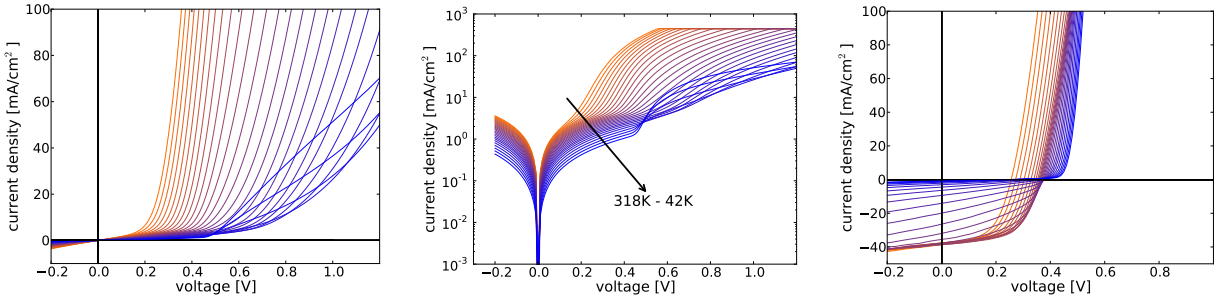
(a) IV curves at ≈ 40 K. *(b) Evaluation with Sites method.*

Figure 6.14.: ***Evaluation of IV curves with different CdS thicknesses*** *- (a) shows IV curves with (dashed lines) and without (solid lines) illumination. Under illumination the onset of the exponential diode current occurs at the same voltage independent of the CdS layer thickness. Under dark conditions the onset is shifted to higher voltages for thicker CdS buffer layer thicknesses. (b) shows the evaluation of the dark curves with the Sites method at low temperatures. Even though the bump is only weakly pronounced, the non-linearity at small values of* $(1 - G\mathrm{d}V/\mathrm{d}J)/(J + J_L - GV)$ *can still be observed and increases with thicker CdS buffer layers.*

6.3.2. Additional heat treatment

As described in section 3.3.3, after the co-evaporation process of the absorber and prior to the deposition of the CdS buffer layer, for some samples an additional heat treatment was applied. The exposure to air between growth process and heat treatment might be an important issue as the IVT curves differ compared to the curves discussed in the previous section 6.3.1.1.

[3] After the growth process, these samples were kept for 12 h at 180 °C. However, the absorbers were not exposed to air during growth and heat treatment and therefore differ from the absorbers discussed in section 6.3.2.



(a) dark linear (b) dark logarithmic (c) illuminated linear

Figure 6.15.: ***IVT curves after low temperature heat treatment*** *- After the high temperature co-evaporation growth process, the absorbers underwent an additional low temperature heat treatment. Note that the samples were exposed to air between these two processes.*

Fig. (6.15) shows an IVT measurement for a sample which underwent the low temperature heat treatment at 180 °C. The temperature dependent IV curves for the additional high temperature annealing treatment do not differ qualitatively from the ones shown in Fig. (6.15) and are therefore omitted. The measurement under dark conditions (Fig. (6.15a)), shows that the forward diode current is recovered for the lowest temperatures. However, this feature is seen only for this sample and not for any other sample, which underwent an additional heat treatment.

A general difference to the devices from as-grown absorbers is the stronger suppression of the forward diode current under dark conditions (except the recovery at very low temperatures). This can be related to a higher activation energy of the series resistance as determined from an Arrhenius plot (not shown). The sample shown in Fig. (6.15) has an activation energy of 85 meV (compared to 11 meV for the as-grown sample shown in Fig. (6.5)). However, the origin of the change of the activation energy of the series resistance is still not resolved.

Along with the increase of the series resistance comes the loss of the photo current as it becomes apparent from Fig. (6.15c).These two phenomena (drop of diode current and loss of photo current) occur in the same temperature range and therefore point to a common barrier, which block both currents at low temperatures, similar to the behaviour of the sequentially processed samples.

However, as I have published in Ref. [41], another reasonable explanation for the thermal activation of the series resistance is the freezing out of free carriers or the mobility. In either way, the series resistance increases via Eqn. (5.60). A detailed discussion about the increase of the series resistance at low temperatures will be given in section 6.4.2.

Another point, which needs to be discussed, is the activation energy of the dominant recombination pathway. It was shown for the as-grown absorbers that the activation energy of J_0 from the extrapolation of the V_{oc} data is slightly below the bandgap. Fig. (6.16) shows the V_{oc} extrapolations for two devices with an additional heat treatment. Blue solid circles and black solid squares show the V_{oc} data for devices with an additional high temperature annealing step and a low temperature heat treatment, respectively [4]. The corresponding open symbols denote the data for their reference samples, which were grown in the same process run but without an additional heat treatment.

[4]Note that the high temperature annealing step is the same as for the sequentially processed samples (see section 3.3.3).

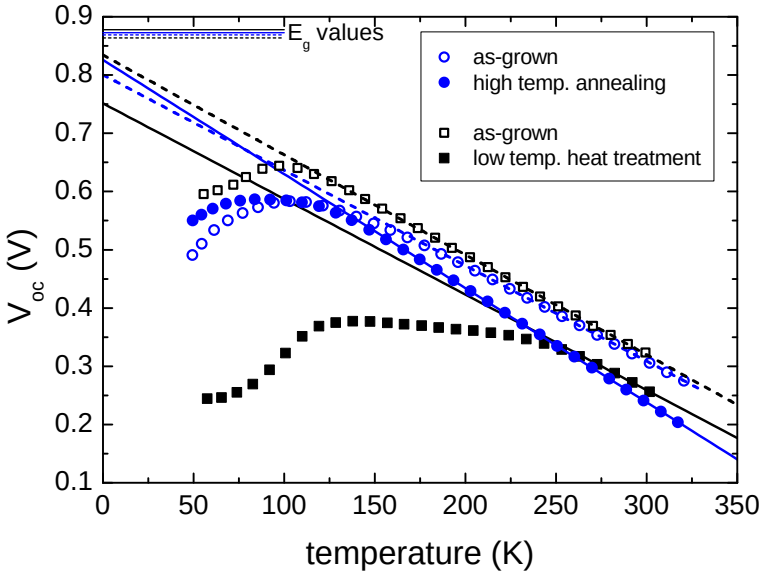


Figure 6.16.: V_{oc} ***extrapolation after additional heat treatment*** *- Compared are two devices. One with a high temperature annealing process (solid blue circles) and one with the low temperature heat treatment (black solid squares). The sample prepared with the low temperature heat treatment shows a significant lowered activation energy compared to its bandgap (c.f. also Fig. (6.17)).*

As I have published in Ref. [41] the as-grown co-evaporated devices all have activation energies of the recombination path of 820 ± 20 meV. Also the co-evaporated device with the high temperature annealing process exhibits an activation energy in this energy range. The devices with a low temperature heat treatment however, demonstrate an activation energy around 740 meV. As I have already suggested in Ref. [41] this lowering of the activation energy might be due to the exposure of the absorber layer to air between the growth and the low temperature heat treatment. This assumption is backed up when looking at the activation energies of the samples which were prepared with different CdS thicknesses as described in section 3.4. These samples were not exposed to air prior to the low temperature heat treatment and show activation energies between 810 meV and 830 meV as it is the case for the as-grown devices. A comparison of the activation energies with the bandgap for the differently processed samples will be given in section 6.4.1.

From these findings of a lowered activation energy of J_0 with the exposure of the absorber to air prior to a heat treatment, another importance of the addition of Se and SnSe during annealing can be pointed out. Initially, Se and SnSe was introduced into the hot zone during annealing in order to stabilize the kesterite phase [74]. However, the other beneficial effect is that the activation energy of J_0 does not suffer due to the exposure of the absorber to air.

6.4. Summary and interpretation of IVT measurements

In this section I want to summarize the results I have discussed in the previous sections on IVT measurements. With that I will recapture the observed phenomena and place them into a model, which describes the experimental data.

6.4.1. Dominant recombination pathway

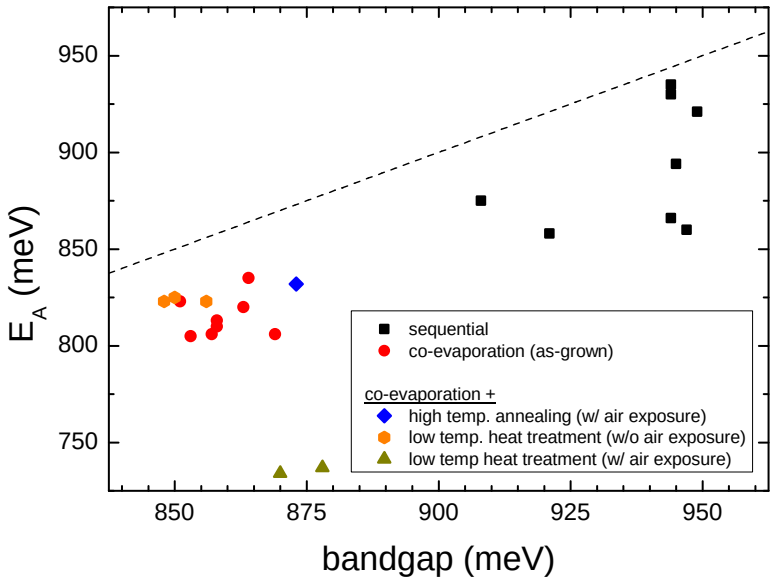


Figure 6.17.: ***Comparison of*** V_{oc} ***intercepts with the bandgap*** *- Except the samples which were exposed to air prior to a low temperature heat treatment (green triangles), all samples show an activation energy slightly below the bandgap.*

Fig. (6.17) compares the activation energy of the V_{oc} extrapolation (open symbols) with the bandgap for a number of measured devices. The dashed straight line in Fig. (6.17) has the slope of 1 and goes through the origin. The devices can be grouped as follows:

1. as-grown co-evaporation (open red circles)
2. sequential process (open black squares)
3. co-evaporation with additional low temperature heat treatment without air exposure (orange hexagons).
4. co-evaporation with additional low temperature heat treatment with air exposure (open green triangles)
5. co-evaporation with additional high temperature heat treatment with air exposure (open blue diamond)

The first observation is that the sequentially processed samples exhibit a larger bandgap compared to the high temperature co-evaporated samples. One explanation might be that these latter devices are rather disordered which can reduce the bandgap up to 110 meV compared to the ordered state [22]. The disordered state could arise from the fast cooling of the absorbers after the co-evaporation process, when the samples are transferred into the loadlock. The sequentially processed samples on the other hand exhibit a slow cooling as these samples cool inside the graphite box, which itself is still located in the hot zone of the oven.

Apart from that, all devices show intercepts of the extrapolation of the V_{oc} with the ordinate slightly below the bandgap. An exception in form of a significant lower activation energy is observed for samples which were exposed to air prior to an additional low temperature heat treatment (green triangles). This reduction of the activation energy is not observed if the

devices are not exposed to air prior to the low temperature heat treatment (orange hexagons). Thus it can be assumed that defect states form at the interface (due to air exposure) which pin the Fermi level and lead to an interface dominated recombination current. Samples which underwent a high temperature heat treatment do not show a decreased activation energy of J_0 probably due to the Se and SnSe annealing atmosphere.

The slightly lowered activation energy for all the other devices might occur due to the fact that the diode quality factor is not temperature independent, as already mentioned in section 6.2.3. Another reason might be an incorrect measurement of the temperature. For the measurement of the IV curve the voltage is generally swept from negative to positive voltages starting from -0.2 V. Thus, by the time the datapoint at V_{oc} is recorded the sample could already be heated due to the illumination. As the temperature sensor cannot be placed at the same position as the sample, which is the position with the highest illumination intensity, the heating of the sensor might be smaller. Consequently, the measured temperature is underestimated, which leads to a smaller slope (in absolute values) of the V_{oc} versus T data. The result is a smaller measured activation energy.

As a conclusion it can be said that these devices all exhibit the same dominant recombination pathway, except the ones which were exposed to air prior to a low temperature heat treatment. Assuming a constant diode quality factor, the dominant recombination pathway could be assigned to bulk recombination. Of course, the temperature independent diode quality factor is not observed experimentally by the voltage dependence of the IV curve. However, this could also be an artefact. One reason could be the violation of the modelling with the one diode model. As previously argued in sections (6.3.1) and (6.2), these devices might very well be modelled with a double diode model. However, how such a barrier impacts the shape of the IV curve and with that the determination of the diode parameters was not further investigated in this work.

6.4.2. Series resistance and drop of photo current

An important feature which is observed for the sequentially processed samples and the co-evaporated samples after a heat treatment is the increase of the series resistance and the drop of the photo current at low temperatures. Interestingly, all co-evaporated samples (either with or without an additional heat treatment) do not show an increase of the series resistance under illumination. This fact might point to a different origin of the series resistance for the sequentially processed and the co-evaporated devices. Thus, these two kind of devices are discussed in the following separately.

6.4.2.1. Sequentially processed samples

As mentioned above, the sequentially processed samples exhibit a thermally activated series resistance in the dark as well as under illumination. Besides, for all these devices a drop of the photo current is observed at low temperatures, which also hints to a barrier for the photo current. As it is shown in Fig. (6.9), these two processes start to occur at the same temperature. Thus, it can be suggested that the origin of these two phenomena is the same.

In literature, the drop of the photo current is also observed for the S based devices, exhibiting a cliff like band alignment with the CdS buffer layer [52–54]. Additionally, for the Se based devices a correlation of the series resistance with the amount of ZnSe at the front contact could

be demonstrated [145]. These findings imply an explanation of the current blocking, which is not due to the CdS buffer layer as discussed in section 6.1.2.4.

As suggested by Redinger *et al.* Ref. [145] an intermediate ZnSe layer at the front contact could be the reason for the current blocking at low temperatures. However, it is unlikely that a complete layer of ZnSe forms at the front contact. Additionally, such a layer was detected neither by atom probe tomography (APT) nor by transmission electron microscopy (TEM) for these devices. However, instead a nanometer sized ZnSe network has been detected by APT [151] in the bulk of the absorber which could very well be the reason for the current blocking in the dark and under illumination. Such a network was not observed for the co-evaporated samples [41] and would therefore explain why the bocking of the current for the as-grown absorber layers is not observed.

6.4.2.2. Co-evaporated samples

The co-evaporated samples showed different behaviour depending on whether an additional heat treatment was applied or not. Additionally, the air exposure between growth and additional heat treatment might be important in the interpretation of the measurements.

As mentioned in section 6.3.1 the as-grown absorbers are well described by the model of a compensated CdS buffer layer. First, a higher injection current is observed for higher illumination intensities. Second, with the Sites method [71] a barrier in forward bias is observed for the dark IV curves, which is not present for the illuminated IV curves.

The sample series with a varying CdS buffer layer thickness behave similar to the as grown samples, i.e. as well according to the model of a compensated CdS buffer layer. Pudov *et al.* [153] carried out simulations where the CdS buffyer layer thickness was varied. These simulated curves show the same qualitative behaviour as the experimental curves, which I have shown in section 6.3.1.1. One feature of the IV curves which was previously not yet pointed out and could also be linked to the CdS buffer layer is a bump in the dark IV curves. I simulated this bump in (the dark IV curves) with SCAPS and could show that such a bump can be modelled by a voltage dependent barrier for injected electrons[5]. I showed next that due to the CdS buffer layer also the bump in the plot in the Sites method of $\mathrm{d}V/\mathrm{d}J$ versus $(1 - G\mathrm{d}V/\mathrm{d}J)/(J + J_L - GV)$ arises. This bump becomes more pronounced for thicker CdS buffer layers, which is well reproduced by the experimental data.

These findings strengthen the model of a compensated CdS buffer layer capable of describing the experimental IV behaviour for the devices from co-evaporated absorbers presented here. Included are all devices, which were prepared by a high temperature co-evaporation process as well as the devices which underwent an additional low temperature heat treatment without air exposure.

The samples which were exposed to air prior to an additional heat treatment differ slightly from the devices discussed above. It seems that the series resistance in the dark and the loss of the photo current is stronger pronounced (occurring already at higher temperatures) compared to the samples from the CdS thickness series (which underwent a low temperature heat treatment but without air exposure). Otherwise they behave similar by means that they do not show an increase of the series resistance under illumination. Thus, the model of the

[5]It needs to be pointed out that a bump in *illuminated* IV curves can be simulated by various models [154]. Such a bump in the illuminated IV curve in the 4th quadrant, often referred to as a red kink, is due to a voltage dependent photo carrier collection and therefore differs from the bump observed in the dark IV curves.

compensated CdS buffer layer might also still be valid for these samples. However note that not only deep acceptors in the CdS layer might produce the different behaviour between illuminated and dark IV curves, but also acceptor like interface states [155]. In this case these states could enforce the blocking of the diode current and could also explain the drop of the photo current [155].

However, as I have discussed already in Ref. [41], another explanation for the series resistance could be carrier or mobility freeze-out. Due to the reduced mobility or free carrier concentration the series resistance under dark conditions would rise exponentially. In contrast, the series resistance under illumination would still be small due to photo generated carriers into the bands. This concept is further discussed in section 7.

CHAPTER

SEVEN

MODEL FOR CURRENT CZTSE DEVICES

In this chapter I want to summarize the effects observed from admittance and IVT measurements. Most signatures from these measurements are now well understood and will be put into a common model. Section 7.1 will give an overview of the samples presented here and their characteristics in IVT and admittance measurements. Section 7.2 will emphasize the importance of the fitting routine for the results obtained in this thesis. Sections 7.3 and 7.4 will then discuss the low and high temperature behaviour of the solar cells putting together insights from both characterisation methods (IVT and admittance).

7.1. Overview of device characteristics

An overview of the devices presented in this thesis is given in Tab. 7.1. It consists of co-evaporated samples (as grown and with various heat treatments) as well as the sequentially processed samples. The observations made from IVT and admittance measurements are listed. Noted is always the general behaviour. However, exceptions from this behaviour may occur as discussed in the previous sections and explained in the table notes.

Table 7.1.: *Overview of investigated samples with their growth process and their characteristics in IVT and admittance measurements.*

Absorber growth					
growth	co evap.	co-evap.	co-evap.	co-evap.	sequential
heat treatment	-	180 °C	180 °C	520 °C [a]	520 °C [a]
air exposure before treatment	no	no	yes	yes	yes
IVT					
therm. act. r_S, dark	(yes)[b]	yes	yes	yes	yes
therm. act. r_S, ill.	no	no	no	no	yes
V_{oc} extrapolation	$\sim E_g$	$\sim E_g$	$< E_g$	$\sim E_g$	$\sim E_g$
Admittance					
high temp. step	no	no	no	yes	yes
double low temp. steps	no[c]	yes	yes[c]	yes[d]	yes
bent Arrhenius plot[e]	-	yes	yes	yes	yes

[a] note that the high temperature annealing is carried out in Se and SnSe atmosphere.
[b] the activation energy for these samples is considerably lower and is therefore marked as *(yes)*.
[c] this is the general observation. However, a few samples also show a different behaviour.
[d] only one sample prepared.
[e] bent Arrhenius diagram is seen for capacitance step 2. Generally capacitance step 1 does not show a clear inflection frequency (only present as shoulder).

7.2. Analysis of capacitance spectra with the fitting routine

In this section I want to stress the significance of the fitting routine for the evaluation of the capacitance spectra presented in section 5.3.2. The fitting routine allows the deconvolution of overlapping capacitance steps and thus attributes the correct capacitance contribution to each individual step. It was pointed out in section 5.3.3 that the Walter analysis [24] overestimates the capacitance contribution in such a scenario of overlapping capacitance steps.

Using this fitting routine it was possible to thoroughly analyse the samples with different CdS buffer layer thicknesses (see section 5.7.2). For these set of samples it was important to extract the correct capacitance drop for each step in order to calculate the expected extension of the SCR width on the n side of the hetero junction.

Another important result is the quantification of the high temperature capacitance transition, which is highlighted in section 7.4 below.

7.3. Low temperature behaviour

By admittance spectroscopy the low temperature behaviour is marked by a capacitance transition which drops to the geometrical capacitance. This transition either consists of an overlapping double step or a single (but often asymmetric) step. From IVT measurements in the dark a thermally activated series resistance can be deduced. For now, only the device behaviour in the dark is considered as these are the conditions for the admittance measurements. Fig. (7.1a) shows the deduced activation energies E_A from admittance spectroscopy (either single or double capacitance step) versus the activation energy Φ_B of the series resistance. Solid black squares and red circles denote the data points for devices exhibiting a double capacitance step and arise from one of the growth processes listed in Tab. 7.1. Only two datapoints for devices with a single capacitance step are available. These devices show the onset of the series resistance and also the drop of the capacitance at too low temperatures such that no reliable energies can be deduced. Literature values are added from Refs. [28, 34, 38][1]. Based on Fig. (7.1a), the two low temperature capacitance steps are discussed in the following two subsections.

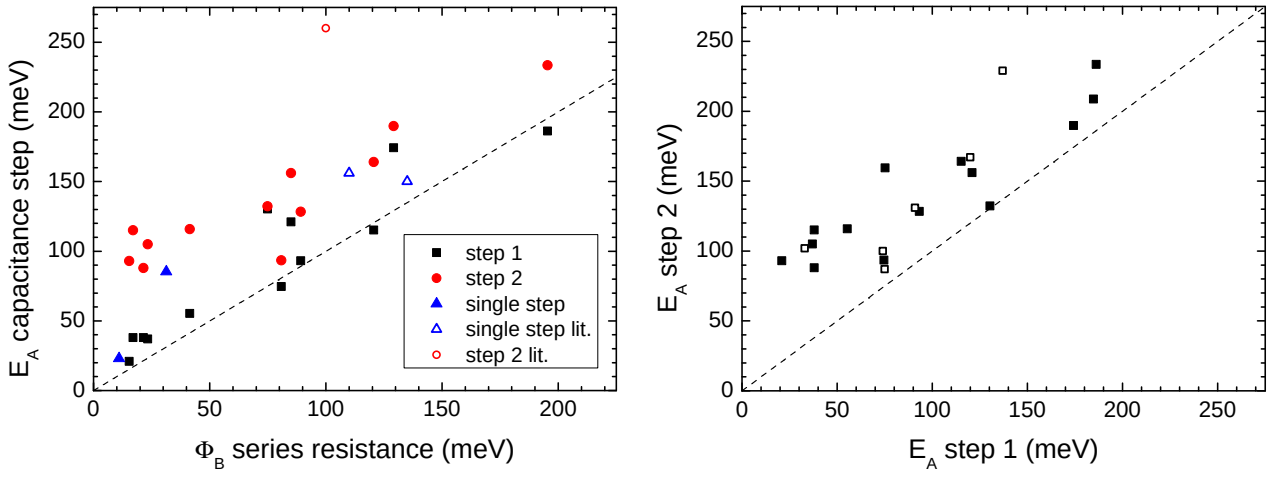
7.3.1. Series resistance and final capacitance step

From Fig. (7.1a) a clear correlation of the activation energies of the series resistance and the final capacitance step can be observed (step 1). I have shown in a previous publication [43] and in section 5.5.2.1 that such a correlation exists for the sequentially processed samples. However, from Fig. (7.1a) it is evident that this behaviour is also fulfilled for the co-evaporated samples (datapoints with $\Phi_B < 50\,\mathrm{meV}$).

The final capacitance step drops to the geometrical capacitance. Gunawan *et al.* have attributed this drop of the capacitance to carrier freeze-out (for CZTSSe based solar cells), which could also be the origin for the devices presented here. In this interpretation, the activation energy is the distance of the doping acceptor from the valence band maximum (see section 5.4.2). The wide spread of the activation energies shown in Fig. (7.1a) could be explained by the Meyer-Neldel law [156], which was already observed for CIGSe based solar cells [127, 157, 158].

As I have pointed out in Ref. [41] and section 5.7.1 also a mobility freeze-out could be responsible for the final capacitance step, which also explains the series resistance at low temperatures.

[1] These values from literature are all based on S containig absorbers, i.e. CZTSSe.



(a) Compilation of activation energies of the series resistance and the capacitance steps

(b) Correlation between the activation energies of the two capacitance steps.

Figure 7.1.: ***Dependence of the series resistance and the two low temperature capacitance steps*** *- From (a) a clear correlation between the activation energie of the energetically lower capacitance with the series resistance can be noticed. This observation holds for the sequentially processed samples as well as for the co-evaporated ones. Literature data taken from Refs. [28, 34, 38] (open symbols). (b) shows that the two low temperature capacitance step are not independent from each other. These capacitance steps shift simultaneously in energy. Literature data taken from Refs. [37, 39, 40, 42] (open symbols).*

As discussed in section 5.4.5, the inflection frequencies are proportional to $\exp\left(-B/T^{1/4}\right)$, where B is a constant proportional to $N(E_F)$, the density of states at the Fermi level. Therefore, instead of different values for the activation energy from the usual Arrhenius evaluation, different values for B are obtained in terms of an evaluation according to a mobility freeze-out (under variable range hopping conduction). The scatter of the various values for B among the samples could thus be explained by different values for $N(E_F)$.

In conclusion, the final capacitance step can very likely be attributed to the series resistance. The series resistance is either due to carrier freeze-out or mobility freeze-out. The scattering of the activation energies in the case of carrier freeze-out could be described by the Meyer-Neldel law [156]. In the case of a mobility freeze-out this effect can be attributed to different values for $N(E_F)$.

7.3.2. Second capacitance step

The interpretation of the capacitance step 2 is still ambiguous. However, the findings which I have gathered from IVT and admittance measurements will be recaptured here.

Several aspects hint to the fact that this capacitance step is caused by the CZTSe/CdS interface:

1. From IVT measurements a barrier under dark conditions and in forward bias is observed (see section 6.2.1 and 6.3.1). I have shown that several indications exist that this barrier is located at the front contact of the absorber layer. The illumination dependent series resistance as well as the sample series with different CdS buffer layer thicknesses

(section 6.3.1.1) is well described by a barrier induced due to a compensated buffer layer. Such a barrier should also be reflected in the admittance spectra. Note that such a barrier could also be induced due to interface defects [155] as mentioned in section 6.4.2.2.

2. The Arrhenius plot of the inflection frequencies shows a bent curve (see Fig. (5.26)) and could be a sign of thermally assisted tunneling through the CdS buffer layer [135]. In this model, the capacitance step originates from an interface defect state.

3. From the drop of the capacitance step the extension of the SCR width can be calculated as described in section 5.4.4. These values roughly correlate with the thickness of the CdS buffer layer plus the intrinsic ZnO layer as I have demonstrated in section 5.7.2. This finding is in accordance with the previous point, i.e. the capacitance step is caused by an interface defect state [127, 128] (see section 5.4.4).

The weak point in the list above is the correlation of the calculated extension of the SCR width on the n side with the experimentally determined thickness of the CdS buffer layer and the i:ZnO layer as presented in section 5.7.2. The assignment of the capacitance step to an extension of the SCR width on the n side is therefore questionable.

Another intriguing point is that the activation energy of this capacitance step correlates with the series resistance similarly as the final capacitance step. A difference is that the activation energy of this second capacitance step is shifted to higher energies. The fact that the activation energies of the two capacitance steps are not independent is shown in Fig. (7.1b). Literature values (open squares) are added from Refs. [37,39,40,42]. The dependence of the two activation energies evaluated from admittance spectroscopy are not understood at this point.

7.4. High temperature capacitance transition and open circuit voltage deficit

The high temperature capacitance transition is observed for samples which underwent the high temperature annealing process (see Tab. 7.1). I have shown that this capacitance signature is introduced due to the annealing process. The fitting routine allows the quantification of this capacitance transition and can be described by a deep defect distribution. A convincing correlation of the depth of the deep defect distribution with the V_{oc} deficit was demonstrated (see Fig. (5.20)). This finding is of crucial importance:

1. Sequential processes are widely applied in literature [13].

2. Such a high temperature capacitance transition is also observed in other devices reported in literature (c.f. Tab. 1.1). Remarkable is the fact that also the 10.1 % efficient device reported in Ref. [28] shows such a transition.

Therefore, being aware of such a deep defect distribution and taking care that such a defect level is not introduced during the annealing step, might help to boost the V_{oc}, which is the main bottleneck for higher efficient kesterite based solar cells [9, 152].

CHAPTER

EIGHT

ACKNOWLEDGMENTS

First of all I want to thank Susanne Siebentritt for the opportunity to work in her group, which involved the electrical characterization of a very new and interesting material. The guidance and discussions during the whole time of this thesis were very helpful. In this regard I also want to thank Alex Redinger who helped me a lot either with discussions, python scripts or in the lab - especially handling and fixing the PVD. Without that help it would have not been possible to publish the papers which resulted during this thesis and which allowed me to travel to conferences and workshops. A big thank you for that.

I want to thank Uwe Rau, Andreas Michels and Thomas Schmidt and again Susanne Siebentritt and Alex Redinger for being part of the dissertation defence committee.

Of course I am also very thankful for the whole LPV and LEM team. A special thank you goes to: Patricia Ramoa, for helping with ordering issues and paper work in general, which I probably would have never managed to do by myself. Thomas Schuler for the thousand things which needed to be fixed in the lab and always having a solution ready. Maxime Thevenin and Michele Melchiorre for all the hours they spent at the SEM and finishing the solar cell devices. Marina Mousel for providing the first set of samples which I then could characterize. Vicente Reis Adonis for building all that stuff I needed for the IVT/admittance setup. Germain Rey for growing together more and more CZTSe absorbers. David Regesch for providing the template of this thesis and helping with all programming related problems. Tobias Bertram for many discussions about admittance and related topics. Didier Arl for last minute FIB measurements. And of course everyone else for the off-topic discussions during kitchen meetings or other occasions.

Finally, I would like to thank my family Simon, Clara, Ina and Ulli Weiß and my girlfriend Laurence Schmitz for mental support during the last years.

APPENDIX

A

SITES METHOD

A.1. Influence of shunt resistance

The analysis carried out in Ref. [72] assumes the contribution of the shunt resistance R_{sh} to be negligible. For the determination of the series resistance r_S and the diode quality factor the authors then state to plot $(J + J_{sc})^{-1}$ versus $\mathrm{d}V/\mathrm{d}J$ and fit the straight part. However, a correction for R_{sh} cannot simply be made by plotting $(J + J_{sc} - GV)^{-1}$ as given in Ref. [72]. In contrast $(1 - G\mathrm{d}V/\mathrm{d}J)\,(J + J_{sc} - GV)^{-1}$ needs to be plotted on the abscissa. This has already been stated by Sites and Mauk [71], but no derivation was given in that publication.

The starting point is Eqn. (2.12), which can be rewritten as

$$J + J_{ph} - G_{sh}V + G_{sh}r_sJ = J_0\exp\left(\frac{q\,(V - r_sJ)}{AkT}\right). \tag{A.1}$$

with $G_{sh} = 1/R_{sh}$ denoting the shunt conductance. Solving for V on the right hand side yields

$$V = r_sJ + \frac{AkT}{q}\ln\left(J + J_{ph} - G_{sh}V + G_{sh}r_sJ\right) - \frac{AkT}{q}\ln J_0. \tag{A.2}$$

Taking the derivative of the expression (A.2) results in

$$\mathrm{d}V/\mathrm{d}J = r_s + \frac{AkT}{q}\frac{1 - G_{sh}\mathrm{d}V/\mathrm{d}J + G_{sh}r_s}{J + J_{ph} - G_{sh}V + G_{sh}r_sJ}. \tag{A.3}$$

Assuming the product of $G_{sh}r_s$ to be small enough Eqn. (A.3) becomes

$$\mathrm{d}V/\mathrm{d}J = r_s + \frac{AkT}{q}\frac{1 - G_{sh}\mathrm{d}V/\mathrm{d}J}{J + J_{ph} - G_{sh}V}. \tag{A.4}$$

Therefore, by plotting $\mathrm{d}V/\mathrm{d}J$ versus $\frac{1-G_{sh}\mathrm{d}V/\mathrm{d}J}{J+J_{ph}-G_{sh}V}$ results in a straight line with the intercept of the ordinate at r_S and with a slope of AkT/q.

A.2. Implementation and analysis

In order to evaluate the IV data according to ref. [72], a self-made Python script is used. It enables to plot the consecutive graphs relying on data obtained from previous plots in this analysis. Fig. (A.1) shows an example of these plots and the obtained IV parameters. The IV curve was taken at $\approx 231\,\mathrm{K}$ in the dark.

First the IV curve is plotted on a linear and a logarithmic current density axis. From that plot the region of the diode behaviour can be selected, which is indicated as the red data points. In the third graph the shunt conductance is calculated from the mean derivative around zero bias. The black line indicates a linear fit to the data and the shunt conductance is then taken as the mean value of the fit, i.e. the value at zero bias for a symmetric fitting range around $0\,\mathrm{V}$. For the calculation of the series resistance and the diode quality factor, a plot of $\mathrm{d}V/\mathrm{d}J$ versus $(1-G\mathrm{d}V/\mathrm{d}J)/(J+J_L-GV)$ needs to be performed. The same datapoints in the region of the diode behaviour as selected from the IV curve are marked in this plot as red circles as well. Linearly fitting yields the series resistance from the intercept with the ordinate and the diode quality factor from the slope. The saturation current density is obtained from the plot of $V-RJ$ versus $\ln(J+J_L-GV)$ and indicated in the last graph. The diode quality factor is also governed from the fit of this graph, too. A general observation is that there is a discrepancy between the two obtained diode quality factors from the last two graphs. However, the diode quality factors obtained from the fit and the plot of $\mathrm{d}V/\mathrm{d}J$ are commonly in good agreement. Therefore, the diode quality factor is given by either of these two methods.

Another interesting feature is that the curve bends backwards in the last graph for high voltages. An improvement of this bending can be achieved by using a smaller series resistance. A smaller series resistance is obtained for a smaller intercept with the ordinate in the plot of $\mathrm{d}V/\mathrm{d}J$. This could be done by fitting the data only for very small values on the ordinate. However, these values correspond to datapoints at high forward bias and therefore do not represent the behaviour of the diode anymore. I think that more reliable values are obtained by deducing the IV parameters as represented in Fig. (A.1). The bending at high values of $V-RJ$ might be attributed to a non-ohmic behaviour at high forward bias voltages.

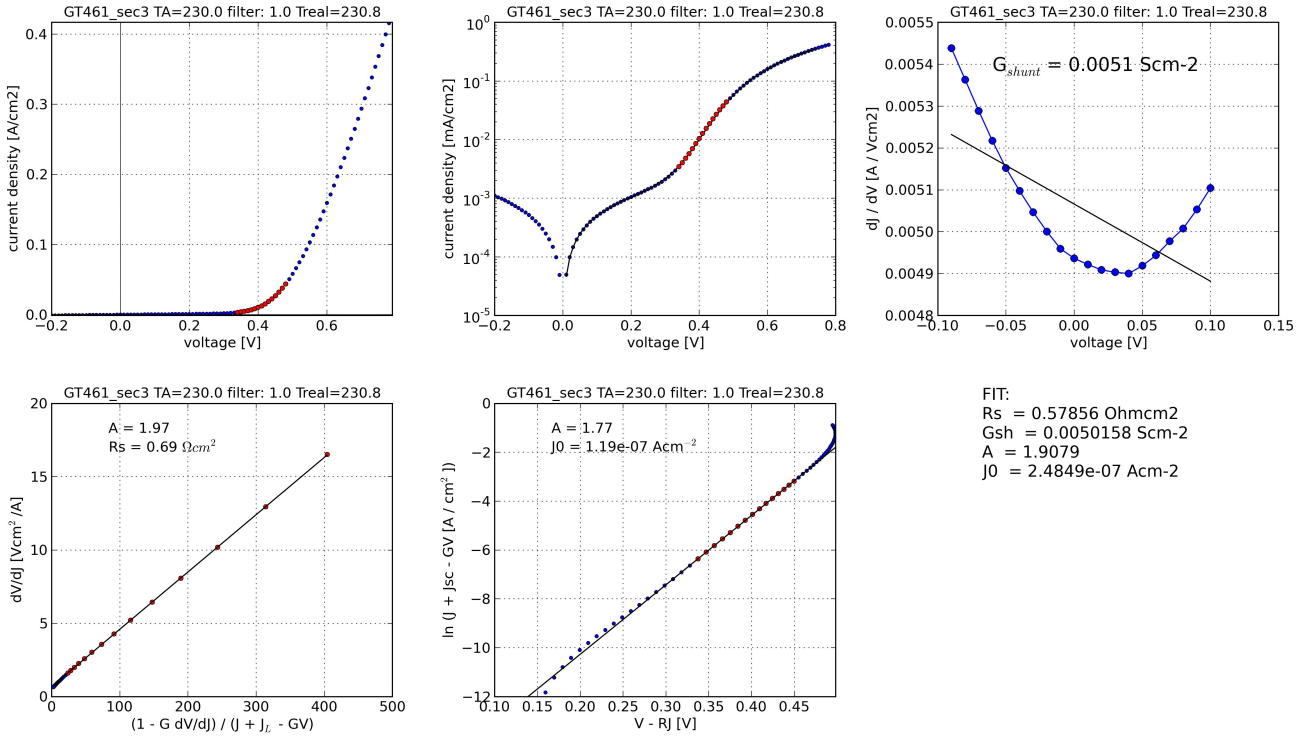


Figure A.1.: ***Implementation of the Sites method*** *- The consecutive plots proposed in Refs. [71, 72] are shown. The plot of $\mathrm{d}J/\mathrm{d}V$ on the ordinate (upper right graph) shows no linear behaviour. However, the variation of the values for $\mathrm{d}J/\mathrm{d}V$ in that voltage range is small so that the solar cell behaviour around zero bias voltage can still be modelled as an ohmic shunt conductance.*

APPENDIX

B

COLLECTION FUNCTION

For a voltage dependent photo carrier collection, the photo current can be written in the form of [159]

$$J_{ph}(V) = J_{sc}\eta(V) \tag{B.1}$$

where $\eta(V)$ is the collection efficiency. With that the current density can be written in the form [50]:

$$J(V) = J_{\text{diode}}(V) - J_{ph}(V). \tag{B.2}$$

This representation is only valid for a small series resistance. The reason is that the photo current needs to be taken into account for the calculation of the diode current, according to Eqn. (2.12). As the voltage drop over the diode is modified by $r_S J$, the shift of the voltage depends on the series resistance and the photo current [160]. Thus, the measured diode current is generally corrected for the series and the shunt resistance [161, 162] and

$$J(V) \rightarrow J'(V'), \tag{B.3}$$

where V' denotes voltage corrected by the series resistance and J' the current corrected by the shunt resistance. With Eqn. (B.1) and (B.2) the collection function can be estimated from two measurements $J_1(V)$ and $J_2(V)$ at different light intensities and yields

$$\eta_{12}(V) = \frac{J_1(V) - J_2(V)}{J_{sc,1} - J_{sc,2}}. \tag{B.4}$$

The calculated collection function gives only the true collection efficiency if the diode currents $J_{diode,1}(V)$ and $J_{diode,2}(V)$ are independent of the illumination intensity. Otherwise $\eta(V)$ also contains the intensity dependence of the diode current [50]. To exclude effects of an illumination dependent diode current the IV curve can be measured at several light intensities, say 4 different intensities, and the collection efficiencies can be compared. If the calculated collection functions are congruent then $\eta(V) = \eta_{12}(V) = \eta_{34}(V)$ in the measured range of light intensities [50, 161, 162].

Measured collection efficiencies based on illumination dependent IV curves yield collection efficiencies at V_{oc} of around 50 % or even below [60, 162]. These values for $\eta(V_{oc})$ are too low for the model of a voltage dependent SCR [163]. However, also different models exist, for example

for a n-i-p structure [164], as it is used for a-Si and a-SiGe solar cells [165] and which also shows good agreement with the measured collection functions for CdTe cells [162]. This model can also explain a cross over of the dark and illuminated IV curve [166]. For far enough forward bias, the electric field is reversed and the photogenerated carriers are swept into the opposite direction than under operating conditions [166].

However, these strongly voltage depdendent collection efficiencies can also be an artefact due to the violation of the assumption of an illumination independent diode current. CIGSe and CdTe based thin-film solar cells exhibit generally a cross over between the light and the dark IV curves, which arises due to barriers either at the back [126] or at the front contact [128,143]. Thus, the measured collection efficiency would only be an artefact. In fact, for thin film solar cells based on $CuInSe_2$ and CdTe, the collection efficiency was calculated based on a model of a voltage dependent SCR width [163]. It was found that the collection efficiency decreases at V_{oc} only by a few percent and can be misinterpreted as an increased shunt resistance.

As CIGSe and CZTSe based solar cells do not resemble a n-i-p structure and the calculated low influence of the collection efficiency at V_{oc}, the effect of $\eta(V_{oc})$ is neglected for the extrapolation of the V_{oc} data.

APPENDIX

C

IVT MEASUREMENTS

C.1. V_{oc} extrapolation

The extrapolation of the V_{oc} with respect to temperature to 0 K is a common method [61, 72] to deduce the activation energy of J_0. The analysis is based on Eqn. (2.14):

$$V_{oc} = \frac{E_A}{q} - \frac{AkT}{q} \ln\left(\frac{J_{00}}{J_{ph}}\right),$$

where the V_{oc} is measured at different temperatures. However, a simple plot of V_{oc} versus temperature and the determination of E_A is only valid if the diode quality factor is temperature independent and the photo current collection is not reduced too much at V_{oc}. An discussion about the collection function can be found in appendix B, where it is concluded that the collection at V_{oc} is diminished only by a few percent.

The diode quality factor on the other hand has a temperature dependence and thus needs to be taken into account for the determination of E_A according to Eqn. (2.14). The temperature dependence of the diode quality factor of a measured CZTSe high temperature co-evaporated solar cell is show in Fig. (C.1b). The data was fitted with the model of tunneling enhanced recombination via an exponential decrease of tailstates from one of the band edges towards midgap [167]. In that case the diode quality factor reads

$$A = \frac{2}{1 + \frac{T}{T^*} - \frac{E_{00}^2}{3(kT)^2}}. \tag{C.1}$$

E_{00} is the tunneling energy and kT^* the characteristic energy of the defect distribution. It needs to be noted that Eqn. (C.1) is only valid for $kT^* > kT \geq E_{00}$ [69]. Thus, it needs to be taken care that there is no discrepancy between the fitting range and the fitted value of E_{00}. The fitting limits for the diode quality factor are shown as dashed black lines in Fig. (C.1b). The lower limit is at 166 K, while $E_{00}/k = 164$ K and thus is not in contradiction with the fitting range.

With the model of a temperature dependent diode quality factor, the IV curves in Fig. (C.1a) are simulated according to the one diode model (Eqn. (2.12)) for temperatures between 160 K and 320 K. The temperature dependence of the extracted V_{oc} from these simulated curves is shown in Fig. (C.1d) (bottom ordinate) as a solid blue line and labelled as 'model'. An

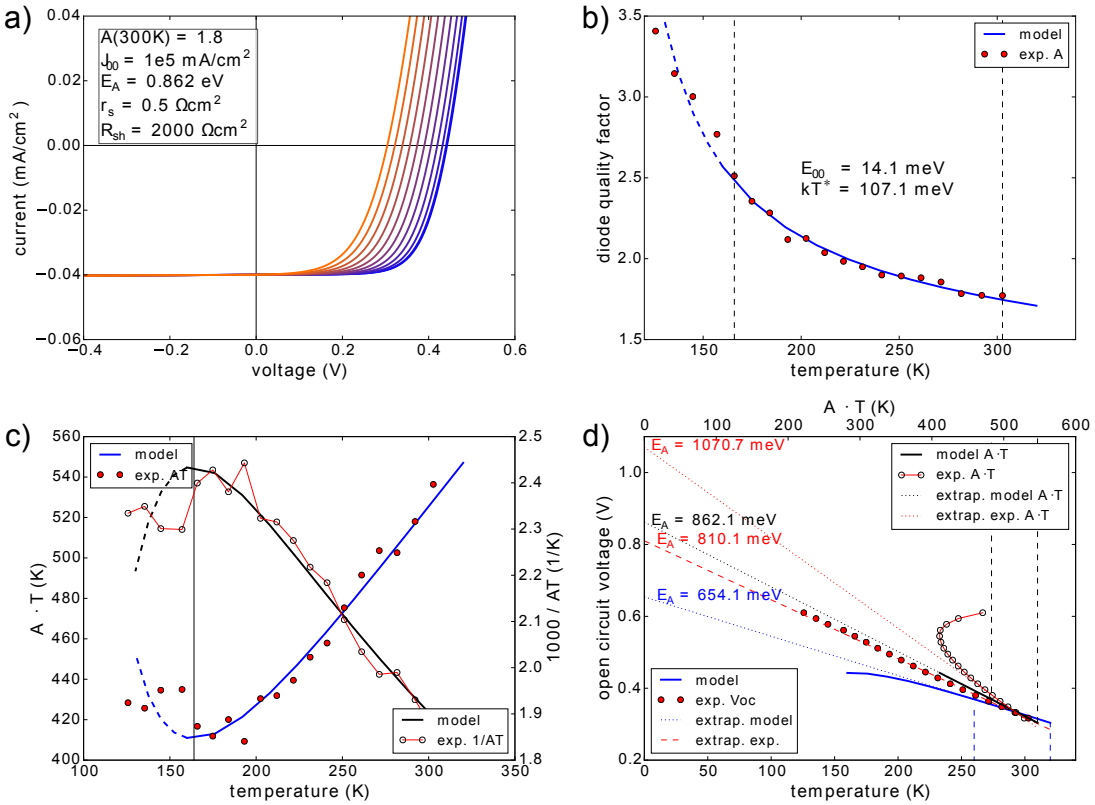


Figure C.1.: ***Simulation of temperature dependent IV curves*** *- The curves were simulated in a temperature range between 160 K and 320 K. The temperature dependence of the diode quality factor is calculated with a model of tunneling enhanced recombination via an exponential band tail [167].*

extrapolation of the modelled V_{oc} data to zero temperature (dotted blue line) yields an intercept with the ordinate of 654.1 mV and thus results in an activation energy much lower than the activation energy, which was put into the model of $E_A = 0.862\,\mathrm{eV}$. This activation energy was determined from QE measurements as it is shown in Fig. (C.2). However, in order to account for the temperature dependence of the diode quality factor the same modelled V_{oc} data was plotted versus $A \cdot T$ (Fig. (C.1d), upper ordinate) as a black solid line and labelled as 'model A · T'. The extrapolation of $A \cdot T$ to 0 K (dotted black line) yields the correct activation energy of 862 meV. As can be seen from Fig. (C.1c), the modelled $A \cdot T$ data (left abscissa, blue solid line) still yields a straight line with a positive slope at high temperatures. Thus, lowering the temperature increases the V_{oc} but to a smaller extent than with a temperature independent diode quality factor. For temperatures of $kT \approx E_{00}$ (solid black line), the slope of $A \cdot T$ becomes zero and thus V_{oc} does not rise anymore by lowering the temperature. Of course, the model of the temperature dependent diode quality factor given by Eqn. (C.1) is not valid anymore at these temperatures, but nevertheless, this behaviour is observed experimentally (Fig. (C.1c), solid red circles).

The experimental V_{oc} data is also shown in Fig. (C.1d). Plotting the data simply versus temperature (full red circles, lower ordinate) yields a straight line. The extrapolation (dashed red line) results in an activation energy only slightly below the bandgap of 862 meV. Extrapolating the experimental V_{oc} data versus $A \cdot T$ (open red circles) an activation energy higher than the bandgap of 1070 meV is obtained (dotted black line indicates the extrapolation). Interestingly, the experimental V_{oc} data always shows higher values than the modelled V_{oc} data. This fact is especially noticeable by the plot of V_{oc} versus $A \cdot T$, where the V_{oc} still raises, while $A \cdot T$ already increases by lowering the temperature. Therefore, there is either another factor, which increases the V_{oc} by lowering the temperature or the deduced diode quality factors are incorrect.

An issue which is observed in thin film compound solar cells are energy fluctuations of the saturation current density, either at the interface or in the bulk of the absorber [46,62,168], for example due to bandgap fluctuations. In that case the saturation current density is written as

$$J_0 = \int_0^\infty \mathrm{d}E_A P(E_A) \cdot J_{00} \exp\left(-\frac{E_A}{AkT}\right). \tag{C.2}$$

With a Gaussian distribution $P(E_A)$ of activation energies, the integration in Eqn. (C.2) yields

$$J_0 = J_{00} \exp\left(-\frac{\bar{E_A} - \frac{\sigma^2}{2A'kT}}{A'kT}\right). \tag{C.3}$$

$\bar{E_A}$ denotes the mean energy, σ the width of the Gaussian distribution and A' the temperature independent diode quality factor. According to Scheer *et al.* [62] the evaluation of the IV-curve with J_0 given by Eqn. (2.13) would result in a temperature dependent diode quality factor given by

$$A(T) = \frac{A'}{\frac{\bar{E_A}}{E_A} - \frac{\sigma^2}{2E_AkT}}, \tag{C.4}$$

where E_A is the activation energy, which would be obtained with the evaluation of J_0 according to Eqn. (2.13). However, I do not see that this could explain the temperature dependence of the experimentally deduced diode quality factor. Experimentally, the diode quality factor is

obtained from the voltage dependence of the IV curve, which should not be affected by any variations in the bandgap of the absorber layer, i.e. an additional temperature dependence of J_0 with respect to temperature.

Using Eqn. (C.3), the V_{oc} expresses as

$$V_{oc} = \frac{\bar{E_A}}{q} - \frac{A(T)kT}{q} \ln \frac{J_{00}}{J_{ph}} - \frac{\sigma^2}{2q} \frac{1}{A(T)kT}. \tag{C.5}$$

The collection efficiency at V_{oc} is neglected [163], i.e. $\eta(V_{oc}) = 1$. The last term in expression (C.5) accounts for the reduction of the effective activation energy due to bandgap fluctuations, which was not present in Eqn. (2.14). This additional term is positive and therefore reduces the V_{oc}. As shown in Fig. (C.1c) (open circles), the slope of $1/AT$ versus T is negative. Therefore, the additional reduction of V_{oc} due to bandgap fluctuations increases with respect to temperature. Hence, it cannot explain the observed high V_{oc} values for the determined diode quality factors.

Experimentally, the V_{oc} yields a straight line. Also for other samples, the high temperature regime (generally at least above 200 K) forms a straight line. The deduced activation energies lie all roughly around the bandgap or a bit lower (see section 6.4.1 and Fig. (6.17)). Since there is no better method for the determination of E_A, the simple model according to Eqn. (2.14) is used. However, due to the discrepancy of the model with the experimentally observed temperature dependent diode quality factor, care must be taken when assigning the dominant recombination pathway to interface or bulk dominated recombination.

C.2. QE of sample from V_{oc} extrapolation analysis

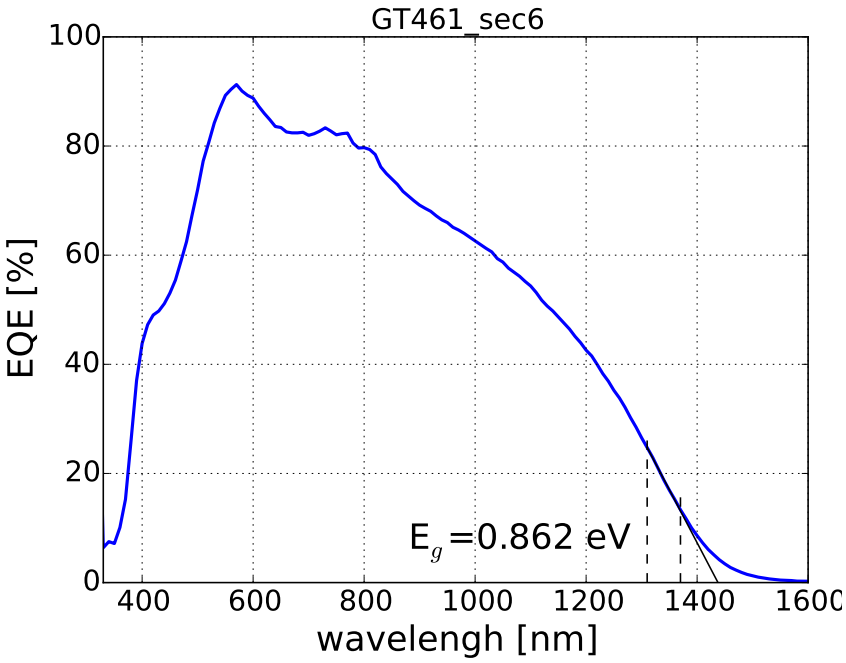


Figure C.2.: ***QE of the sample used for*** V_{oc} ***extrapolation analysis*** *- Long wavelength regime was fitted linearly to extrapolate the bandgap energy. Fitting limtis are denoted as black dashed lines.*

C.3. Evaluation of dark IV curves of as-grown co-evaporated samples

As shown in Fig. (6.12), the evaluation of the IV curves with the Sites method yields a thermally activated series resistance. The IV fit routine however results in a rather constant series resistance due to the failure of the fit of the curves measured at low temperatures. Exemplary fits of the as-grown co-evaporated samples presented in Fig. (6.5) are shown for four different temperatures in Fig. (C.3). At lowered temperatures (Fig. (C.3a) and (C.3b)), the fit does not pass through the origin, i.e. 0 current at 0 voltage, and also the diode like regime is not fitted correctly: First, the diode quality factor is overestimated as evident by the smaller slope of the linear part. Second, the series resistance is underestimated as the bending from the linear part is smaller compared to the measured data. Thus, the Sites method seems to be more appropriate for the evaluation of the series resistance and its activation energy.

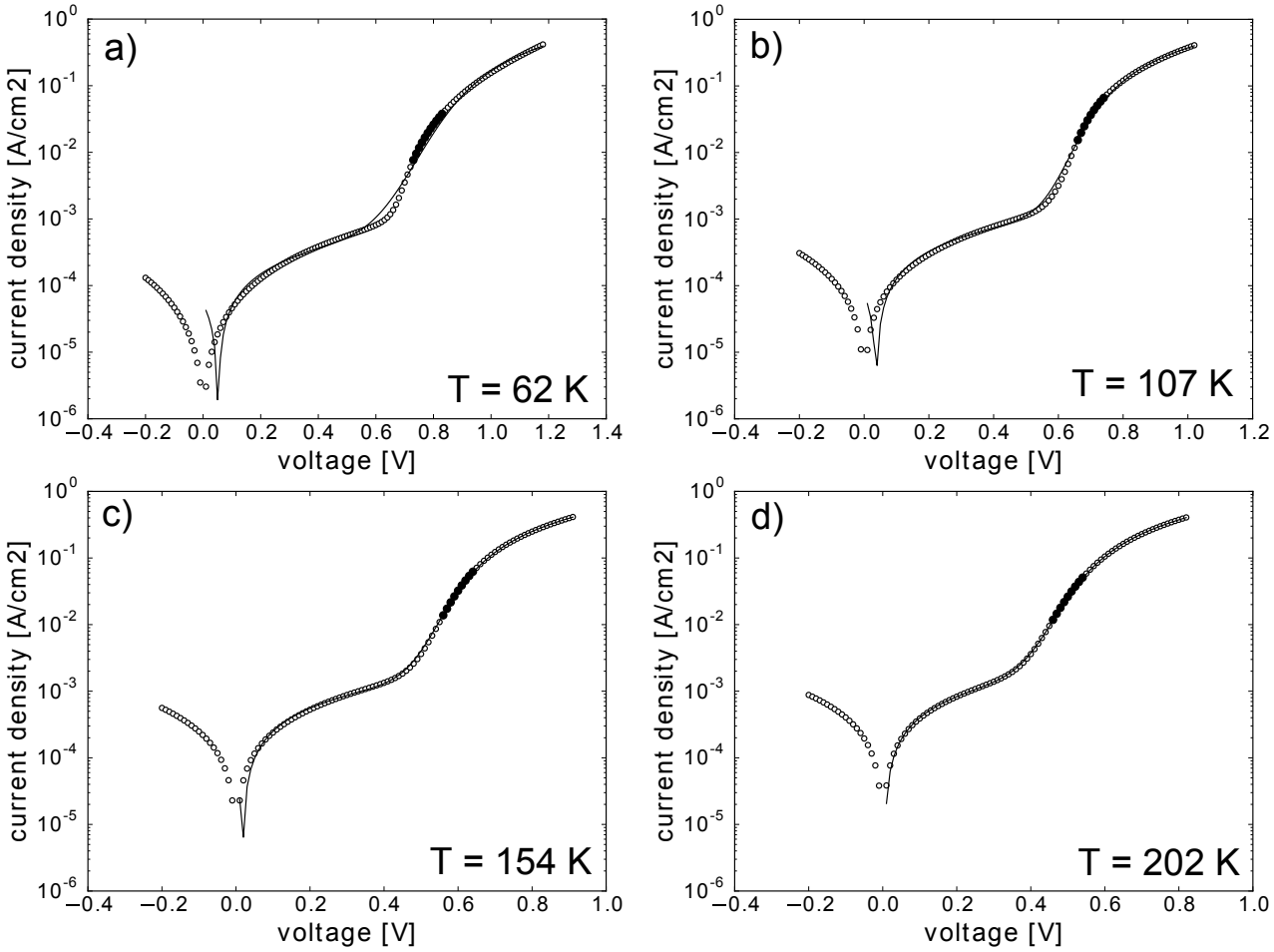


Figure C.3.: ***Fitting the IV curves of as-grown co-evaporated samples*** *- It is evident that the fit at low temperatures fails. The diode quality factor is over estimated and the series resistance underestimated.*

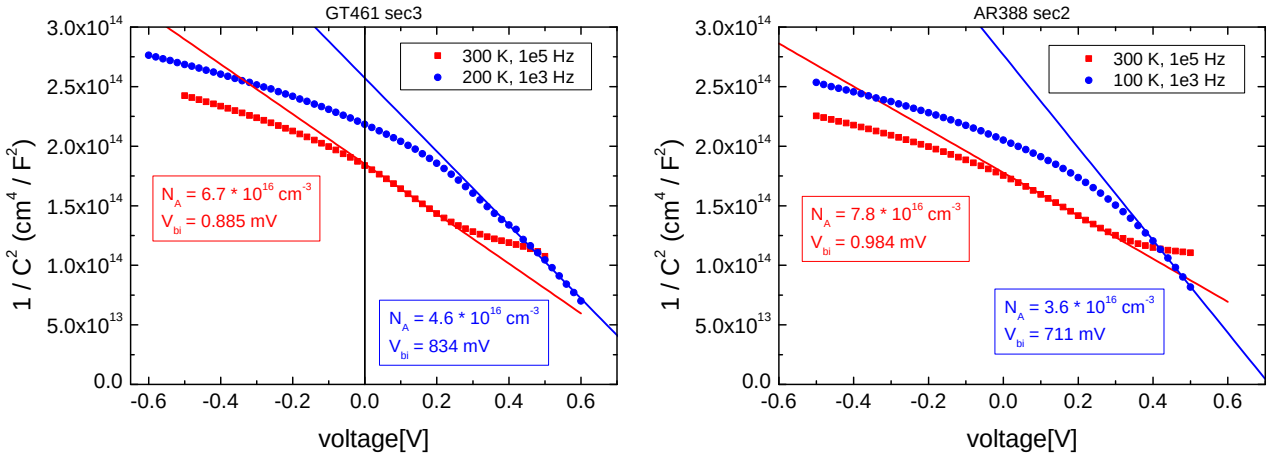
APPENDIX

D

ADDITIONAL GRAPHS OF CAPACITANCE MEASUREMENTS

D.1. CV of as-grown high temperature co-evaporated samples

The CV measurements for the two samples presented in section 5.6.1. The admittance spectra of these two samples are shown in Fig. (5.22).



(a) from single stage process *(b) from multi-stage process*

Figure D.1.: ***CV measurements from devices with as grown co-evaporated absorbers*** *- The measurement at 300 K is already influenced by the dc current of the diode, which is seen by the leveling off around 0.4 V. At low temperatures J_0 (c.f. Eqn. (2.12) and (2.13)) decreases and the onset of the exponential diode current is shifted to higher voltages. Thus, the bending of the Mott-Schottky plot is clearly visible.*

D.2. Capacitance derivative after heat treatment

Fig. (D.2) shows the derivative of the capacitance spectra shown in Fig. (5.24). The two graphs on the left hand side result from the as-grown samples. Upper and lower right graph arise from

the samples with the low temperature heat treatment and the high temperature annealing, respectively.

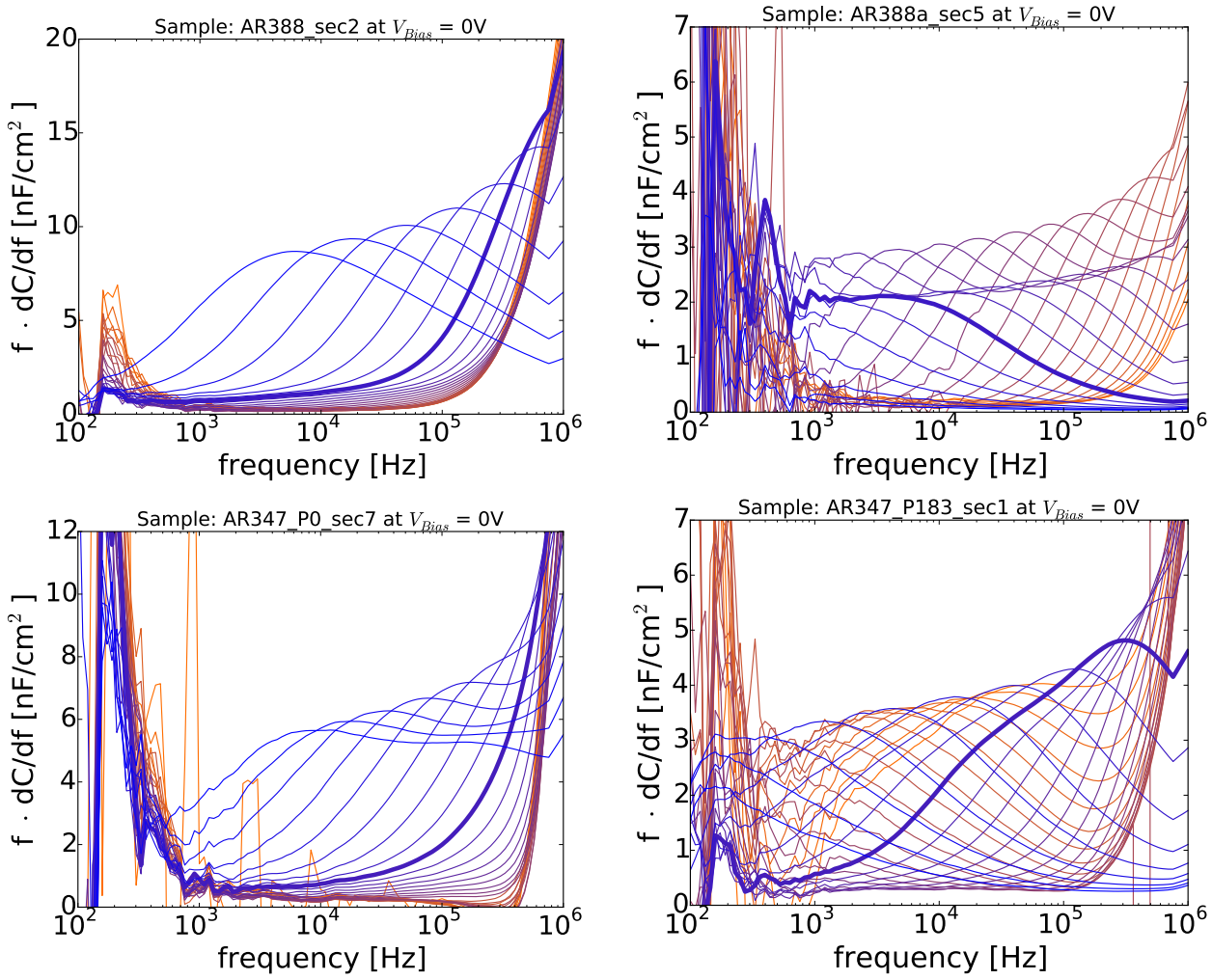


Figure D.2.: ***Impact of different heat treatments on the derivative of the capacitance spectrum*** *- Left hand side shows the spectra from the solar cells originating from the as grown absorbers. Right graphs show the spectra after the absorber layers underwent an additional heat treatment. Upper right shows the low temperature heat treatment, lower right the high temperature annealing.*

APPENDIX

E

CDS THICKNESS VARIATION

E.1. Device characteristics

Fig. (E.1) shows the IV curves and the EQE spectra of the devices with different CdS thicknesses, which were later further investigated by IVT and admittance measurements. Tab. E.1 summarizes the IV parameters of these solar cells. Noticeable is an inferior solar cell behaviour for the one with 1.0 CdS runs. This is due to inhomogeneities across the sample. All solar cells from the processes described in section 3.4 were slightly inhomogeneous in a way that one corner showed poor efficiencies as shown in Fig. (E.2)[1]. For the set of solar cells with the CdS thickness variation only 3 inch × inch absorber substrates were available[2] and therefore, one absorber substrate was cut in half. From these half absorber layers the solar cells with 1.0 CdS and 2.0 CdS runs were made. The inhomogeneous part was evidently located on the part with 1.0 CdS thickness.

Fig. (E.1b) shows a similar QE behaviour for all three devices for wavelengths, which are not absorbed in the CdS layer. For thinner CdS buffer layers, less photons with energies above 2.4 eV (bandgap of CdS) are absorbed in that layer and therefore a higher QE is obtained. As mentioned in the figure capture, the sample with 1.0 CdS runs could not be measured.

All devices listed in Tab. E.1 show rather high J_{sc} values as measured by IV (c.f. section 4.4). Besides, the J_{sc} values do not show the trend, which is suggested by the EQE curves, i.e. a higher short circuit current for thinner CdS buffer layers. Thus, the J_{sc} is calculated from the EQE using an AM1.5G spectrum according to

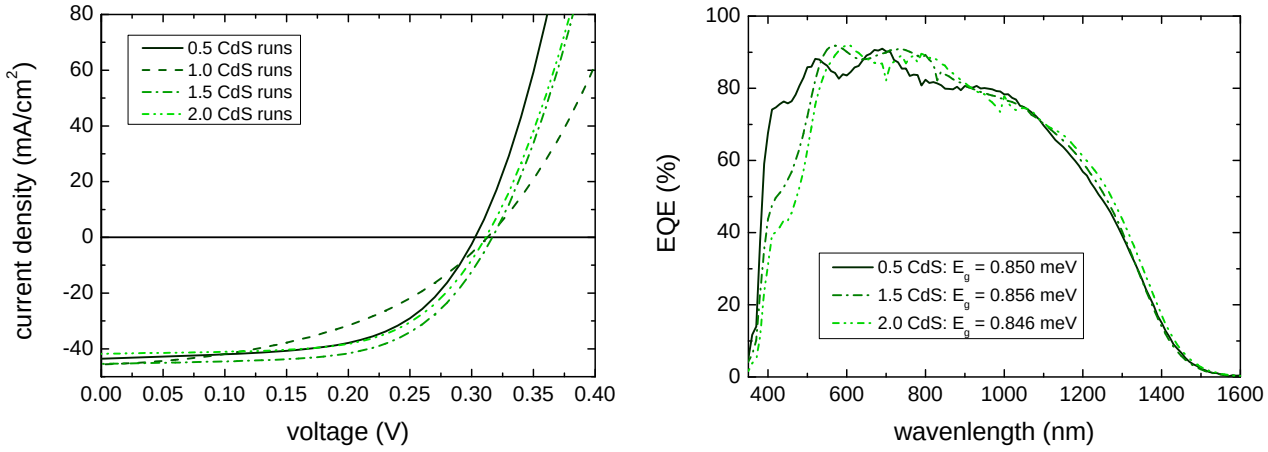
$$J_{sc} = q \int \mathrm{d}E \; b_s(E) EQE(E), \tag{E.1}$$

where $b_s(E)$ is the incident spectral photon flux density [169]. The J_{sc} values calculated from the EQE curve are given in Tab. E.1 as well ($J_{sc}(EQE)$). As expected, a lower $J_{sc}(EQE)$ is observed for thicker CdS buffer layers due to the absorption in the CdS as already indicated by the EQE curves. The efficiency is corrected for the $J_{sc}(EQE)$ values and is given in the last column. For the device with 1.0 CdS runs, the mean $J_{sc}(EQE)$ value of the devices with

[1] This might occur due to the *in-situ* low temperature heat treatment. Samples from the standard process did not show this inhomogeneity.

[2] One absorber layer substrate was accidentally processed *as a standard* in another deposition run for the CdS buffer layer and the window layer.

0.5 CdS runs and 1.5 CdS runs is taken to calculate corrected efficiency and is therefore put into brackets. Note that the IV curves are measured with a cold mirror halogen lamp and thus with another spectrum than the AM1.5G. Nevertheless, such a strong deviation between the J_{sc} values determined from IV and EQE are generally not observed and could arise from an unstable halogen lamp (operated at the end of its lifetime).



(a) IV curves *(b) EQE curves*

Figure E.1.: ***Device characteristics with different CdS thicknesses*** *- Except the solar cell with 1.0 CdS runs, the IV curves show proper diode behaviour (a). The 1.0 CdS runs sample shows inferior diode behaviour due to an inhomogeneous absorber (see details in the text). EQE spectra shown in (b) show the same long wavelength behaviour but differ at short wavelengths due to absorption in the CdS buffer layer. The EQE spectra were measured after IVT and admittance measurements. The sample with 1.0 CdS runs broke after these measurements and therefore could not be measured.*

Table E.1.: *Summary of solar cells with different CdS thicknesses and their IV parameters.*

CdS runs	nom. thickness (nm)	eff. (%)	FF (%)	V_{oc} (mV)	J_{sc} (IV) (mA/cm^2)	J_{sc} (EQE) (mA/cm^2)	eff. corr. (%)
0.5	25	7.8	59.2	303	43.2	39.6	7.2
1.0	50	6.3	44.3	313	45.6	N/A	(5.4)
1.5	75	8.8	61.2	316	45.4	39.1	7.6
2.0	100	8.0	61.5	311	41.8	38.5	7.4

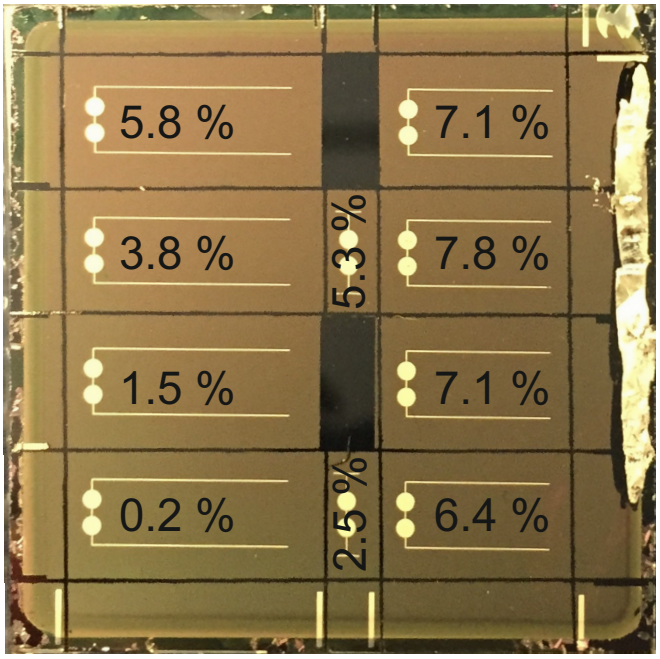


Figure E.2.: ***Inhomogeneity issues of absorbers for the CdS thickness variation*** *- One corner of the devices on the inch × inch substrate shows poor solar cell efficiencies due to absorber inhomogeneities.*

E.2. Fitted capacitance spectra for CdS thickness series

The fitted capacitance spectra and their respective fitting parameters are shown in Fig. (E.3) and Tab. E.2, respectively. All spectra were fitted with the weights $w_C = 1$ and $w_d = 3$ (c.f. Eqn. (5.54)).

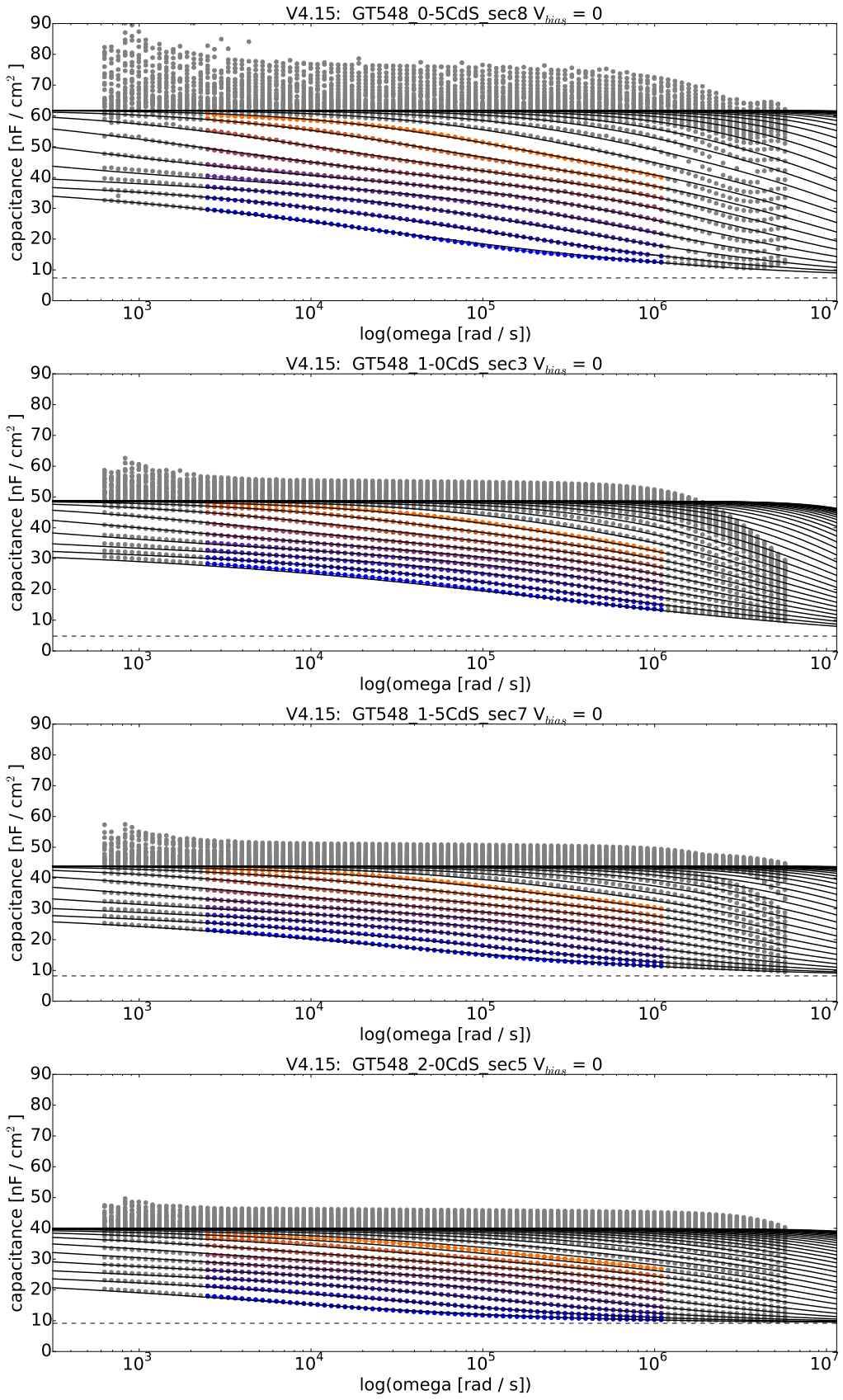


Figure E.3.: ***Fitted capacitance spectra of the samples with varying CdS buffer layers*** *- High temperature capacitance data is always excluded from the fit as no frequency dependence is observed. Parameters of the fits are listed in Tab. E.2. Dashed black lines indicated the fitted geometrical capacitance.*

Table E.2.: *Fitting parameters for the capacitance spectra shown in Fig. (E.3).*

parameter	unit	0.5 CdS runs	1.0 CdS runs	1.5 CdS runs	2.0 CdS runs
E_{A1}	meV	38	21	37	38
ν_1	s^{-1}	$9.5 \cdot 10^8$	$1.1 \cdot 10^8$	$7.4 \cdot 10^8$	$6.8 \cdot 10^8$
σ_1	meV	13.4	14.4	12.8	9.5
ΔC_1	nF/cm^2	29.6	28.7	18.8	10.0
E_{A2}	meV	115	93	105	88
ν_2	s^{-1}	$3.5 \cdot 10^{10}$	$4.3 \cdot 10^{10}$	$1.7 \cdot 10^{10}$	$4.2 \cdot 10^9$
σ_2	meV	20.2	18.9	21.6	32.6
ΔC_2	nF/cm^2	24.8	17.1	16.9	20.8
C_{inf}	nF/cm^2	7.4	4.8	8.2	9.2

APPENDIX

F

PUBLICATIONS AND CONFERENCE CONTRIBUTIONS

Publications

- T. P. Weiss, A. Redinger, J. Luckas, M. Mousel and S. Siebentritt, Admittance spectroscopy in kesterite solar cells: defect signal or circuit response, Appl. Phys. Lett., **102**, 202105, 2013.

- T. P. Weiss, A. Redinger, J. Luckas, M. Mousel and S. Siebentritt, Role of high series resistance in admittance spectroscopy of kesterite solar cells, Proceedings of 39th IEEE PVSC, pages 3066 - 3070, Tampa, 2013.

- T. P. Weiss, A. Redinger, D. Regesch, M. Mousel and S. Siebentritt, Direct Evaluation of Defect Distributions From Admittance Spectroscopy, IEEE Journal of Photovoltaics, Vol. 4, pages 1665 - 1670, 2014.

- T. P. Weiss, A. Redinger, G. Rey, T. Schwarz, M. Spies, O. Cojocaru-Mirédin, P.-P. Choi and S. Siebentritt, Low temperature heat treatment for improved collection properties of co-evaporated $Cu_2ZnSnSe_4$ based solar cells, (under review).

- M. Mousel, T. Schwarz, R. Djemour, T. P. Weiss, J. Sendler, J. C. Malaquias, A. Redinger, O. Cojocaru-Mirédin, P.-P. Choi and S. Siebentritt, Cu-Rich Precursors Improve Kesterite Solar Cells, Adv. Energy Mater. Vol. 4, 1300543, 2013.

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- S. Siebentritt, G. Rey, A. Finger, D. Regesch, J. Sendler, T. P. Weiss, T. Bertram, What is the Bandgap of Kesterite?, Solar Energy Materials and Solar Cells, (under review).
- Ö. Demiricioğlu, N. Neugebohrn, M. Mousel, A. Redinger, G. Rey, T. P. Weiss, S. Siebentritt, I. Riedel, L. Gütay, Detection of a $MoSe_2$ Secondary Phase Layer in CZTSe by Spectroscopic Ellipsometry, (submitted).
- G. Rey, T. P. Weiss, J. Sendler, A. Finger, C. Spindler, F. Werner, M. Melchiorre, M. Hála, S. Siebentritt, Ordering kesterite improves solar cells: a low temperature post-deposition annealing study, (submitted).

Oral presentations

- T. P. Weiss, A. Redinger, J. Luckas, M. Mousel and S. Siebentritt, Role of high series resistance in admittance spectroscopy of kesterite solar cells, 39th IEEE PVSC, Tampa, 2013.
- T. P. Weiss, A. Redinger, J. Luckas, M. Mousel and S. Siebentritt, Role of high series resistance in admittance spectroscopy of kesterite solar cells, 4th European Kesterite Workshop, Berlin, 2013.
- T. P. Weiss, A. Redinger and S. Siebentritt, (*invited talk*) How to make efficient kesterite solar cells by co-evaporation, IW-CIGSTech 5 Workshop, Berlin, 2014.
- T. P. Weiss, A. Redinger, D. Regesch, M. Mousel and S. Siebentritt, Direct evaluation of defect distributions from admittance spectroscopy, 40th IEEE PVSC, Denver, 2014.

Poster presentations

- T. P. Weiss, A. Redinger, G. Rey, M. Mousel and S. Siebentritt, Sequential process or co-evaporation: Comparison of IVT and admittance data, 5th European Kesterite Workshop, Tallinn, 2014.
- T. P. Weiss, A. Redinger, G. Rey, M. Mousel, T. Schwarz, O. Cojocura-Mirédin, P.-P. Choi and S. Siebentritt, Sequential process or co-evaporation: Comparison of IVT and admittance data, MRS Spring Meeting, San Francisco, 2015.

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